PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5941788

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
CHIAO TUNG HOLDINGS, LLC	11/26/2019

RECEIVING PARTY DATA

Name:	INTELLECTUAL VENTURES ASSETS 158 LLC
Street Address:	251 LITTLE FALLS DRIVE
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 22

Property Type	Number
Patent Number:	6225830
Patent Number:	6034955
Patent Number:	6108528
Patent Number:	6084925
Patent Number:	6094490
Patent Number:	6134288
Patent Number:	6169504
Patent Number:	6079623
Patent Number:	5874844
Patent Number:	6169808
Patent Number:	6212249
Patent Number:	6285789
Patent Number:	6053641
Patent Number:	6081137
Patent Number:	6088112
Patent Number:	6133860
Patent Number:	6163299
Patent Number:	6188244
Patent Number:	6269134
Patent Number:	6314087

Property Type	Number
Patent Number:	6434112
Patent Number:	6452963

CORRESPONDENCE DATA

Fax Number: (404)645-7707

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4046457700
Email: docketing@mcciplaw.com
Correspondent Name: LAWRENCE AARONSON
Address Line 1: 999 PEACHTREE STREET NE
Address Line 2: SUITE 1300
Address Line 4: ATLANTA, GEORGIA 30309

ATTORNEY DOCKET NUMBER:	11206-001GEN
NAME OF SUBMITTER:	LAWRENCE A. AARONSON
SIGNATURE:	/Lawrence A. Aaronson/
DATE SIGNED:	02/01/2020

Total Attachments: 16
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page1.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page2.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page3.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page4.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page5.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page6.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page7.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page8.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page9.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page10.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page11.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page12.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page13.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page14.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page15.tif
source=Chiao Tung Holdings, LLC to IVA 158 LLC (Fully Executed)_26 Nov 2019#page16.tif

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Chiao Tung Holdings, LLC, a Delaware limited liability company, having an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Intellectual Ventures Assets 158 LLC, a Delaware limited liability company, having an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignee***"), or its designees, the right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "*Certain Assets*"):

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
(DE19901185.0)	DE	(1/14/1999)	NAND/NOR gate combination for operation in differential mode Ra, Youn-Wook
KR10-0275948 (KR10-1998-0013204)	KR	9/25/2000 (4/14/1998)	Differential Mode NAND/NOR Gate Ra, Youn-Wook
6225830 (09/290543)	US	5/1/2001 (4/12/1999)	Differential mode logic gate having NAND and NOR portions to produce complementary outputs Ra, Youn-Wook
JP3101812 (JP09-292412)	JP	8/25/2000 (10/24/1997)	Data Transmitter-Receiver And Data Transmission/Reception Method For Serially Transmitting And Receiving Data Cho, Dong Soo
KR10-0198669 (KR10-1996-0048004)	KR	3/2/1999 (10/24/1996)	Apparatus and method for serial interfacing Cho, Dong Soo
6034955 (08/931718)	US	3/7/2000 (9/16/1997)	Single line interface system and method thereof Cho, Dong Soo
DE19719115.0 (DE19719115.0)	DE	7/13/2006 (5/6/1997)	Squelch circuit for removing noise in data signal LYU HYUNG LYUL
(JP09-302073)	JP	(11/4/1997)	RECEPTION SQUELCH CIRCUIT HAVING PULSE WIDTH DETECTING FUNCTION LYU HYUNG LYUL

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6108528 (08/958929)	US	8/22/2000 (10/28/1997)	Receive squelch circuit having function of detecting pulse width Lyu, Hyung Lyul
KR10-0239705 (KR10-1996-005{755)	KR	10/21/1999 (11/4/1996)	Squelch Circuits For Detecting Pulse Width RYU HYUNG-RYUL
DE19727431.5 (DE19727431.5)	DE	2/20/2004 (6/27/1997)	Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
GB2315000 (GB9713710.3)	GB	11/21/2000 (6/27/1997)	A Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
JP3155728 (JP09-168744)	JP	2/2/2001 (6/25/1997)	Synchronous And Asynchronous Decision Method And Device For Viterbi Decoding Signal Baek, Jong Seob
6084925 (08/884685)	US	7/4/2000 (6/27/1997)	Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
TWI097086 (TW086108935)	TW	10/1/1998 (6/26/1997)	A METHOD AND APPARATUS FOR DISCRIMINATING SYNCHRONOUS OR ASYNCHRONOUS STATES OF VITERBI DECODED DATA Baek, Jong Seob
KR10-0223735 (KR10-1996-0026546)	KR	7/12/1999 (6/29/1996)	Device Of Judging Synchronous / Asynchronous State Of Viterbi Decoding Signal Baek, Jong Seop
JP3194135 (JP09-323121)	JP	6/1/2001 (11/25/1997)	Digital Audio Processor Unable to Verify

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6094490 (08/978474)	US	7/25/2000 (11/25/1997)	Noise Gate Apparatus For Digital Audio Processor Unable to Verify
TW1097354 (TW086103866)	TW	9/21/1998 (3/26/1997)	Noise Gate Apparatus For Digital Audio Processor Unable to Verify
KR10-0179936 (KR10-1996-0058085)	KR	11/28/1998 (11/27/1996)	Noise Gate Device Of Digital Audio Processor Unable to Verify
DE19745780.0 (DE19745780.0)	DE	11/14/2003 (10/16/1997)	Title Not Available Baek, Jong Seob
GB2318710 (GB9721865.5)	GB	4/18/2001 (10/15/1997)	Apparatus And Method For Generating A Decoding Clock Signal In Response To A Period Of Write And Read Clock Signals Baek, Jong Seob
JP3094285 (JP09-299463)	JP	8/4/2000 (10/16/1997)	Decoding Clock Generator By Coding Rate And Its Method Baek, Jong Seob
6134288 (08/953009)	US	10/17/2000 (10/16/1997)	Apparatus And Method For Generating A Decoding Clock Signal In Response To A Period Of Write And Read Clock Signals Baek, Jong Seob
KR10-0233291 (KR10-1996-0046238)	KR	9/10/1999 (10/16/1996)	Restoring Clock Generator According To Coding Ratio And Method Thereof Baek, Jong Seop
DE19822784.1 (DE19822784.1)	DE	2/7/2003 (5/20/1998)	Analog-to-digital converter using interleaved sampling Park, Yong-Pal
(JP10-346399)	JP	(12/7/1998)	Analog / Digital Converter Park, Yong-Pal

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6169504 (09/172075)	US	1/2/2001 (10/14/1998)	Device And Method For Converting Analog Signal To Digital Signal Using Interleaving Sampling Park, Yong-Pal
KR10-0286326 (KR10-1997-0068515)	KR	1/11/2001 (12/13/1997)	Interleaving Sampling Analog / Digital Converter Park, Yong-Pal
KR10-0242462 (KR10-1996-0052656)	KR	11/10/1999 (11/7/1996)	I/O Address Mapping Device Using Indexing Mechanism Ahn, Mun Weon
6079623 (08/965766)	US	6/27/2000 (11/7/1997)	Apparatus for mapping memory PCMCIA cards into I/O window address space to select an internal register and perform read and write operations using an index mechanism Ahn, Mun Weon
(DE19751301.8)	DE	(11/19/1997)	Schmitt-trigger circuit for input buffer Shin, Dong Young
(JP09-332731)	JP	(12/3/1997)	SCHMITT TRIGGER CIRCUIT CAPABLE OF ADJUSTING TRIGGER VOLTAGE Shin, Dong Young
5874844 (08/905716)	US	2/23/1999 (8/4/1997)	SCHMITT TRIGGER CIRCUIT WITH AN ADJUSTABLE TRIGGER VOLTAGE Shin, Dong Young
KR10-0215839 (KR10-1997-0009450)	KR	5/26/1999 (3/20/1997)	SCHMIDT TRIGGER CIRCUIT CAPABLE OF CONTROLLING TRIGGER VOLTAGE Unable to Verify
DE19818020.9 (DE19818020.9)	DE	11/22/2004 (4/22/1998)	Signal compression circuit Kim, Seong-Ryeol
6169808 (09/037175)	US	1/2/2001 (3/9/1998)	Signal compressing circuit Kim, Seong-Ryeol

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
KR10-0275937 (KR10-1997-0046060)	KR	9/25/2000 (9/6/1997)	A CIRCUIT FOR DATA COMPRESSION Unable to Verify
(JP09-236828)	JP	(9/2/1997)	DATA ISOLATING CIRCUIT Shin, Byeong Cheol
6212249 (08/921586)	US	4/3/2001 (9/2/1997)	DATA SEPARATION CIRCUIT AND METHOD Shin, Byeong Cheol
KR10-0205354 (KR10-1996-0037839)	KR	4/2/1999 (9/2/1996)	DATA SEPARATION CIRCUIT Shin, Byeong Cheol
6285789 (09/154094)	US	9/4/2001 (9/16/1998)	Variable length code decoder for MPEG Kim, Young Goan
KR10-0253366 (KR10-1997-0065566)	KR	1/22/2000 (12/3/1997)	Variable length code decoder for MPEG Kim, Young Goan
(JP09-354217)	JP	(12/8/1997)	Fiber Pig Tail For Optical Communication Module Chun, Sung-Hak
KR10-0272265 (KR10-1996-0077822)	KR	8/23/2000 (12/30/1996)	Fiber Pigtail For A Optical Communication Module Chun, Sung Hak
6053641 (08/999150)	US	4/25/2000 (12/29/1997)	Fiber Pigtail For Optical Communication Module Chun, Sung-Hak
KR10-0259590 (KR10-1998-0000287)	KR	3/25/2000 (1/8/1998)	Frequency Detection Circuit Choi, Sang-Shin
TWI115402 (TW087113575)	TW	5/11/2000 (8/18/1998)	Frequency Ddetecting Circuit Choi, Sang-Shin

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6081137 (09/166960)	US	6/27/2000 (10/6/1998)	Frequency Detecting Circuit Choi, Sang-Shin
KR10-0296136 (KR10-1998-0024574)	KR	5/7/2001 (6/27/1998)	Image sensor having test pattern for determining characteristics of color filter Unable to Verify
6088112 (09/344823)	US	7/11/2000 (6/25/1999)	Image Sensor Having Test Patterns For Measuring Characteristics Of Color Filters Unable to Verify
JP3691261 (JP10-316234)	JP	6/24/2005 (11/6/1998)	Data Changeable Device For Variable Length Decoder Ryu, Seung-Chol
6133860 (09/186637)	US	10/17/2000 (11/6/1998)	A VARIABLE LENGTH DECODER WITH ENHANCED ROUTING OF DATA TO MULTIPLEXERS Ryu, Seung-Chol
KR10-0292050 (KR10-1997-0058867)	KR	3/19/2001 (11/8/1997)	Data Simulator Of Variable Length Decoder Kim, Yong Hwan
(DE19840020.9)	DE	(9/2/1998)	Wireless Subscriber Connection Cable System With Patch Antenna Park, Yong-Pal
KR10-0286331 (KR10-1998-0003575)	KR	1/11/2001 (2/7/1998)	Wireless Local Loop System Using Patch Antenna Park, Yong Pal
6163299 (09/244089)	US	12/19/2000 (2/4/1999)	Wireless Local Loop System Using Patch-Type Antenna Park, Yong-Pal
(DE19818021.7)	DE	(4/22/1998)	Input Buffer Circuit With Hysteresis Characteristic Joo, Yang-Sung

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
JP2973115 (JP10-266079)	JP	9/3/1999 (9/21/1998)	Hysteresis Input Buffer Joo, Yang-Sung
6188244 (09/159759)	US	2/13/2001 (9/24/1998)	Hysteresis Input Buffer Joo, Yang-Sung
KR10-0266011 (KR10-1997-0050720)	KR	6/20/2000 (10/1/1997)	Hysteresis Input Buffer Oh, Joon-Hwan
DE19757636.2 (DE19757636.2)	DE	10/13/2005 (12/23/1997)	Data Transmission Method For PAM Communication System Yoon, Young-Bin
6269134 (09/119740)	US	7/31/2001 (7/21/1998)	Data Transmission Method And Apparatus In Pulse Amplitude Modulation Communication System Yoon, Young-Bin
KR10-0226504 (KR10-1997-0034248)	KR	7/28/1999 (7/22/1997)	Data Transmitting Method Of Pulse Amplitude Modulation Communication System And Device Thereof Kwon, Gi Jo
(DE19751267.4)	DE	(11/19/1997)	Priority Sequence Determination Method For Data Traffic On Network Oh, Joong-Chan
JP3691654 (JP10-050423)	JP	6/24/2005 (3/3/1998)	Network Traffic Priority Determining Method Oh, Joong-Chan
6314087 (09/053703)	US	11/6/2001 (4/2/1998)	Method For Determining Traffic Priority Order On Network Oh, Joong Chan
KR10-0259082 (KR10-1997-0012213)	KR	3/17/2000 (4/2/1997)	Method For Determining Network Traffic Priority Oh, Jung Chan

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6434112 (09/177511)	US	8/13/2002 (10/23/1998)	Frame Transmission Method Unable to Verify
KR10-0232237 (KR10-1997-0054992)	KR	9/3/1999 (10/25/1997)	Local Area Network Interface Device And Method For The Same Unable to Verify
KR10-0263478 (KR10-1998-0003063)	KR	5/17/2000 (2/4/1998)	Connection Method Of Modem Lee, Seong Gwon
6452963 (09/239532)	US	9/17/2002 (1/29/1999)	Method For Connecting Modems Lee, Seong Kwon

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this 26th day of November 2019.

ASSIGNOR:

Chiao Tung Holdings, LLC

By: _____

Name: Meng-Tien YU

Title: Authorized Person

ASSIGNEE:

Intellectual Ventures Assets 158 LLC

By: _____

Name: Lawrence Froeber

Title: Chief Financial Officer

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Chiao Tung Holdings, LLC, a Delaware limited liability company, having an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Intellectual Ventures Assets 158 LLC, a Delaware limited liability company, having an address at 251 Little Falls Drive, Wilmington, DE 19808 ("***Assignee***"), or its designees, the right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

Patent or Application No.	**Country**	**Grant Date Filing Date**	**Title of Patent and First Named Inventor**
(DE19901185.0)	DE	(1/14/1999)	NAND/NOR gate combination for operation in differential mode Ra, Youn-Wook
KR10-0275948 (KR10-1998-0013204)	KR	9/25/2000 (4/14/1998)	Differential Mode NAND/NOR Gate Ra, Youn-Wook
6225830 (09/290543)	US	5/1/2001 (4/12/1999)	Differential mode logic gate having NAND and NOR portions to produce complementary outputs Ra, Youn-Wook
JP3101812 (JP09-292412)	JP	8/25/2000 (10/24/1997)	Data Transmitter-Receiver And Data Transmission/Reception Method For Serially Transmitting And Receiving Data Cho, Dong Soo
KR10-0198669 (KR10-1996-0048004)	KR	3/2/1999 (10/24/1996)	Apparatus and method for serial interfacing Cho, Dong Soo
6034955 (08/931718)	US	3/7/2000 (9/16/1997)	Single line interface system and method thereof Cho, Dong Soo
DE19719115.0 (DE19719115.0)	DE	7/13/2006 (5/6/1997)	Squelch circuit for removing noise in data signal LYU HYUNG LYUL
(JP09-302073)	JP	(11/4/1997)	RECEPTION SQUELCH CIRCUIT HAVING PULSE WIDTH DETECTING FUNCTION LYU HYUNG LYUL

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6108528 (08/958929)	US	8/22/2000 (10/28/1997)	Receive squelch circuit having function of detecting pulse width Lyu, Hyung Lyul
KR10-0239705 (KR10-1996-0051755)	KR	10/21/1999 (11/4/1996)	Squelch Circuits For Detecting Pulse Width RYU HYUNG-RYUL
DE19727431.5 (DE19727431.5)	DE	2/20/2004 (6/27/1997)	Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
GB2315000 (GB9713710.3)	GB	11/21/2000 (6/27/1997)	A Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
JP3155728 (JP09-168744)	JP	2/2/2001 (6/25/1997)	Synchronous And Asynchronous Decision Method And Device For Viterbi Decoding Signal Baek, Jong Seob
6084925 (08/884685)	US	7/4/2000 (6/27/1997)	Method And Apparatus For Discriminating Synchronous Or Asynchronous States Of Viterbi Decoded Data Baek, Jong Seob
TWI097086 (TW086108935)	TW	10/1/1998 (6/26/1997)	A METHOD AND APPARATUS FOR DISCRIMINATING SYNCHRONOUS OR ASYNCHRONOUS STATES OF VITERBI DECODED DATA Baek, Jong Seob
KR10-0223735 (KR10-1996-0026546)	KR	7/12/1999 (6/29/1996)	Device Of Judging Synchronous / Asynchronous State Of Viterbi Decoding Signal Baek, Jong Seop
JP3194135 (JP09-323121)	JP	6/1/2001 (11/25/1997)	Digital Audio Processor Unable to Verify

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6094490 (08/978474)	US	7/25/2000 (11/25/1997)	Noise Gate Apparatus For Digital Audio Processor Unable to Verify
TWI097354 (TW086103866)	TW	9/21/1998 (3/26/1997)	Noise Gate Apparatus For Digital Audio Processor Unable to Verify
KR10-0179936 (KR10-1996-0058085)	KR	11/28/1998 (11/27/1996)	Noise Gate Device Of Digital Audio Processor Unable to Verify
DE19745780.0 (DE19745780.0)	DE	11/14/2003 (10/16/1997)	Title Not Available Baek, Jong Seob
GB2318710 (GB9721865.5)	GB	4/18/2001 (10/15/1997)	Apparatus And Method For Generating A Decoding Clock Signal In Response To A Period Of Write And Read Clock Signals Baek, Jong Seob
JP3094285 (JP09-299463)	JP	8/4/2000 (10/16/1997)	Decoding Clock Generator By Coding Rate And Its Method Baek, Jong Seob
6134288 (08/953009)	US	10/17/2000 (10/16/1997)	Apparatus And Method For Generating A Decoding Clock Signal In Response To A Period Of Write And Read Clock Signals Baek, Jong Seob
KR10-0233291 (KR10-1996-0046238)	KR	9/10/1999 (10/16/1996)	Restoring Clock Generator According To Coding Ratio And Method Thereof Baek, Jong Seop
DE19822784.1 (DE19822784.1)	DE	2/7/2003 (5/20/1998)	Analog-to-digital converter using interleaved sampling Park, Yong-Pal
(JP10-346399)	JP	(12/7/1998)	Analog / Digital Converter Park, Yong-Pal

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6169504 (09/172075)	US	1/2/2001 (10/14/1998)	Device And Method For Converting Analog Signal To Digital Signal Using Interleaving Sampling Park, Yong-Pal
KR10-0286326 (KR10-1997-0068515)	KR	1/11/2001 (12/13/1997)	Interleaving Sampling Analog / Digital Converter Park, Yong-Pal
KR10-0242462 (KR10-1996-0052656)	KR	11/10/1999 (11/7/1996)	I/O Address Mapping Device Using Indexing Mechanism Ahn, Mun Weon
6079623 (08/965766)	US	6/27/2000 (11/7/1997)	Apparatus for mapping memory PCMCIA cards into I/O window address space to select an internal register and perform read and write operations using an index mechanism Ahn, Mun Weon
(DE19751301.8)	DE	(11/19/1997)	Schmitt-trigger circuit for input buffer Shin, Dong Young
(JP09-332731)	JP	(12/3/1997)	SCHMITT TRIGGER CIRCUIT CAPABLE OF ADJUSTING TRIGGER VOLTAGE Shin, Dong Young
5874844 (08/905716)	US	2/23/1999 (8/4/1997)	SCHMITT TRIGGER CIRCUIT WITH AN ADJUSTABLE TRIGGER VOLTAGE Shin, Dong Young
KR10-0215839 (KR10-1997-0009450)	KR	5/26/1999 (3/20/1997)	SCHMIDT TRIGGER CIRCUIT CAPABLE OF CONTROLLING TRIGGER VOLTAGE Unable to Verify
DE19818020.9 (DE19818020.9)	DE	11/22/2004 (4/22/1998)	Signal compression circuit Kim, Seong-Ryeol
6169808 (09/037175)	US	1/2/2001 (3/9/1998)	Signal compressing circuit Kim, Seong-Ryeol

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
KR10-0275937 (KR10-1997-0046060)	KR	9/25/2000 (9/6/1997)	A CIRCUIT FOR DATA COMPRESSION Unable to Verify
(JP09-236828)	JP	(9/2/1997)	DATA ISOLATING CIRCUIT Shin, Byeong Cheol
6212249 (08/921586)	US	4/3/2001 (9/2/1997)	DATA SEPARATION CIRCUIT AND METHOD Shin, Byeong Cheol
KR10-0205354 (KR10-1996-0037839)	KR	4/2/1999 (9/2/1996)	DATA SEPARATION CIRCUIT Shin, Byeong Cheol
6285789 (09/154094)	US	9/4/2001 (9/16/1998)	Variable length code decoder for MPEG Kim, Young Goan
KR10-0253366 (KR10-1997-0065566)	KR	1/22/2000 (12/3/1997)	Variable length code decoder for MPEG Kim, Young Goan
(JP09-354217)	JP	(12/8/1997)	Fiber Pig Tail For Optical Communication Module Chun, Sung-Hak
KR10-0272265 (KR10-1996-0077822)	KR	8/23/2000 (12/30/1996)	Fiber Pigtail For A Optical Communication Module Chun, Sung Hak
6053641 (08/999150)	US	4/25/2000 (12/29/1997)	Fiber Pigtail For Optical Communication Module Chun, Sung-Hak
KR10-0259590 (KR10-1998-0000287)	KR	3/25/2000 (1/8/1998)	Frequency Detection Circuit Choi, Sang-Shin
TWI115402 (TW087113575)	TW	5/11/2000 (8/18/1998)	Frequency Ddetecting Circuit Choi, Sang-Shin

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6081137 (09/166960)	US	6/27/2000 (10/6/1998)	Frequency Detecting Circuit Choi, Sang-Shin
KR10-0296136 (KR10-1998-0024574)	KR	5/7/2001 (6/27/1998)	Image sensor having test pattern for determining characteristics of color filter Unable to Verify
6088112 (09/344823)	US	7/11/2000 (6/25/1999)	Image Sensor Having Test Patterns For Measuring Characteristics Of Color Filters Unable to Verify
JP3691261 (JP10-316234)	JP	6/24/2005 (11/6/1998)	Data Changeable Device For Variable Length Decoder Ryu, Seung-Chol
6133860 (09/186637)	US	10/17/2000 (11/6/1998)	A VARIABLE LENGTH DECODER WITH ENHANCED ROUTING OF DATA TO MULTIPLEXERS Ryu, Seung-Chol
KR10-0292050 (KR10-1997-0058867)	KR	3/19/2001 (11/8/1997)	Data Simulator Of Variable Length Decoder Kim, Yong Hwan
(DE19840020.9)	DE	(9/2/1998)	Wireless Subscriber Connection Cable System With Patch Antenna Park, Yong-Pal
KR10-0286331 (KR10-1998-0003575)	KR	1/11/2001 (2/7/1998)	Wireless Local Loop System Using Patch Antenna Park, Yong Pal
6163299 (09/244089)	US	12/19/2000 (2/4/1999)	Wireless Local Loop System Using Patch-Type Antenna Park, Yong-Pal
(DE19818021.7)	DE	(4/22/1998)	Input Buffer Circuit With Hysteresis Characteristic Joo, Yang-Sung

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
JP2973115 (JP10-266079)	JP	9/3/1999 (9/21/1998)	Hysteresis Input Buffer Joo, Yang-Sung
6188244 (09/159759)	US	2/13/2001 (9/24/1998)	Hysteresis Input Buffer Joo, Yang-Sung
KR10-0266011 (KR10-1997-0050720)	KR	6/20/2000 (10/1/1997)	Hysteresis Input Buffer Oh, Joon-Hwan
DE19757636.2 (DE19757636.2)	DE	10/13/2005 (12/23/1997)	Data Transmission Method For PAM Communication System Yoon, Young-Bin
6269134 (09/119740)	US	7/31/2001 (7/21/1998)	Data Transmission Method And Apparatus In Pulse Amplitude Modulation Communication System Yoon, Young-Bin
KR10-0226504 (KR10-1997-0034248)	KR	7/28/1999 (7/22/1997)	Data Transmitting Method Of Pulse Amplitude Modulation Communication System And Device Thereof Kwon, Gi Jo
(DE19751267.4)	DE	(11/19/1997)	Priority Sequence Determination Method For Data Traffic On Network Oh, Joong-Chan
JP3691654 (JP10-050423)	JP	6/24/2005 (3/3/1998)	Network Traffic Priority Determining Method Oh, Joong-Chan
6314087 (09/053703)	US	11/6/2001 (4/2/1998)	Method For Determining Traffic Priority Order On Network Oh, Joong Chan
KR10-0259082 (KR10-1997-0012213)	KR	3/17/2000 (4/2/1997)	Method For Determining Network Traffic Priority Oh, Jung Chan

Patent or Application No.	Country	Grant Date Filing Date	Title of Patent and First Named Inventor
6434112 (09/177511)	US	8/13/2002 (10/23/1998)	Frame Transmission Method Unable to Verify
KR10-0232237 (KR10-1997-0054992)	KR	9/3/1999 (10/25/1997)	Local Area Network Interface Device And Method For The Same Unable to Verify
KR10-0263478 (KR10-1998-0003063)	KR	5/17/2000 (2/4/1998)	Connection Method Of Modem Lee, Seong Gwon
6452963 (09/239532)	US	9/17/2002 (1/29/1999)	Method For Connecting Modems Lee, Seong Kwon

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this 20th day of November 2019.

ASSIGNOR:

Chiao Tung Holdings, LLC

By: _____

Name: _____

Title: _____

ASSIGNEE:

Intellectual Ventures Assets 158 LLC

By: _____

Name: Lawrence Froeber

Title: Chief Financial Officer