PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT5960963

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
POLARIS INNOVATIONS LIMITED	11/30/2019

RECEIVING PARTY DATA

Name:	CHANGXIN MEMORY TECHNOLOGIES, INC
Street Address:	ROOM 630, HAIHENG BUILDING, NO. 6, CUIWEI ROAD
Internal Address:	ECONOMIC AND TECHNOLOGICAL DEVELOPMENT ZONE
City:	HEFEI, ANHUI
State/Country:	CHINA
Postal Code:	230000

PROPERTY NUMBERS Total: 83

Property Type	Number
Patent Number:	8120182
Patent Number:	8178927
Patent Number:	8158485
Patent Number:	7457913
Patent Number:	7415569
Patent Number:	7457177
Patent Number:	7349253
Patent Number:	7362633
Patent Number:	7321240
Patent Number:	7333383
Patent Number:	7299388
Patent Number:	7297983
Patent Number:	7297468
Patent Number:	7308628
Patent Number:	7005240
Patent Number:	6898747
Patent Number:	7126326
Patent Number:	7421667
Patent Number:	7396749

Property Type	Number
Patent Number:	6909152
Patent Number:	6813748
Patent Number:	6774688
Patent Number:	6858447
Patent Number:	6541387
Patent Number:	6720785
Patent Number:	6531377
Patent Number:	6496423
Patent Number:	6545927
Patent Number:	8241989
Patent Number:	7564114
Patent Number:	7595262
Patent Number:	7477717
Patent Number:	7291560
Patent Number:	7312492
Patent Number:	7368385
Patent Number:	8003538
Patent Number:	7316962
Patent Number:	7342291
Patent Number:	6849365
Patent Number:	6716720
Patent Number:	7452821
Patent Number:	7368390
Patent Number:	6787801
Patent Number:	6559547
Patent Number:	6571383
Patent Number:	8918597
Patent Number:	7937631
Patent Number:	7888948
Patent Number:	7263638
Patent Number:	7184337
Patent Number:	7154793
Patent Number:	7171327
Patent Number:	6744304
Patent Number:	6797613
Patent Number:	6919269
Patent Number:	6756314
Patent Number:	6864188

Property Type	Number
Patent Number:	6708405
Patent Number:	6596625
Patent Number:	6456553
Patent Number:	6429503
Patent Number:	6730607
Patent Number:	6680503
Patent Number:	6483166
Patent Number:	6440753
Patent Number:	6479396
Patent Number:	6728902
Patent Number:	6413886
Patent Number:	7835197
Patent Number:	7872931
Patent Number:	7248067
Patent Number:	7193883
Patent Number:	6501150
Patent Number:	6545526
Patent Number:	6603699
Patent Number:	6704676
Patent Number:	6768695
Patent Number:	6687170
Patent Number:	6465282
Patent Number:	6642602
Patent Number:	6759894
Patent Number:	6813200
Patent Number:	7126204

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	53EH
NAME OF SUBMITTER:	HUANYONG GAO

SIGNATURE:	/Huanyong Gao/
DATE SIGNED:	02/12/2020

Total Attachments: 5
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Exhibit B
Form of Assignment Agreement

THIS ASSIGNMENT is made as of November 30, 2019 (the "Closing Date") by and between ChangXin Memory Technologies, Inc. a corporation duly organized and existing under the laws of the People's Republic of China ("Purchaser") and Polaris Innovations Limited, an Irish company ("Seller").

WHEREAS in this Assignment, "Patents" means the United States and non-United States patents and patent applications listed on Schedule A to this Assignment; and

AND WHEREAS Seller owns all interest, right, title, property and benefit in and to each of the Patents and has agreed to sell, assign, transfer and convey all interest, right, title, property and benefit in and to each of the Patents to Purchaser;

NOW, THEREFORE, in consideration of good and valuable consideration, the receipt and sufficiency of which are hereby expressly acknowledged, Seller hereby sells, assigns, transfers and conveys to Purchaser (a) all right, title and interest to each Patent, (b) the exclusive rights to make, use, offer for sale, sell or import products and services that infringe any Patents and to practice each Patent, (c) the exclusive right to exclude other persons from practicing any of the Patents and the exclusive right to collect any damages for past, current and future infringement Seller may have as at the Closing Date in respect of each Patent, (d) any right Seller may have to sue for past, current and future infringement of each Patent and (e) any right Seller may have to seek equitable or other relief (including a preliminary or permanent injunction or other exclusionary order of any type) with respect to any product, service or process that may or does infringe any Patent.

IN WITNESS WHEREOF, Seller has caused this Assignment to be executed effective as of the date first written above by its duly authorized officer.

Signed: _____
Name: Michael Wadesen
Title: CEO & President

Country of CANADA)
City of OTTAWA)
)

On this 10th January, 2020, before me appeared Michael Wadesen, to me personally known who, being duly sworn, did depose and say that he is the CEO & President of Seller as named in the Assignment above and that such Assignment was signed on behalf of Seller, and such person acknowledged the Assignment to be the free and authorized act and deed of Seller.

_____
Notary Public
My commission expires: N/A

Schedule A
Certain Patents

Country	Title	Patent #
UNITED STATES	INTEGRATED CIRCUIT COMPRISING CONDUCTIVE LINES AND CONTACT STRUCTURES AND METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT	8,120,182
UNITED STATES	Integrated Circuits Having a Contact Structure Having an Elongate Structure and Methods for Manufacturing the Same	8,178,927
UNITED STATES	INTEGRATED CIRCUIT DEVICE HAVING OPENINGS IN A LAYERED STRUCTURE	8,158,485
UNITED STATES	Finding a Data Pattern in a Memory	7,457,913
UNITED STATES	Memory Including a Write Training Block	7,415,569
UNITED STATES	Random Access Memory Including Circuit to Compress Comparison Results	7,457,177
UNITED STATES	MEMORY DEVICE AND METHOD FOR TESTING MEMORY DEVICES WITH REPAIRABLE REDUNDANCY	7,349,253
UNITED STATES	Parallel Read for Front End Compression Mode	7,362,633
UNITED STATES	DRIVER CIRCUIT FOR BINARY SIGNALS	7,321,240
UNITED STATES	FUSE RESISTANCE READ-OUT CIRCUIT	7,333,383
UNITED STATES	Method and Apparatus for Selectively Accessing and Configuring Individual Chips of a Semi-Conductor Wafer	7,299,388
UNITED STATES	METHOD FOR FABRICATING AN INTEGRATED CIRCUIT ON A SEMICONDUCTOR SUBSTRATE	7,297,983
UNITED STATES	METHOD FOR FORMING A STRUCTURE ELEMENT ON A WAFER BY MEANS OF A MASK AND A TRIMMING MASK ASSIGNED HERETO	7,297,468
UNITED STATES	INPUT SWITCHING ARRANGEMENT FOR A SEMICONDUCTOR CIRCUIT AND TEST METHOD FOR UNIDIRECTIONAL INPUT DRIVERS IN SEMICONDUCTOR CIRCUITS	7,308,628
UNITED STATES	METHOD FOR FORMING A HARD MASK IN A LAYER ON A PLANAR DEVICE	7,005,240
UNITED STATES	Method for testing circuit units to be tested with increased data compression for burn-in	6,898,747
UNITED STATES	SEMICONDUCTOR DEVICE TESTING APPARATUS, SEMICONDUCTOR DEVICE TESTING SYSTEM, AND SEMICONDUCTOR DEVICE TESTING METHOD FOR MEASURING AND TRIMMING THE OUTPUT IMPEDANCE OF DRIVER DEVICES	7,126,326
UNITED STATES	SYSTEM AND METHOD FOR ENABLING A VENDOR MODE ON AN INTEGRATED CIRCUIT	7,421,667
UNITED STATES	METHOD FOR CONTACTING PARTS OF A COMPONENT INTEGRATED INTO A SEMICONDUCTOR SUBSTRATE	7,396,749
UNITED STATES	HIGH DENSITY DRAM WITH REDUCED PERIPHERAL DEVICE AREA AND METHOD OF MANUFACTURE	6,909,152
UNITED STATES	SYSTEM AND METHOD FOR ENABLING A VENDOR MODE ON AN INTEGRATED CIRCUIT	6,813,748
UNITED STATES	CIRCUIT FOR SYNCHRONIZING SIGNALS DURING THE EXCHANGE OF INFORMATION BETWEEN CIRCUITS	6,774,688
UNITED STATES	METHOD FOR TESTING SEMICONDUCTOR CHIPS	6,858,447
UNITED STATES	PROCESS FOR THE IMPLEMENTATION OF A HARDMASK	6,541,387
UNITED STATES	INTEGRATED CIRCUIT WITH TEST MODE, AND TEST CONFIGURATION FOR TESTING AN INTEGRATED CIRCUIT	6,720,785

UNITED STATES	METHOD FOR HIGH ASPECT RATIO GAP FILL USING SEQUENTIAL HDP-CVD	6,531,377
UNITED STATES	CHIP ID REGISTER CONFIGURATION	6,496,423
UNITED STATES	INTEGRATED SEMICONDUCTOR CIRCUIT, IN PARTICULAR A SEMICONDUCTOR MEMORY CONFIGURATION, AND METHOD FOR ITS OPERATION	6,545,927
UNITED STATES	Integrated circuit with stacked devices	8,241,989
UNITED STATES	Semiconductor Devices and Methods of Manufacture Thereof	7,564,114
UNITED STATES	MANUFACTURING METHOD FOR AN INTEGRATED SEMICONDUCTOR STRUCTURE	7,595,262
UNITED STATES	INPUT RECEIVER CIRCUIT	7,477,717
UNITED STATES	Method of Producing Pitch Fractionizations in Semiconductor Technology	7,291,560
UNITED STATES	METHOD FOR FABRICATING A DRAM MEMORY CELL ARRANGEMENT HAVING FIN FIELD EFFECT TRANSISTORS AND DRAM MEMORY CELL	7,312,492
UNITED STATES	METHOD OF PRODUCING A STRUCTURE ON THE SURFACE OF A SUBSTRATE	7,368,385
UNITED STATES	METHOD OF PRODUCING A STRUCTURE ON THE SURFACE OF A SUBSTRATE	8,003,538
UNITED STATES	HIGH DIELECTRIC CONSTANT MATERIALS	7,316,962
UNITED STATES	STANDBY CURRENT REDUCTION OVER A PROCESS WINDOW WITH A TRIMMABLE WELL BIAS	7,342,291
UNITED STATES	REFLECTION MASK FOR EUV-LITHOGRAPHY AND METHOD FOR FABRICATING THE REFLECTION MASK	6,849,365
UNITED STATES	METHOD FOR FILLING DEPRESSIONS ON A SEMICONDUCTOR WAFER	6,716,720
UNITED STATES	METHOD FOR THE FORMATION OF CONTACT HOLES FOR A NUMBER OF CONTACT REGIONS FOR COMPONENTS INTEGRATED IN A SUBSTRATE	7,452,821
UNITED STATES	PHOTOLITHOGRAPHIC PATTERNING PROCESS USING A CARBON HARD MASK LAYER OF DIAMOND-LIKE HARDNESS PRODUCED BY A PLASMA-ENHANCED DEPOSITION PROCESS	7,368,390
UNITED STATES	WAFER WITH ADDITIONAL CIRCUIT PARTS IN THE KERF AREA FOR TESTING INTEGRATED CIRCUITS ON THE WAFER	6,787,801
UNITED STATES	PATTERNING OF CONTENT AREAS IN MULTILAYER METALIZATION CONFIGURATIONS OF SEMICONDUCTOR COMPONENTS	6,559,547
UNITED STATES	SEMICONDUCTOR DEVICE FABRICATION USING A PHOTOMASK DESIGNED USING MODELING AND EMPIRICAL TESTING	6,571,383
UNITED STATES	DIGITAL DATA INVERSION FLAG GENERATOR CIRCUIT	8,918,597
UNITED STATES	Method for self-test and self-repair in a Multi-Chip Package environment	7,937,631
UNITED STATES	Controlling an analog signal in an integrated circuit	7,888,948
UNITED STATES	MEMORY HAVING TEST CIRCUIT	7,263,638
UNITED STATES	METHOD FOR TESTING AN INTEGRATED SEMICONDUCTOR MEMORY	7,184,337
UNITED STATES	INTEGRATED MEMORY AND METHOD FOR FUNCTIONAL TESTING OF THE INTEGRATED MEMORY	7,154,795
UNITED STATES	TEMPERATURE SENSOR SCHEME	7,171,327

UNITED STATES	ELECTRONIC CIRCUIT FOR GENERATING AN OUTPUT VOLTAGE HAVING A DEFINED TEMPERATURE DEPENDENCE	6,744,304
UNITED STATES	PROCESS FOR DEPOSITING WSIX LAYERS ON A HIGH TOPOGRAPHY WITH A DEFINED STOICHIOMETRY	6,797,613
UNITED STATES	PRODUCTION METHOD FOR A SEMICONDUCTOR COMPONENT	6,919,269
GERMANY	PRODUCTION METHOD FOR A SEMICONDUCTOR COMPONENT	50202631.6
UNITED STATES	METHOD FOR ETCHING A HARD MASK LAYER AND A METAL LAYER	6,756,314
UNITED STATES	SEMICONDUCTOR CONFIGURATION AND PROCESS FOR ETCHING A LAYER OF THE SEMICONDUCTOR CONFIGURATION USING A SILICON-CONTAINING ETCHING MASK	6,864,188
UNITED STATES	METHOD FOR PRODUCING AN ELECTRICALLY CONDUCTING CONNECTION	6,708,405
UNITED STATES	METHOD AND DEVICE FOR PRODUCING A METAL/METAL CONTACT IN A MULTILAYER METALLIZATION OF AN INTEGRATED CIRCUIT	6,596,625
UNITED STATES	CIRCUIT CONFIGURATION FOR SWITCHING OVER A RECEIVER CIRCUIT IN PARTICULAR IN DRAM MEMORIES AND DRAM MEMORY HAVING THE CIRCUIT CONFIGURATION	6,456,553
UNITED STATES	CONNECTION ELEMENT	6,429,503
UNITED STATES	METHOD FOR FABRICATING A BARRIER LAYER	6,730,607
UNITED STATES	FIELD-EFFECT TRANSISTOR STRUCTURE WITH AN INSULATED GATE	6,680,503
UNITED STATES	SEMICONDUCTOR CONFIGURATION HAVING AN OPTICAL FUSE	6,483,166
UNITED STATES	METAL HARD MASK FOR ILD RIE PROCESSING OF SEMICONDUCTOR MEMORY DEVICES TO PREVENT OXIDATION OF CONDUCTIVE LINES	6,440,753
UNITED STATES	DRY POLYMER AND OXIDE VEIL REMOVAL FOR POST ETCH CLEANING	6,479,396
UNITED STATES	INTEGRATED CIRCUIT HAVING A SELF-TEST DEVICE FOR CARRYING OUT A SELF-TEST OF THE INTEGRATED CIRCUIT	6,728,902
UNITED STATES	METHOD FOR FABRICATING A MICROTECHNICAL STRUCTURE	6,413,886
UNITED STATES	Integrated semiconductor memory with generation of data	7,835,197
UNITED STATES	Integrated Circuit with Control Circuit for Performing Retention Test	7,872,931
UNITED STATES	SEMICONDUCTOR DEVICE WITH TEST CIRCUIT DISCONNECTED FROM POWER SUPPLY CONNECTION	7,248,067
UNITED STATES	INPUT RETURN PATH BASED ON VDDQ/VSSQ	7,193,883

UNITED STATES	FUSE CONFIGURATION FOR A SEMICONDUCTOR APPARATUS	6,501,150
UNITED STATES	FUSE CIRCUIT CONFIGURATION	6,545,526
UNITED STATES	CONFIGURATION FOR FUSE INITIALIZATION	6,603,699
UNITED STATES	METHOD AND CIRCUIT CONFIGURATION FOR IDENTIFYING AN OPERATING PROPERTY OF AN INTEGRATED CIRCUIT	6,704,676
UNITED STATES	CIRCUIT CONFIGURATION FOR DRIVING A PROGRAMMABLE LINK	6,768,695
UNITED STATES	SYSTEM AND METHOD FOR STORING PARITY INFORMATION IN FUSES	6,687,170
UNITED STATES	METHOD OF FORMING A SELF-ALIGNED ANTIFUSE LINK	6,465,282
UNITED STATES	Self-Terminating Blow Process of Electrical Anti-Fuses	6,642,602
UNITED STATES	METHOD AND CIRCUIT FOR CONTROLLING FUSE BLOW	6,759,894
UNITED STATES	CIRCUIT CONFIGURATION FOR READING OUT A PROGRAMMABLE LINK	6,813,200
UNITED STATES	INTEGRATED SEMICONDUCTOR CIRCUIT WITH AN ELECTRICALLY PROGRAMMABLE SWITCHING ELEMENT	7,126,204