PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5989784

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
INVECAS, INC.	02/13/2020

RECEIVING PARTY DATA

Name:	SYNOPSYS, INC.
Street Address:	690 EAST MIDDLEFIELD ROAD
City:	MOUNTAIN VIEW
State/Country:	CALIFORNIA
Postal Code:	94043

PROPERTY NUMBERS Total: 42

Property Type	Number
Patent Number:	8669792
Patent Number:	8643516
Patent Number:	9286260
Patent Number:	9337846
Patent Number:	8952737
Patent Number:	9564905
Patent Number:	9948310
Patent Number:	9467149
Patent Number:	9349421
Patent Number:	9444463
Patent Number:	9946620
Patent Number:	9799413
Patent Number:	9620179
Patent Number:	9564183
Patent Number:	9564184
Patent Number:	9865361
Patent Number:	9954538
Patent Number:	10014866
Patent Number:	9715907
Patent Number:	9613700

Property Type	Number
Patent Number:	9564180
Patent Number:	9716492
Patent Number:	9971975
Patent Number:	10094859
Patent Number:	10061340
Application Number:	15432208
Application Number:	15654595
Application Number:	15698289
Application Number:	15795144
Application Number:	15895915
Application Number:	15989081
Application Number:	15904139
Application Number:	16059477
Application Number:	16398644
Application Number:	16268206
Application Number:	16374666
Application Number:	15573907
Application Number:	15573917
Application Number:	15554000
Application Number:	15573921
Application Number:	15577340
Application Number:	16423554

CORRESPONDENCE DATA

Fax Number: (650)938-5200

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 6503357607
Email: dchevalier@fenwick.com
Correspondent Name: RAJIV P. PATEL
Address Line 1: 801 CALIFORNIA STREET
Address Line 4: MOUNTAIN VIEW, CALIFORNIA 94041

ATTORNEY DOCKET NUMBER:	22524-01000
NAME OF SUBMITTER:	RAJIV P. PATEL
SIGNATURE:	/RAJIV P. PATEL/
DATE SIGNED:	02/29/2020

Total Attachments: 7
source=01000 Invectas to Synopsys (Ipala) Patent Assignment Agreement EXECUTED#page1.tif
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PATENT ASSIGNMENT

This **PATENT ASSIGNMENT** (this "**Assignment**") is made effective as of February 13, 2020 (the "**Effective Date**") by and between **INVECAS, INC.**, a Delaware corporation (the "**Assignor**"), and **SYNOPSYS, INC.**, a Delaware corporation ("**Assignee**").

WHEREAS, Assignor is the owner of the entire right, title, interest of certain patents and patent applications identified on Schedule 1 attached hereto (the "**Patents**"); and

WHEREAS, Assignee desires to acquire the Patents, and Assignor desires to sell, all of Assignor's right, title and interest in and to the Patents and Patent Rights (as defined below) to Assignee, pursuant to that certain Asset Purchase Agreement, dated as of December 24, 2020 (the "**Purchase Agreement**"), by and between Assignor and Assignee;

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties agree as follows:

1. Assignor hereby irrevocably sells, assigns, transfers, and conveys to Assignee all right, title, and interest in and to any and all of the following (collectively, the "**Patent Rights**"):

(a) the Patents, together with any patent issuing on any such patent application, including any rights of priority in or to any of the foregoing patents or patent applications;

(b) each patent and patent application that derives priority from any of the patents or patent applications described in clause "(a)" above, including all extensions, renewals, reissues, reexaminations, divisionals, substitutions, provisionals, continuations, continuations-in-part, conversions, prolongations, continued examinations, continued prosecution applications, and domestic and foreign counterparts that derive priority from any of the patents or patent applications described in clause "(a)" above, and each patent issuing on any of the foregoing (each patent and patent application described in clauses "(a)" through and including "(b)" above, collectively, the "**Assigned Patents**");

(c) all rights to apply in any and all jurisdictions anywhere in the world for patents, certificates of inventions, utility models, or other governmental grants with respect to each Assigned Patent, including the right to apply for patents pursuant to any convention, treaty, agreement or understanding;

(d) to the extent they exist, any and all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Assigned Patents in any of the foregoing clauses "(a)" through and including "(c)" above, including all causes of action and other enforcement rights for (i) damages, (ii) injunctive relief, (iii) any other remedies of any kind (in each of the cases in clauses "(i)", "(ii)", and "(iii)" of this clause "(d)" for past, current, and future infringement), and (iv) all rights to collect royalties and other payments under or on account of each of the Assigned Patents and items in any of the foregoing clauses "(a)" through and including "(c)" above.

2. Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

3. Assignor hereby authorizes and requests the attorney or agent of record to insert on this Assignment any further identification that may be necessary or desirable in order to comply with the rules of the respective patent office or governmental agency in each jurisdiction for recordation or other official recognition.

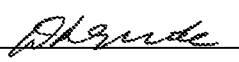
4. From and after the Effective Date, Assignor shall cooperate with Assignee and Assignee's representatives, and shall execute and deliver such documents and take such other actions as Assignee may reasonably request, to cause to be conveyed to Assignee and its successors or assigns all of the rights, titles and interests intended to be conveyed to Assignee under this Assignment. Assignor hereby irrevocably nominates, constitutes and appoints Assignee as the true and lawful attorney-in-fact of Assignor (with full power of substitution) effective as of the Effective Date, and hereby authorizes Assignee, in the name of and on behalf of Assignor, to execute, deliver, acknowledge, certify, file and record any document and to take any other action (on or at any time after the date of this Assignment) that Assignee may deem appropriate for the purpose of collecting, asserting, enforcing or perfecting any claim, right or interest in or to any of the Patent Rights. The power of attorney referred to in the preceding sentence is and shall be coupled with an interest and shall be irrevocable, and shall survive the dissolution or insolvency of Assignor.

5. The terms and conditions of this Assignment will inure to the benefit of Assignee and Assignee's successors and assigns of the Patent Rights and other rights set forth above.

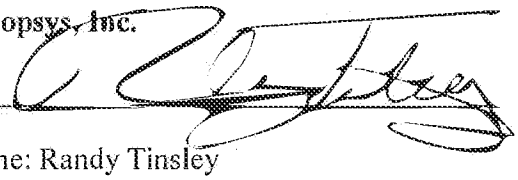
6. This Assignment shall be construed and interpreted in accordance with the Purchase Agreement. Nothing in this Assignment shall, or shall be deemed to, modify or otherwise affect any provisions of the Purchase Agreement or affect or modify any of the rights or obligations of the parties under the Purchase Agreement. In the event of any conflict between the provisions hereof and the provisions of the Purchase Agreement, the provisions of the Purchase Agreement shall govern and control. Any rule of construction to the effect that ambiguities are to be resolved against the drafting party will not be applied in the construction or interpretation of this Assignment. The words "include", "including" and variations thereof will be deemed to be followed by the words "without limitation". The use of "or" will not be deemed to be exclusive. This Assignment may be executed in counterparts, each of which when executed will be deemed to be an original but all of which taken together will constitute one and the same agreement.

[*Signature page follows*]

IN WITNESS WHEREOF, intending to be legally bound, the parties through their duly authorized representatives have executed this Assignment as of the Effective Date.

Invecas, Inc.	**Synopsys, Inc.**
By: 	By: _____
Name: Dasaradha Gude	Name: _____
Title: Chief Executive Officer	Title: _____
Date: February 13, 2020	Date: _____

IN WITNESS WHEREOF, intending to be legally bound, the parties through their duly authorized representatives have executed this Assignment as of the Effective Date.

Invecas, Inc.	**Synopsys, Inc.**
By:_____	By: 
Name:_____	Name: Randy Tinsley
Title:_____	Title: VP, Strategic and Corporate Business Development
Date:_____	Date: February 13, 2020

Schedule 1

Patents and Patent Applications

No.	Application Number	Title	Application Status	Filing Date	Patent Number
1	13/667,290	A Voltage Mode Driver	Issued	11/2/2012	**8,669,792**
2	13/669,137	Parallel-to-Serial Converter	Issued	11/5/2012	**8,643,516**
3	13/851,767	Serial-to-Parallel Converter	Issued	3/27/2013	**9,286,260**
4	13/922,193	Methods and Systems for Receiver Detection on a PCI-Express Bus	Issued	6/19/2013	**9,337,846**
5	14/065,754	Methods and Systems for Calibration of a Delay Locked Loop	Issued	10/29/13	**8,952,737**
6	14/066,583	Methods and Systems for Clocking a Physical Layer Interface	Issued	10/29/13	**9,564,905**
7	15/145,735	Methods and Systems for Clocking a Physical Layer Interface	Issued	5/3/2016	**9,948,310**
8	14/170,064	Methods and Systems for Distributing Clock and Reset Signals	Issued	1/31/2014	**9,467,149**
9	14/171,646	A Memory Interface	Issued	2/3/2014	**9,349,421**
10	14/608,137	Voltage Level Shifter	Issued	1/28/2015	**9,444,463**
11	15/012,707	A Memory Built-In Self Test System	Issued	2/1/2016	**9,946,620**
12	15/012,721	Multi-Domain Fuse Management	Issued	2/1/2016	**9,799,413**
13	14/934,021	A Sense Amplifier	Issued	11/5/2015	**9,620,179**
14	14/934,050	A Sense Amplifier having a Timing Circuit for a Presearch and a Main Search	Issued	11/5/2015	**9,564,183**
15	14/939,782	A Sense Amplifier for Single-ended Sensing	Issued	11/12/15	**9,564,184**

16	15/140,242	Diagnostics for a Memory Device	Issued	4/27/2016	**9,865,361**
17	15/192,594	Clock Alignment Scheme for Data Macros of DDR PHY	Issued	6/24/2016	**9,954,538**
18	15/707,205	Clock Alignment Scheme for Data Macros of DDR PHY	Issued	9/18/2017	**10,014,866**
19	15/150,334	Optimal Data Eye for Improved Vref Margin	Issued	5/9/2016	**9,715,907**
20	15/183,591	TCAM Field Enable Logic	Issued	6/15/2016	**9,613,700**
21	15/192,697	Deep-Sleep Wake Up for a Memory Device	Issued	6/24/2016	**9,564,180**
22	15/241,664	Method and Circuit for Duty Cycle Detection	Issued	8/19/2016	**9,716,492**
23	15/432,208	Temperature Sensing for Integrated Circuits	Filed	2/14/2017	
24	15/467,775	Optimal Data Eye for Improved Vref Margin	Issued	3/23/2017	**9,971,975**
25	15/654,595	Duty Cycle Detection	Filed	7/19/2017	
26	15/698,289	Voltmeter	Filed	9/7/17	
27	15/654,598	Voltage Detector	Issued	7/19/2017	**10,094,859**
28	15/795,144	Multi-Protocol Receiver	Filed	10/26/17	
29	15/879,355	Bandgap Reference Voltage Generator	Issued	1/24/2018	**10,061,340**
30	15/895,915	A Receiver For Handling High Speed Transmissions	Filed	2/13/2018	
31	15/989,081	DAC	Filed	5/24/2018	
32	15/904,139	PWM Modulation	Filed	2/23/2018	

33	16/059,477	Memory Bypass Function For A Memory	Filed	8/9/2018	
34	16/398,644	Method and Apparatus for Operating A Programmable Clock	Filed	4/30/2019	
35	16/268,206	Method and Apparatus of Operating Synchronizing High-Speed Clock Dividers to Correct Clock Skew	Filed	2/5/2019	
36	16/374,666	Method and Apparatus for Memory Clock Level-Shifter with No Performance Overhead	Filed	4/2/2019	
37	15/573,907	Asynchronous Clock Gating Circuit	Filed	11/14/2017	
38	15/573,917	Method for Cycle Accurate Data Transfer in a Skewed Synchronous Clock Domain	Filed	11/14/2017	
39	15/554,000	A System and Method for Multi-Cycle Write Leveling	Filed	08/27/2017	
40	15/573,921	A Method for Calibrating the Read Latency of a DDR DRAM Module	Filed	11/14/2017	
41	15/577,340	System and Method for Controlling Phase Alignment of Clock Signals	Filed	11/27/2017	
42	16/423,554	Method and Apparatus for Memory Noise-Free Wake-up Protocol from Power-Down	Filed	05/28/2019	