

<b>PATENT ASSIGNMENT COVER SHEET</b>
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Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT6173591

<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	RELEASE OF SECURITY INTEREST
<b>CONVEYING PARTY DATA</b>	
<b>Name</b>	<b>Execution Date</b>
CRESTLINE DIRECT FINANCE, L.P.	06/24/2020
<b>RECEIVING PARTY DATA</b>	
<b>Name:</b>	EMPIRE TECHNOLOGY DEVELOPMENT LLC
<b>Street Address:</b>	C/O ALLIED INVENTORS, LLC
<b>Internal Address:</b>	520 PIKE STREET, SUITE 1520
<b>City:</b>	SEATTLE
<b>State/Country:</b>	WASHINGTON
<b>Postal Code:</b>	98101
<b>PROPERTY NUMBERS Total: 36</b>	
<b>Property Type</b>	<b>Number</b>
Patent Number:	9940170
Patent Number:	9405691
Patent Number:	9785568
Patent Number:	9811469
Patent Number:	8260996
Patent Number:	8321614
Patent Number:	9569270
Patent Number:	9189282
Patent Number:	8881157
Patent Number:	8131970
Patent Number:	8244982
Patent Number:	8195888
Patent Number:	8244986
Patent Number:	8407426
Patent Number:	8667227
Patent Number:	8874855
Patent Number:	8751854
Patent Number:	9519305
Patent Number:	8234431

PATENT

Property Type	Number
Patent Number:	8874849
Patent Number:	9336146
Patent Number:	9760486
Patent Number:	9047194
Patent Number:	9836514
Patent Number:	9053057
Patent Number:	9251072
Patent Number:	8990828
Patent Number:	9471381
Patent Number:	9158689
Patent Number:	9275696
Patent Number:	9588900
Patent Number:	10049045
Patent Number:	9473426
Patent Number:	9632832
Patent Number:	10289452
Patent Number:	7996595

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**NAME OF SUBMITTER:** LAURA TREMONT

**SIGNATURE:** /Laura Tremont/

**DATE SIGNED:** 06/26/2020

**Total Attachments: 3**

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**NOTICE OF RELEASE OF SECURITY INTEREST IN PATENTS**

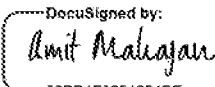
Dated as of June 24, 2020

The lien and security interest evidenced by that certain Patent Security Agreement, dated as of December 28, 2018, executed by, *inter alia*, EMPIRE TECHNOLOGY DEVELOPMENT LLC, a Delaware limited liability company (the "Grantor"), in favor of CRESTLINE DIRECT FINANCE, L.P., as administrative agent (the "Agent"), which was duly recorded on January 29, 2019, at Reel 048373, Frame 0217 in the United States Patent and Trademark Office, and any other right, title or interest granted to the Agent solely in the patents set forth on Schedule 1 attached hereto is hereby terminated, cancelled and released, without representation or warranty, and the Agent hereby re-assigns to the Grantor any right, title or interest it may have in or to any of the patents set forth on Schedule 1.

**CRESTLINE DIRECT FINANCE, L.P.,**  
as Agent

By: Crestline Direct Finance (GP), L.L.C., its general partner

By: Crestline Investors, Inc., its managing member

By:   
Name: Amit Mahajan  
Title: Managing Director

SCHEDULE 1

Patent Registrations

<b>Application Number</b>	<b>Publication Number</b>	<b>Patent Number</b>	<b>Country</b>	<b>Title</b>
13/978,949	US20140181837	9,940,170	United States of America	Dynamically managing distribution of data and computation across cores for sequential programs
14/369,913	US20150242322	9,405,691	United States of America	Locating cached data in a multi-core processor
14/715,114	US20150331804	9,785,568	United States of America	Cache lookup bypass in multi-level cache systems
14/407,761	US20160283386	9,811,469	United States of America	Sequential access of cache data
12/429,580	US20100274941	8,260,996	United States of America	Interrupt Optimization for Multiprocessors
12/429,539	US20100274879	8,321,614	United States of America	Dynamic Scheduling Interrupt Controller for Multiprocessors
12/557,985	US20110066828	9,569,270	United States of America	Mapping thread phases onto heterogeneous cores based on execution characteristics and cache line eviction counts
12/427,602	US20100268912	9,189,282	United States of America	Thread-to-core mapping based on thread deadline, thread demand, and hardware characteristics data collected by a performance counter
12/557,971	US20110067029	8,881,157	United States of America	Allocating threads to cores based on threads falling behind thread completion target deadline
12/427,609	US20100268889	8,131,970	United States of America	Compiler based cache allocation
12/545,625	US20110047333	8,244,982	United States of America	Allocating processor cores with cache memory associativity
12/408,075	US20100241811	8,195,888	United States of America	Multiprocessor cache prefetch with off-chip bandwidth allocation
12/649,659	US20110161346	8,244,986	United States of America	Data storage and access in multi-core processor architectures
13/410,526	US20120166735	8,407,426	United States of America	Data storage and access in multi-core processor architectures
12/644,658	US20110153946	8,667,227	United States of America	Domain based cache coherence protocol
12/648,092	US20110161596	8,874,855	United States of America	Directory-based coherence caching
12/642,871	US20110154089	8,751,854	United States of America	Processor core clock rate selection

Application Number	Publication Number	Patent Number	Country	Title
14/294,146	US20140281657	9,519,305	United States of America	Processor core clock rate selection
12/578,270	US20110087815	8,234,431	United States of America	Interrupt Masking for Multi-Core Processors
13/498,071	US20120317361	8,874,849	United States of America	Sectored cache with a tag structure capable of tracking sectors of data stored for a particular cache way
13/319,159	US20120173819	9,336,146	United States of America	Accelerating cache state transfer on a directory-based multicore architecture
15/080,605	US20160210229	9,760,486	United States of America	Accelerating cache state transfer on a directory-based multicore architecture
13/818,485	US20140223104	9,047,194	United States of America	Virtual cache directory in multi-processor architectures
13/502,312	US20130117227	9,836,514	United States of America	Cache based key-value store mapping and replication
13/877,422	US20140082297	9,053,057	United States of America	Cache coherence directory in multi-processor architectures
14/687,452	US20150220437	9,251,072	United States of America	Cache coherence directory in multi-processor architectures
13/812,400	US20140059560	8,990,828	United States of America	Resource allocation in multi-core architectures
14/657,716	US20150186186	9,471,381	United States of America	Resource allocation in multi-core architectures
13/982,607	US20140229680	9,158,689	United States of America	Aggregating cache eviction notifications to a directory
13/812,967	US20140032829	9,275,696	United States of America	Energy conservation in a multicore chip
13/989,798	US20140032843	9,588,900	United States of America	Management of chip multiprocessor cooperative caching based on eviction rate
15/450,020	US20170177480	10,049,045	United States of America	Management of chip multiprocessor cooperative caching based on eviction rate
14/005,520	US20140286179	9,473,426	United States of America	Hybrid routers in multicore architectures
14/758,404	US20160253212	9,632,832	United States of America	Thread and data assignment in multi-core processors based on cache miss data
15/495,126	US20170228259	10,289,452	United States of America	Thread and data assignment in multi-core processors based on cache miss data
12/423,368	US20100262742	7,996,595	United States of America	Interrupt Arbitration for Multiprocessors

**PATENT**

**RECORDED: 06/26/2020**

**REEL: 053047 FRAME: 0868**