PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
WESTERN DIGITAL TECHNOLOGIES, INC.	05/11/2020

RECEIVING PARTY DATA

Name:	JPMORGAN CHASE BANK, N.A., AS AGENT
Street Address:	IL1-1145/54/63, P.O. BOX 6026
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60680

PROPERTY NUMBERS Total: 163

Property Type	Number
Patent Number:	10636442
Patent Number:	10553241
Application Number:	16780281
Application Number:	16780216
Application Number:	16781885
Application Number:	16781194
Application Number:	16781216
Application Number:	16781717
Application Number:	16781688
Application Number:	16781225
Application Number:	16783057
Application Number:	16784077
Application Number:	16786889
Application Number:	16787482
Application Number:	16787859
Application Number:	16788117
Application Number:	62975661
Application Number:	16792060
Application Number:	16791759
Application Number:	16791560

Property Type	Number
Application Number:	16791238
Application Number:	16792010
Application Number:	16794079
Application Number:	16794100
Application Number:	16799757
Application Number:	16798650
Application Number:	16798590
Application Number:	16798682
Application Number:	16801921
Application Number:	16801375
Application Number:	16803952
Application Number:	16803960
Application Number:	16803962
Application Number:	16803958
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Application Number:	16802638
Application Number:	16805244
Application Number:	16805403
Application Number:	16805414
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Application Number:	16816211
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Application Number:	16815860
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Application Number:	16817264
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Application Number:	16818817
Application Number:	16818752

Property Type	Number
Application Number:	16818290
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Application Number:	16819636
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Application Number:	16821849
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Application Number:	16823235
Application Number:	16823185
Application Number:	16822010
Application Number:	16824508
Application Number:	16824581
Application Number:	16824587
Application Number:	16824519
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Application Number:	16824269
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Application Number:	16828948
Application Number:	16828945

Property Type	Number
Application Number:	16828532
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Application Number:	16836424
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Application Number:	16851568
Application Number:	16852091
Application Number:	16851510
Application Number:	16851574

Property Type	Number
Application Number:	16852462
Application Number:	16853275
Application Number:	16853408
Application Number:	16853233
Application Number:	16853407
Application Number:	63013236
Application Number:	16854677
Application Number:	16855549
Application Number:	16857053
Application Number:	16857423
Application Number:	16858332
Application Number:	16858339
Application Number:	16858345
Application Number:	16858350
Application Number:	16858356
Application Number:	16858358
Application Number:	16858390
Application Number:	16858223
Application Number:	16858265
Application Number:	16858318
Application Number:	16859940
Application Number:	16859494
Application Number:	16861118
Application Number:	16861068
Application Number:	16860720
Application Number:	16853440
Application Number:	16861543
Application Number:	16861565
Application Number:	16731672

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	MICHELLE DELOS ANGELES
SIGNATURE:	/Michelle Delos Angeles/
DATE SIGNED:	05/14/2020

Total Attachments: 10
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Execution Version

Patent Collateral Agreement

This Monday, May 11, 2020, WESTERN DIGITAL TECHNOLOGIES, INC. ("*Debtor*"), for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the "*Agent*"), acting as collateral agent hereunder for the Secured Parties as defined in the Security Agreement, dated as of May 12, 2016, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the "*Security Agreement*") for the benefit of the Secured Parties, a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, "*Patent Collateral*"):

(i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on Schedule A hereto (the "*Patents*"); and

(ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

WESTERN DIGITAL TECHNOLOGIES, INC., as Debtor

DocuSigned by:

By: Michael Ray
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Name: Michael Ray
Title: Executive Vice President,
Chief Legal Officer and Secretary

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By: _____

Name:

Title:

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT

[*See Attached.*]

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

No.	Title	Patent/App. Number
1	Storage System and Method for Boundary Wordline Data Retention Handling	16/780,281
2	Storage System and Method for Host Memory Access	16/780,216
3	Dual SLC/QLC Programming and Resource Releasing	16/781,885
4	DATA STORAGE DEVICE MANAGING PEAK CURRENT FOR MULTIPLE ACTUATORS	16/781,194
5	DATA STORAGE DEVICE SORTING ACCESS COMMANDS BASED ON PEAK CURRENT FOR MULTIPLE ACTUATORS	16/781,216
6	Storage System and Method for Optimized Surveillance Search	16/781,717
7	Storage System and Method for Automatic Data Phasing	16/781,688
8	MAGNETIC DEVICE INCLUDING MULTIFERROIC REGIONS AND METHODS OF FORMING THE SAME	16/781,225
9	MAGNETIC RECORDING WRITE HEAD WITH SPIN-TORQUE OSCILLATOR (STO) AND EXTENDED SEED LAYER	16/783,057
10	TRAINING DATA SAMPLE SELECTION FOR USE WITH NON-VOLATILE MEMORY AND MACHINE LEARNING PROCESSOR	16/784,077
11	Nand Dropped Command Detection And Recovery	16/786,889
12	THERMAL RELIEF FOR THROUGH-HOLE AND SURFACE MOUNTING	16/787,482
13	RESTRICTING ACCESS TO A DATA STORAGE SYSTEM ON A LOCAL NETWORK	16/787,859
14	METHOD AND SYSTEM FOR ADDRESS TABLE CACHE MANAGEMENT	16/788,117
15	BiSb Topological Insulator with Novel Buffer Layer that Promotes a BiSb (012) Orientation	62/975,661
16	SPIN-TORQUE OSCILLATOR WITH MULTILAYER SEED LAYER BETWEEN THE WRITE POLE AND THE FREE LAYER IN A MAGNETIC RECORDING WRITE HEAD	16/792,060
17	SPIN TORQUE OSCILLATOR (STO) SENSORS USED IN NUCLEIC ACID SEQUENCING ARRAYS AND DETECTION SCHEMES FOR NUCLEIC ACID SEQUENCING	16/791,759
18	STORAGE DEVICE WITH INCREASED ENDURANCE	16/791,560
19	HEAT-ASSISTED MAGNETIC RECORDING (HAMR) DISK DRIVE WITH INTERFACE VOLTAGE CONTROL CIRCUITRY	16/791,238
20	TWO-DIMENSIONAL MAGNETIC RECORDING (TDMR) READ HEAD STRUCTURE WITH DIFFERENT STACKED SENSORS AND DISK DRIVE INCORPORATING THE STRUCTURE	16/792,010
21	Load/Unload Ramp Mechanism For Reduced Cracking	16/794,079
22	Ultra-low RA and high TMR magnetic sensor with radiation reflective lead	16/794,100
23	DATA STORAGE DEVICE ADAPTOR WITH SECUREMENT MECHANISM	16/799,757
24	VARIABLE READ SCAN FOR SOLID-STATE STORAGE DEVICE QUALITY OF SERVICE	16/798,650
25	DYNAMICALLY ADJUST DATA TRANSFER SPEED FOR NON-VOLATILE MEMORY DIE INTERFACES	16/798,590

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

26	DATA STORAGE DEVICE BANK WRITING SERVO SECTORS FOR INTERLEAVED SERVO CONTROL PROCESSING	16/798,682
27	OFFSET SWAGE BASEPLATE FOR STACKED ASSEMBLY	16/801,921
28	DATA STORAGE DEVICE WITH SPREAD SPECTRUM SPINDLE MOTOR CONTROL	16/801,375
29	SPIN TRANSFER TORQUE (STT) DEVICE WITH TEMPLATE LAYER FOR HEUSLER ALLOY MAGNETIC LAYERS	16/803,952
30	SPIN TRANSFER TORQUE DEVICE WITH OXIDE LAYER BENEATH THE SEED LAYER	16/803,960
31	AREAL DENSITY CAPABILITY IMPROVEMENT WITH A MAIN POLE SKIN	16/803,962
32	SPIN-ORBIT TORQUE INDUCED MAGNETIZATION SWITCHING IN A MAGNETIC RECORDING HEAD	16/803,958
33	OBJECT DETECTION USING MULTIPLE NEURAL NETWORK CONFIGURATIONS	16/803,851
34	Data Storage With Improved Write Performance For Preferred User Data	16/802,638
35	Embedded PHY (EPHY) IP Core for FPGA	16/805,244
36	HAMR Media To Assist Optically Transparent Build-Up On NFT To Improve Reliability	16/805,403
37	In-situ NFT pre-treatment to accumulate optically transparent material on NFT to improve reliability	16/805,414
38	Data Storage With Improved Suspend Resume Performance	16/805,570
39	Data Storage With Improved Read Performance By Avoiding Line Discharge	16/805,574
40	CALIBRATING ELEVATOR ACTUATOR FOR DISK DRIVE	16/806,029
41	DATA STORAGE DEVICE EMPLOYING STAGGERED SERVO WEDGES TO INCREASE CAPACITY	16/808,656
42	MAGNETIC RECORDING HEAD WITH NON-MAGNETIC CONDUCTIVE STRUCTURE	16/811,816
43	Data Storage Device With Improved Interface Transmitter Training	16/812,549
44	Semiconductor Device With Top Die Positioned To Reduce Die Cracking	16/814,761
45	Semiconductor Device Including Magnetic Hold-Down Layer	16/814,812
46	Semiconductor Device Including Contact Fingers On Opposed Surfaces	16/814,864
47	MAGNETIC SENSOR ARRAYS FOR NUCLEIC ACID SEQUENCING AND METHODS OF MAKING AND USING THEM	62/987,831
48	Cycle Borrowing Counter	16/814,631
49	HIGH-BANDWIDTH STO BIAS ARCHITECTURE WITH INTEGRATED SLIDER VOLTAGE POTENTIAL CONTROL	16/816,211
50	DATA STORAGE DEVICE EMPLOYING MULTI-LEVEL PARITY SECTORS FOR DATA RECOVERY PROCEDURE	16/815,416
51	Storage System and Method for Implementing an Encoder, Decoder, and/or Buffer Using a Field Programmable Gate Array	16/815,860
52	DATA STORAGE DEVICE	29/727,700
53	Snapshot management in partitioned storage	16/817,264
54	DATA STORAGE DEVICE CONTROLLING HEAD FLY HEIGHT BASED ON TEMPERATURE	16/817,138

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

55	Multi-Module Integrated Interposer And Semiconductor Device Formed Therefrom	16/818,817
56	High Capacity Semiconductor Device Including Bifurcated Memory Module	16/818,752
57	Semiconductor Device Including High Speed Heterogeneous Integrated Controller And Cache	16/818,290
58	Semiconductor Device Including Vertically Stacked Semiconductor Dies	16/818,883
59	SEMICONDUCTOR DIE AND SEMICONDUCTOR PACKAGE	16/818,426
60	METHODS AND SYSTEMS FOR IMPLEMENTING REDUNDANCY IN MEMORY CONTROLLERS	16/818,949
61	Combined QLC Programming Method	16/818,571
62	Storage System and Method for Improved Playback Analysis	16/818,452
63	MEASUREMENT, CALIBRATION AND TUNING OF MEMORY BUS DUTY CYCLE	16/820,552
64	DEVICES AND METHODS FOR FREQUENCY- AND PHASE-BASED DETECTION OF MAGNETICALLY-LABELED MOLECULES USING SPIN TORQUE OSCILLATOR (STO) SENSORS	16/819,636
65	APERTURE STRUCTURE ON SEMICONDUCTOR COMPONENT BACKSIDE TO ALLEVIATE DELAMINATION IN STACKED PACKAGING	16/821,860
66	EXTENSIBLE STORAGE SYSTEM AND METHOD	16/821,918
67	System and Method to Enhance Solder Joint Reliability	16/821,926
68	REFERENCE-GUIDED GENOME SEQUENCING	16/821,849
69	DEVICES AND METHODS FOR LOCATING A SAMPLE READ IN A REFERENCE GENOME	16/820,711
70	SOFT-DECISION INPUT GENERATION FOR DATA STORAGE SYSTEMS	16/823,235
71	TANGENTIAL AND LONGITUDINAL GLIDE RAMP FOR MAGNETIC STORAGE DEVICE	16/823,185
72	REFERENCE-GUIDED GENOME SEQUENCING	16/822,010
73	Systems and Methods for Multi-Zone Data Tiering for Endurance Extension in Solid State Drives	16/824,508
74	Multi-Stream Journaled Replay	16/824,581
75	DISTRIBUTION OF LOGICAL-TO-PHYSICAL ADDRESS ENTRIES ACROSS BANK GROUPS	16/824,587
76	DYNAMIC MULTI-STAGE DECODING	16/824,519
77	ADJUSTABLE READ RETRY ORDER BASED ON DECODING SUCCESS TREND	16/824,584
78	MULTILAYER FLEX CIRCUIT WITH NON-PLATED OUTER METAL LAYER	16/824,269
79	MAGNETIC GRADIENT CONCENTRATOR/RELUCTANCE DETECTOR FOR MOLECULE DETECTION	16/823,592
80	SWAGE PLATE ASSEMBLY WITH SWAGE BOSS INSERT	16/824,514
81	Entropy Driven Endurance For Normalized Quality Of Service	16/823,714
82	CODE RATE SWITCHING MECHANISM FOR FLASH MEMORY	16/826,063
83	VOLTAGE-CONTROLLED INTERLAYER EXCHANGE COUPLING MAGNETORESISTIVE MEMORY DEVICE AND METHOD OF OPERATING THEREOF	16/824,814

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

84	SYSTEMS AND METHODS FOR QUEUING DEVICE MANAGEMENT CONFIGURATION REQUESTS	16/825,762
85	Power allocation management for external storage	16/825,836
86	WEAR LEVELING IN SOLID STATE DEVICES	16/827,605
87	Data Storage Device, Method and System, and Control of Data Storage Device Based on Writing Operations and Lifetime	16/827,597
88	CONTEXT-AWARE DYNAMIC COMMAND SCHEDULING FOR A DATA STORAGE SYSTEM	16/827,591
89	ADJUSTABLE PERFORMANCE PARAMETERS FOR SSDS	16/827,585
90	POWER MANAGEMENT FOR DATA STORAGE DEVICES IMPLEMENTING NON-VOLATILE MEMORY (NVM) SETS	16/827,548
91	MAMR WRITE HEAD WITH THERMAL DISSIPATION CONDUCTIVE GUIDE	16/828,901
92	PARALLEL PROCESSING OF FILTERED TRANSACTION LOGS	16/828,953
93	METADATA COMPACTION IN A DISTRIBUTED STORAGE SYSTEM	16/828,948
94	DISTRIBUTED OBJECT STORAGE SYSTEM WITH DYNAMIC SPREADING	16/828,945
95	Dynamic Allocation of Sub Blocks	16/828,532
96	ALL-CONNECTED BY VIRTUAL WIRES NETWORK OF DATA PROCESSING NODES	16/829,792
97	ELECTROSTRICTIVE CONTROL FOR THE WIDTH OF A TAPE-HEAD-ARRAY	16/830,222
98	FLEXIBLE ACCELERATOR FOR SPARSE TENSORS IN CONVOLUTIONAL NEURAL NETWORKS	16/830,129
99	FLEXIBLE ACCELERATOR FOR SPARSE TENSORS IN CONVOLUTIONAL NEURAL NETWORKS	16/830,167
100	WRITE DATA PROTECTION AT EMERGENCY POWER OFF	16/831,004
101	SLIDER GAS-BEARING SURFACE DESIGNS WITH LEADING-EDGE POCKETS	16/830,612
102	INTELLIGENT SAS PHY CONNECTION MANAGEMENT	16/831,729
103	Optimized Dual Thermal Fly-Height Design For Dual Writers For Advanced Magnetic Recording	16/831,728
104	NON-VOLATILE MEMORY ARRAY WITH WRITE FAILURE PROTECTION FOR MULTI-LEVEL CELL (MLC) STORAGE ELEMENTS USING COUPLED WRITES	16/831,517
105	TEMPERATURE VARIATION COMPENSATION	16/833,310
106	BANDWIDTH LIMITING IN SOLID STATE DRIVES	16/832,402
107	DATA STORAGE DEVICE MIGRATING DATA FROM NON-ENERGY ASSIST DISK SURFACE TO ENERGY ASSIST DISK SURFACE	16/832,352
108	MAGNETIC RECORDING DEVICES AND METHODS USING A WRITE-FIELD-ENHANCEMENT STRUCTURE AND BIAS CURRENT WITH OFFSET PULSES	16/833,650
109	MICROWAVE-ASSISTED MAGNETIC RECORDING (MAMR) WRITE HEAD WITH COMPENSATION FOR DC SHUNTING FIELD	16/835,198
110	DATA STORAGE DEVICES WITH INTEGRATED SLIDER VOLTAGE POTENTIAL CONTROL	16/833,942
111	Dynamic ZNS open zone active limit	16/835,191
112	PIEZOELECTRIC-BASED MICROACTUATOR ARRANGEMENT FOR MITIGATING OUT-OF-PLANE FORCE AND PHASE VARIATION OF FLEXURE VIBRATION	16/835,016

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

113	SEPARATE STORAGE AND CONTROL OF STATIC AND DYNAMIC NEURAL NETWORK DATA WITHIN A NON-VOLATILE MEMORY ARRAY	16/834,515
114	SHIELDING IMPROVEMENT FOR A DATA STORAGE DEVICE	16/834,403
115	Spintronic Devices with Narrow Spin Polarization Layers	16/836,687
116	SENSOR SYSTEM WITH LOW POWER SENSOR DEVICES AND HIGH POWER SENSOR DEVICES	16/836,764
117	Advanced CE encoding for Bus Multiplexer Grid for SSD	16/836,730
118	Snapback Electrostatic Discharge Protection For Electronic Circuits	16/835,837
119	Command Optimization Through Intelligent Threshold Detection	16/835,836
120	Boosting Reads of Chunks of Data	16/836,679
121	FTL Flow Control For Hosts Using Large Sequential NVM Reads	16/836,454
122	Dual-Connector Storage System and Method for Simultaneously Providing Power and Memory Access to a Computing Device	16/836,424
123	SMART ERASE VERIFY TEST TO DETECT SLOW-ERASING BLOCKS OF MEMORY CELLS	16/837,313
124	Read Modify Write Optimization for Video Performance	16/837,786
125	Advanced File Recovery Method For Flash Memory	16/837,889
126	Zone-append command scheduling based on zone state	16/845,685
127	Weighting Of Read Commands to Zones In Storage Devices	16/847,352
128	Adapting Transmitter Training Behavior Based Upon Assumed Identify Of Training Partner	16/848,700
129	Magnetoresistive Sensor with Improved Magnetic Properties and Magnetostriction Control	16/851,568
130	Storage System and Method for Multiprotocol Handling	16/852,091
131	DATA STORAGE DEVICE CALIBRATING BIAS FOR FINE ACTUATORS	16/851,510
132	DATA STORAGE DEVICE STAGGERING ACCESS OPERATIONS TO FACILITATE CONCURRENT ACCESS OF TWO DISK SURFACES	16/851,574
133	ESTABLISHING CONNECTIONS BETWEEN DATA STORAGE DEVICES	16/852,462
134	Storage System with Privacy-Centric Multi-Partitions and Method for Use Therewith	16/853,275
135	Keeping Zones Open with Intermediate Padding	16/853,408
136	Dynamic Memory Controller and Method for Use Therewith	16/853,233
137	TUNNELING METAMAGNETIC RESISTANCE MEMORY DEVICE AND METHODS OF OPERATING THE SAME	16/853,407
138	High-Throughput DNA Sequencing with Single-Molecule Sensor-Arrays	63/013,236
139	VARIABLE POWER MODE INFERENCING	16/854,677
140	Storage Device Parameter Monitoring for Load Balancing	16/855,549
141	LOW RESISTANCE MONOSILICIDE ELECTRODE FOR PHASE CHANGE MEMORY AND METHODS OF MAKING THE SAME	16/857,053
142	MAGNETIC WRITE HEAD WITH WRITE-FIELD ENHANCEMENT STRUCTURE INCLUDING A MAGNETIC NOTCH	16/857,423
143	STORAGE DEVICES HAVING MINIMUM WRITE SIZES OF DATA	16/858,332

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENT REGISTRATION

144	STORAGE DEVICES HAVING MINIMUM WRITE SIZES OF DATA	16/858,339
145	DATA PARKING FOR SSDS WITH ZONES	16/858,345
146	DATA PARKING FOR SSDS WITH STREAMS	16/858,350
147	STORAGE DEVICES HIDING PARITY SWAPPING BEHAVIOR	16/858,356
148	STORAGE DEVICES HIDING PARITY SWAPPING BEHAVIOR	16/858,358
149	WEIGHTED READ COMMANDS AND OPEN BLOCK TIMER FOR STORAGE DEVICES	16/858,390
150	Mechanism to Improve Driver Capability With Fine Tuned Calibration Resistor	16/858,223
151	TAPE EMBEDDED DRIVE WITH HDD COMPONENTS	16/858,265
152	DUAL DRIVE TAPE EMBEDDED SYSTEM	16/858,318
153	Zone-based device with control level selected by the host	16/859,940
154	System for Accelerated Training of Bit Output Timings	16/859,494
155	BiSb Topological Insulator with Seed Layer or Interlayer to Prevent Sb Diffusion and Promote BiSb (012) Orientation	16/861,118
156	Condensing Logical to Physical Table Pointers in SSDs Utilizing Zoned Namespaces	16/861,068
157	SSD Address Table Cache Management	16/860,720
158	TUNNELING METAMAGNETIC RESISTANCE MEMORY DEVICE AND METHODS OF OPERATING THE SAME	16/853,440
159	DATA STORAGE DEVICE CONFIGURED WITH MANUFACTURE PCB FOR CONCURRENT WRITE/READ OPERATION	16/861,543
160	DATA STORAGE DEVICE COMPRISING DUAL CHANNEL PREAMP CIRCUIT	16/861,565
161	NEAR-FIELD TRANSDUCER FOR HEAT ASSISTED MAGNETIC RECORDING COMPRISING OF THERMALLY STABLE MATERIAL LAYER	10636442
162	NEAR-FIELD TRANSDUCER (NFT) FOR A HEAT ASSISTED MAGNETIC RECORDING (HAMR) DEVICE	10553241
163	AUTOMATIC DATA BACKUP AND CHARGING OF MOBILE DEVICES	16/731,672