PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT6322319

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
HEADWAY TECHNOLOGIES, INC.	02/04/2019

RECEIVING PARTY DATA

Name:	TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
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Internal Address:	HSINCHU SCIENCE PARK
City:	HSINCHU
State/Country:	TAIWAN
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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17035153

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ATTORNEY DOCKET NUMBER:	P2900159/24061.3955US02
NAME OF SUBMITTER:	MARCY OGADO
SIGNATURE:	/Marcy Ogado/
DATE SIGNED:	09/28/2020

Total Attachments: 18
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EXHIBIT B

Patent Assignment

Headway Technologies, Inc., a California Corporation, with an office at 682 South Hillview Drive, Milpitas, CA 95035 ("Assignor") is the owner of the patents and patent applications listed in Schedule 1 hereto (collectively the "Listed Patents"); and

Taiwan Semiconductor Manufacturing Company, Ltd, a Republic of China (Taiwan) company that maintains its principal place of business at No. 8, Li-Hsin Road 6, Hsinchu Science Park, Hsinchu 300-78, Taiwan, R.O.C. ("Assignee"), desires to acquire all right, title and interest in the Listed Patents and the other patents and related rights described below.

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and convey to Assignee and its successors and assigns all right, title and interest that may exist today and in the future to any and all:

(1) Listed Patents;

(2) patents and patent applications to which any of the Listed Patents directly or indirectly claims priority anywhere in the world;

(3) reissues, reexaminations, extensions, continuations, continuations-in-part (except for claims in future continuations-in-part that claim new matter), continuing prosecution applications and divisions of any of the items covered by (1) or (2) above;

(4) foreign counterparts to any of the items covered by (1), (2) or (3) above, including without limitation utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;

(5) inventions, invention disclosures, designs and discoveries described, disclosed or claimed in the items covered by (1) through (4) above;

(6) patents that issue from any of the items covered by (1) through (5) above;

(7) claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items covered by (1) through (6) above, including without limitation all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current or future infringement thereof and including without limitation rights afforded under 35 U.S.C. § 154(d);

(8) royalties, income and other payments due as of the date hereof or hereafter under or arising from any of the items covered by (1) through (7) above; and

(9) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of any kind related to any of the items covered by (1) through (8) above.

Assignor shall execute and deliver any instruments, and do and perform any other acts and things as may be reasonably necessary or desirable for effecting and evidencing the assignments contemplated hereby,

including without limitation the execution, acknowledgment and recordation of any instruments.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks and any other patent office to issue any and all patents, utility models or other governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Assignee.

The assignments and rights pursuant hereto will inure to the benefit of Assignee and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

Assignor, by its duly authorized representative, has executed this assignment on the date set forth below.

DATE: Feb 4, 2019

Headway Technologies, Inc.

By: WENJIE CHEN
Printed/Typed Name

Title: President & CEO

Signature

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California
County of Santa Clara

On Feb. 4, 2019 before me, Marisol M. Moreno, Notary Public, personally appeared Wenjie Chen, who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature of Notary Public

[Affix Seal here]

MARISOL M. MORENO
Notary Public - California
Santa Clara County
Commission # 2165882
My Comm. Expires May 18, 2019

ACCEPTED:

DATE: March 11, 2019

Taiwan Semiconductor Manufacturing Company, Ltd

By: Donald P. McKenna

Name: Donald P. McKenna
Printed/Typed Name

Title: Director

Schedule 1 to Patent Assignment

U.S.

Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	IBM	Renesas	Remark
US7321507	Reference Cell Scheme for MRAM	Yang	11284293	11/21/2005	1/22/2008	O	O	
US7495984	A Reference Cell Scheme for MRAM	Yang	12002183	12/14/2007	3/3/2009	O	O	
US7480172	A Novel Programming Scheme for Segmented Word Line MRAM Array	Shi	11339189	1/25/2006	1/20/2009	O	O	
US7265404	A Novel Bottom Conductor Lead Structure /Method For Fabricating High Performance MTJ for MRAM Applic	Cao	11215276	8/30/2005	9/4/2007	O	O	
US7358100	Improved Bottom Conductor for Integrated MRAM	Cao	11501803	8/14/2007	4/15/2008	O	O	
US7880249	Spacer Structure In MRAM Cell And Method Of Fabricating The Same	Yuan	11290763	11/30/2005	2/1/2011	O	O	
US8422276	Space Structure in MRAM Cell and Method of its Fabrication	Yuan	13020859	1/28/2011	4/16/2013	O	O	
US7696548	MRAM with Super-paramagnetic sensing layer	Wang	11200360	8/9/2005	4/13/2010	O	O	
US8035929	MRAM with Storage Layer and Super Paramagnetic Sensing Layer	Wang	12661349	3/15/2010	10/18/2011	O	O	
US8062909	MRAM with Storage Layer and Super Paramagnetic Sensing Layer	Wang	12661365	3/16/2010	11/22/2011	O	O	
US8178363	MRAM with Storage Layer and Super-Paramagnetic Sensing Layer	Wang	13289127	11/4/2011	5/15/2012	O	O	
US7362644	A Configurable MRAM	Yang	11313019	12/20/2005	4/22/2008	O	O	
US7345911	Multi-Bit Thermal Assisted Integrated Storage Layer MRAM Design	Min	11353339	2/14/2006	3/18/2008	O	O	
US7598555	Multi-State Thermally Assisted Storage	Min	12012975	2/4/2008	9/15/2009	O	O	
US7479394	A Novel Oxidation Structure/Method To Form MgO/NiFe(free layer)-MTJ for high performance MRAM_spp8	Horng	11317388	12/22/2005	1/20/2009	O	O	
US8687458	Magnetic Random Access Memory with Selective Toggle Memory Cell	Gan	12181234	8/8/2008	3/18/2014	O	O	
US7838436	Bottom Electrode For MRAM Device And Method To Fabricate It	Horng	11528877	9/28/2006	11/23/2010	O	O	
US8273666	Process to Fabricate Bottom Electrode for MRAM Device	Xiao	12927815	11/19/2010	9/25/2012	O	O	
US8698259	Bottom Electrode for MRAM Device	Xiao	12927870	11/19/2010	2/9/2015	O	O	
US7456029	Planar Flux Concentrator For MRAM Devices	Guo	11478485	6/28/2006	11/25/2008	O	O	
US7582942	Planar Flux Concentrator for MRAM Devices	Guo	12290410	10/30/2008	9/1/2009	O	O	
US7672093	Hafnium Doped Cap and Free Layer for MRAM Device	Horng	11582244	10/17/2006	3/2/2010	O	O	
US7508042	Spin Transfer MRAM Device With Magnetic Biasing	Guo	11644132	12/22/2006	3/24/2009	O	O	
US7715224	MRAM with Enhanced Programming Margin	Min	11787335	4/16/2007	5/11/2010	O	O	
US7885094	MRAM With Cross-Tie Magnetization	Min	12150241	4/25/2008	2/8/2011	O	O	
US7609543	Method and Implementation Of Stress Test for MRAM	Yang	11904439	9/27/2007	10/27/2009	O	O	
US7480173	Spin Transfer MRAM Device With Novel Magnetic Free Layer	Guo	11717347	3/13/2007	1/20/2009	O	O	
US8058697	Spin Transfer MRAM Device With Novel Magnetic Synthetic Free Layer	Guo	11729491	3/29/2007	11/15/2011	O	O	
US8259881	Spin Transfer MRAM Device with Novel Magnetic Synthetic Free Layer	Guo	13373173	11/7/2011	9/18/2012	O	O	
US7852662	Spin Torque Switching MRAM, SpinRAM, Array	Yang	11789324	4/24/2007	12/14/2010	O	O	
US7508700	Method Of Magnetic Tunneling Layer Pattern Layout For MRAM	Zhang	11724425	3/15/2007	3/24/2009	O	O	
US8497559	MRAM With Means of Controlling Magnetic Anisotropy	Min	11973781	10/10/2007	7/30/2013	O	O	
US7663131	A Novel SyAF Structure To Fabricate Mbit MTJ MRAM	Horng	11716728	3/8/2007	2/16/2010	O	O	
US9830321	Spin Transfer MRAM Device with Reduced Coefficient of MTJ Resistance Variation	Guo	11881627	7/22/2016	1/8/2018	O	O	
US7750421	A High Performance MTJ Element for STT-RAM And Method For Making the Same	Horng	11880563	7/23/2007	7/6/2010	O	O	
US8436437	A High Performance MTJ Element for STT-RAM and Method for Making the Same	Horng	12803181	6/21/2010	5/7/2013	O	O	
US8058699	A High Performance MTJ Element for STT-RAM and Method for Making the Same	Horng	12803189	6/21/2010	11/15/2011	O	O	
US8080432	A High Performance MTJ Element STT-RAM and Method for Making the Same	Horng	12803190	6/21/2010	12/20/2011	O	O	
US8133745	Method Of Magnetic Tunneling Layer Processes For Spin-Transfer Torque MRAM Devices	Zhong	11975045	10/17/2007	3/13/2012	O	O	
US7936027	Method Of MRAM Fabrication With Zero Electrical Shorting	Xiao	12006893	1/7/2008	5/3/2011	O	O	
US7577021	Spin Transfer MRAM Device With Separated CPP Assisted Writing	Guo	11986675	11/21/2007	8/18/2009	O	O	
US7755933	Spin Transfer MRAM Device with Separated CPP Assisted Writing	Guo	12462453	8/4/2009	7/13/2010	O	O	
US7760544	Spin Transfer MRAM Device with Separated CPP Assisted Writing	Guo	12462434	8/4/2009	7/20/2010	O	O	

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US7764536	Spin Transfer MRAM Device with Separated CPP Assisted Writing	Guo	12462462	8/4/2009	7/27/2010	O	O	
US8334213	Sulfide Hardmask Etching Process in MRAM Cell	Mao	12455787	5/5/2009	12/18/2012	O	O	
US8372661	A High Performance MTJ Element for Conventional MRAM And For STT-RAM And Method For Making The Same	Hong	11981127	10/31/2007	2/12/2013	O	O	
US8716003	A High Performance MTJ Element for Conventional MRAM and for STT-RAM and a Method for Making the Same	Hong	13764357	2/11/2013	5/13/2014	O	O	
US8057925	A Low Switching Current Dual Spin Filter (DSF) Element for STT_RAM and Method for Making The Same	Hong	12078448	3/27/2008	11/15/2011	O	O	
US8404367	Low Switching Current Dual Spin Filter (DSF) Element for STT-RAM and a Method for Making the Same	Hong	13317484	10/19/2011	3/26/2013			
US8779491	Method of Forming a Spin-Transfer Torque Random Access Memory (STT-RAM) Device	Hong	13373128	11/4/2011	8/26/2014	O	O	
US7940044	A Low Switching Current MTJ Element For Ultra-High STT-RAM and Method For Making The Same	Hong	12082155	4/8/2008	5/24/2011	O	O	
US7755951	Boosted Gate Voltage Programming For Spin-RAM Array	Hou	12313487	11/20/2008	8/24/2010	O	O	
US8246845	Boosted Gate Voltage Programming for Spin-Torque MRAM Array	Yang	12809984	9/5/2010	8/21/2012	O	O	
US8132881	Structure and Method To Fabricate High Performance MTJ Devices For Spin-Transfer Torque (STT) - RAM	Hong	12284088	9/18/2008	3/20/2012	O	O	
US7920072	A Novel Spin Momentum Transfer MRAM Design	Min	12813706	11/24/2008	4/19/2011	O	O	
US7957186	Single Bit Line SMT MRAM Array Architecture and the Programming Method	Yang	12307537	9/4/2009	6/7/2011	O	O	
US7804708	Sulfide Electrode Mask Design For Ultra-Thin Interlayer Dielectric Approach in MRAM Devices Fabrication	Zhang	12310117	11/17/2008	9/28/2010	O	O	
US7894497	A Novel MRAM Design With Coupling Valve Switching Mechanism	Min	12361567	2/13/2009	8/8/2011	O	O	
US7884403	Method to High Density Spin-Transfer Torque MRAM Process	Zhang	12290496	10/31/2008	8/8/2011	O	O	
US8324663	High Density Spin-Transfer Torque MRAM Process	Zhang	13030833	2/4/2011	12/4/2012	O	O	
US8159081	A High Density Spin-Transfer Torque MRAM Process	Zhang	12931648	2/7/2011	5/22/2012	O	O	
US8018758	Gate Drive Voltage Boost Schemes For Memory Array	Yang	12468005	7/6/2009	9/13/2011	O	O	
US7885572	Magnetic Memory Capable Of Minimizing Gate Voltage Stress In Unselected Memory Cells	Yang	12082958	9/17/2008	7/29/2011	O	O	
US8170879	Controlling the Accumulated Read Error In A Memory System	Yang	12468923	5/20/2009	10/27/2010	O	O	
US7936027	A Novel Free Layer/Capping Layer For High Performance MRAM MTJ	Hong	12319571	1/14/2009	10/5/2010	O	O	
US8680582	STT-RAM with A Magnetic Tunnel Junction Written in Thermally Assisted Method	Hong	12480413	7/17/2009	12/17/2013	O	O	
US8304271	Structure and Method to Fabricate High Performance MTJ Devices for Spin-Transfer Torque (STT)-RAM Application	Hong	14058804	12/9/2013	6/3/2016	O	O	
US7989230	Method of Double Patterning and Etching Magnetic Tunnel Junction Structures for Spin-Transfer Torque	Belen	12382259	3/23/2009	1/4/2011	O	O	
US8437161	Shared Bit Line Array With Slidin Transistors Between the Bit Lines	Yang	13803823	6/28/2010	5/7/2013	O	O	
US8565014	Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines	Yang	13687287	5/4/2013	10/22/2013	O	O	
US8576618	Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines	Yang	13687288	5/4/2013	11/5/2013	O	O	
US8570793	Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines	Yang	13687289	5/4/2013	10/29/2013	O	O	
US8964577	Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines	Yang	13687291	5/4/2013	2/18/2014	O	O	
US7919407	Method of High Density Field Induced MRAM Process	Tom	12550346	11/17/2009	4/5/2011	O	O	
US8043463	Method of High Density Memory Fabrication	Tom	12556660	5/29/2009	10/17/2016	O	O	
US8274819	Read Disturb Free SMT Reference Cell Scheme II	Yang	12859239	8/4/2010	9/25/2012	O	O	
US8139395	A Novel Bit Line Preparation Method in MRAM Fabrication	Mao	12559140	10/29/2009	3/20/2012	O	O	

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US8722543	Composite Hard Mask With Upper Sacrificial Dielectric Layer for the Patterning and Etching of Nanometer Size MRAM Devices	Balan	12804540	7/30/2010	5/13/2014	O	O	
US8432287	A pulse field assisted spin momentum transfer MRAM design	Min	12807511	9/8/2010	4/16/2013	O	O	
US8133809	Method to Fabricate Thin Metal Via Interconnects on Copper Wires in MRAM Devices	Mao	12806381	8/11/2010	3/13/2012	O	O	
US8605520	Replaceable, Precise-Tracking Reference Lines	Pu	12924184	9/22/2010	12/10/2013	O	O	
US8488357	Reference Cell Architectures for Small Memory Array Block Activation	Sunaga	12925492	10/22/2010	7/16/2013	O		
US8217684	Fast and Accurate Current Driver with Zero Standby Current and Features for Boost and Temperature Compensation for MRAM Write	Yuh	12925004	10/12/2010	7/10/2012	O		
US8786036	Improved Magnetic Tunnel Junction for MRAM Applications	Cao	12930577	1/10/2011	7/22/2014	O		
US9224940	Magnetic Tunnel Junction for MRAM Applications	Cao	14316436	6/26/2014	12/29/2015	O		
US9455400	Magnetic Tunnel Junction for MRAM Applications	Cao	14979949	12/28/2015	9/27/2016			
US8693273	Averaging for MRAM Sense Amplifiers	Yuh	13345116	1/6/2012	4/8/2014			
US8775865	Method and Apparatus for Scrubbing Accumulated Disturb Data Errors in Array of SMT MRAM Mem Cells Inc Rewriting Ref Bits	Yang	13195292	7/28/2011	7/8/2014			
US8492169	Improved Magnetic Tunnel Junction for MRAM Applications	Cao	13136529	8/15/2011	7/23/2013			
US8735004	Magnetic Tunnel Junction for MRAM Applications	Wei	13941741	7/15/2013	5/27/2014			
US8900884	MTJ Element for STT MRAM	[illegible]	13525502	6/18/2012	12/2/2014			
US8921961	Storage Element for STT MRAM Applications	Kula	13617482	9/14/2012	12/30/2014			
US8981503	STT-MRAM Reference Layer Having Substantially Reduced Stray Field and Consisting of a Single Magnetic Domain	Beach	13421983	3/16/2012	3/17/2015			
US6969895	MRAM Cell With Flat Topography and Controlled Bit Line to Free Layer Distance and Method of Manufact	Han	10733013	12/10/2003	11/29/2005	O	O	
US7335960	MRAM Cell with Flat Topography and Controlled Bit Line to Free Layer Distance and Method of Manufact	Han	11178282	7/12/2005	2/26/2008	O	O	
US6974708	Oxidation Structure/Method to Fabricate a High-Performance Magnetic Tunneling Junction MRAM	Horng	10820391	4/8/2004	12/13/2005	O	O	
US7045841	Oxidation Structure/Method to Fabricate a High-Performance Magnetic Tunneling Junction MRAM	Horng	11268362	11/7/2005	5/16/2006	O	O	
US6979586	Magnetic Random Access Memory Array with Coupled Soft Adjacent Magnetic Layer	Guo	10872915	6/21/2004	12/27/2005	O	O	
US7085183	Adaptive Algorithm for MRAM Manufacturing	Yang	10889011	7/13/2004	8/1/2006	O	O	
US7045368	MRAM Cell Structure and Method of Fabrication	Hong	10849311	5/19/2004	5/16/2006	O	O	
US7476919	MRAM Cell Structure and Method of Fabrication	Hong	11418910	5/5/2006	1/13/2009	O	O	
US7611912	A Novel UnderLayer For High Performance Magnetic Tunneling Junction MRAM	Horng	10881449	6/30/2004	11/3/2009	O	O	
US7999985	A Novel Underlayer for High Performance Magnetic Tunneling Junction MRAM	Horng	12589485	10/23/2009	8/16/2011	O	O	
US8673654	A Novel Underlayer for High Performance Magnetic Tunneling Junction MRAM	Horng	12589465	10/23/2009	3/18/2014	O	O	
US7241632	Method of Fabricating MRAM Cell Structure Containing Sidewall Spacers	Yang	11106330	4/14/2005	7/10/2007	O	O	
US7544382	MTJ read head with sidewall spacers	Yang	11825032	7/2/2007	6/9/2009	O	O	
US7978505	Heat Assisted Switching and Separated Read-Write MRAM	Zhou	12322107	1/29/2009	7/12/2011	O	O	
US8184411	MTJ incorporating CoFe/Ni multilayer film with perpendicular anisotropy for MRAM application	Zhang	12589614	10/26/2009	5/22/2012	O	O	
US8456883	Method of Spin Torque MRAM Process Integration	Liu	13482157	5/29/2012	6/4/2013			
US8860156	Minimal Thickness SAF Structure with Perpendicular Magnetic Anisotropy for STT-MRAM	Beach	13609780	9/11/2012	10/14/2014			
	Minimal Thickness Synthetic Antiferromagnetic (SAF) Structure with Perpendicular Magnetic Anisotropy for STT-MRAM	Beach	14489507	9/18/2014				
US8772051	Fabrication Method for Embedded Magnetic Memory	Zhong	13766086	2/14/2013	7/8/2014			

US8817038	Adaptive Reference Scheme for Magnetic Memory Applications	Jan	13660178	10/25/2012	12/23/2014			
US9843132	MRAM Write Pulses to Dissipate Intermediate State Domains	Lee	13830923	3/23/2013	3/17/2015			
US9747965	Improved Adaptive Reference Scheme for Magnetic Memory Applications	Jan	14980356	12/28/2015	8/29/2017			
	Improved Adaptive Reference Scheme for Magnetic Memory Applications	Jan	15686448	8/25/2017				
US9880816	Implementation of One Time Programmable Memory using a MRAM Stack Design	Jan	15078183	3/23/2016	10/31/2017			
US9780236	Seed Layer for Improving the Thermal Budget of the PMA Layer for Embedded MRAM Applications	Zhu	14946232	11/23/2015	10/3/2017			
	Seed Layer for Improving the Thermal Budget of the PMA Layer for Embedded MRAM Applications	Zhu	15707373	9/18/2017				
	A Writing Scheme to Reduce Back Hopping for STT-MRAM	Liu	15618118	8/7/2017				
US9868569	MgO Insertion in Free Layer for Magnetic Memory Applications	Iwata	15/461775	3/17/2017	5/8/2018			
	MgO Insertion in Free Layer for Magnetic Memory Applications	Iwata	15/972284	5/7/2018				
US9871195	Spacer Assisted Ion Beam Etching of Spin Torque Magnetic Random Access Memory	Yang	15/465044	3/22/2017	1/16/2018			
	STT-MRAM Heat Sink and Magnetic Shield Structure Design for More Robust Read/Write Performance	Zhong	15857783	12/29/2017				
				8/23/2018				Remark, it is #137
	Initialization Process for Magnetic Random Access Memory	Lee	15818149	11/20/2017				
	Self-Adaptive Halogen Treatment to Improve Photoresist pattern and MRAM Device uniformity	Yang	15685240	8/24/2017				
	High Thermal Stability by Doping of Oxide Capping Layer for Spin Torque Transfer (STT) Magnetic Random Access Memory	Jan	15728815	10/10/2017				
US10134892	Free Layer Sidewall Oxidation and Spacer Assisted Magnetic Tunnel Junction (MTJ) Etch for High Performance Magnetoresistive Random Access Memory (MRAM) Devices	Yang	15789150	10/20/2017	11/20/2018			
	Nitride Capping Layer for Spin Torque Transfer (STT)-Magnetoresistive Random Access Memory (MRAM)	Iwata	15881033	1/25/2018				
	CMP Stop Layer and Sacrifice Layer for High Yield Small Size MRAM Devices	Yang	15891767	2/8/2018				
	Multiply Spin-Coated Ultra-Thick Hybrid Hard Mask for Sub 60nm MRAM Devices	Yang	15895085	2/13/2018				
	Fabrication of Large Height Top Metal Electrode for Sub 60nm MRAM Devices	Yang	15902415	2/22/2018				
	Metal/Dielectric/Metal Hybrid to Define Ultra-large Height Top Electrode for Sub 60nm MRAM Devices	Yang	15902381	2/22/2018				
	Novel Free Layer Structure of Magnetoresistive Memory (MRAM) for Metal Mo or W Capping Layer	Fukuzawa	15/933479	3/23/2018				
	Ion Beam Etching Fabricated Sub 30nm Vias to Reduce Conductive Material Re-Deposition for Sub 60nm MRAM Devices	Yang	15/947812	4/6/2018				
	Highly Selective Ion Beam Etch Hard Mask for Sub 60nm MRAM Devices	Yang	15951873	4/12/2018				
	Highly Physical Ion Resistive Spacer to Define Chemical Damage Free Sub 60nm MRAM Devices	Yang	15986244	5/22/2018				
	Sub 60nm Etchless MRAM Devices by Ion Beam Etching Fabricated T-shaped Bottom Electrode	Yang	16008839	6/14/2018				
	Under-cut Via Electrode for Sub 60nm Etchless MRAM Devices by Decoupling the Via Etch Process	Yang	16008880	6/14/2018				
US7122386	Pad/DD Structure	Torng	11031874	9/21/2005	10/17/2006	O	O	
US8450119	Magnetic Tunnel Junction Patterning Using Ta/TaN as Hard Mask	Torng	11378558	3/17/2006	5/28/2013	O	O	
US7528457	A Novel Method To Form Non-magnetic NiFeMg Cap for the NiFe(free)-MTJ Stack to Enhance dR/R	Horng	11404448	4/14/2006	5/5/2009	O	O	
US7595520	Paramagnetic-NiFeHf Capping Layer Is Deposited By Co-Sputtering of NiFe and Hf	Horng	11480891	7/31/2006	9/29/2009	O	O	
US8378330	A Novel Capping Layer for a Magnetic Tunnel Junction Device to Enhance dR/R and a Method of Making	Horng	12584190	9/1/2009	2/19/2013	O	O	

US8179892	A Process For Manufacturing A Magnetic Tunnel Junction (MTJ) Device	Horng	12657776	1/27/2010	5/15/2012	○	○	
US7598579	A Novel Magnetic Tunnel Junction (MTJ) To Reduce Spin Transfer Magnetization Switching Current	Horng	11699875	1/30/2007	10/6/2009	○	○	
US8238292	A Novel Magnetic Tunnel Junction (MTJ) to Reduce Spin Transfer Magnetization Switching Current	Horng	12584946	9/15/2009	8/15/2012	○	○	
US8456893	A Novel Magnetic Tunnel Junction (MTJ) to Reduce Spin Transfer Magnetization Switching Current	Horng	12584871	9/15/2009	6/4/2013	○	○	
US7696551	Composite Hard Mask For the Patterning/Etching Of Nanometer-size Magnetic Multilayer-based device	Xiao	11901989	9/20/2007	4/13/2010	○	○	
US8105948	Method Of Exposing Magnetic Tunnel Junction Structure Using Chemical Mechanical Polishing	Zhong	12070286	2/14/2008	1/31/2012	○	○	
US8169816	Design and Fabrication Methods of Partial Cladded Write Line to Enhance Write Margin for Magnetic Ra	Min	12584562	9/10/2009	5/1/2012	○	○	
US8470462	Structure/Method for Enhancing Interfacial Perpendicular Anisotropy in CoFe(B)/MgO/CoFeB Magnetic Tunnel Junction	Horng	12927939	11/30/2010	6/25/2013	○		
US9159908	Composite magnetic free layer within magnetic tunnel junction for MRAM application	Gan	13068222	5/6/2011	10/13/2015	○		
US8541855	Co/Ni Multilayers with Improved Out-of-plane Anisotropy for Magnetic Device Applications	Jan	13068398	5/10/2011	9/24/2013	○		
US8508006	Co/Ni Multilayers with Improved Out-of-plane Anisotropy for Magnetic Device Applications	Jan	13561301	7/30/2012	8/13/2013			
US9373780	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	13955035	7/31/2013	6/21/2016	○		
US8698261	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	13955039	7/31/2013	4/15/2014	○		
US8987849	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14264943	4/4/2014	3/24/2015	○		
US8878323	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14032983	9/20/2013	11/4/2014	○		
US9373777	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14528242	10/31/2014	6/21/2016	○		
US9478733	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14528246	10/31/2014	10/25/2016	○		
US9373778	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14528251	10/31/2014	6/21/2016	○		
US9081285	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14528254	10/31/2014	7/14/2015	○		
US8987847	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14264937	4/4/2014	3/24/2015	○		
US8987848	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14264940	4/4/2014	3/24/2015	○		
US8962348	Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	14032869	9/20/2013	2/24/2015	○		
US9006704	Magnetic element with improved out-of-plane anisotropy for spintronics applications	Jan	13031990	2/11/2011	4/14/2015	○		
US8592927	Multilayers having reduced perpendicular demagnetizing field using moment dilution for spintronics applications	Jan	13068172	5/4/2011	11/26/2013	○		
US9048411	Multilayers Having Reduced Perpendicular Demagnetizing Field Using Moment Dilution for Spintronic Application	Jan	14047130	10/7/2013	6/2/2015	○		
US8823118	Spin Torque transfer MTJ fabricated with a composite tunneling barrier layer	Horng	13344232	1/5/2012	9/2/2014			
US8871365	High thermal stability reference structure with out-of plane anisotropy for Magnetic Device	Wang	13406972	2/28/2012	10/28/2014			
US9472752	High Thermal Stability Reference Structure with Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	14483418	3/22/2014	10/18/2016			

US9466789	High Thermal Stability Reference Structure with Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	14511273	10/10/2014	10/11/2016			
	Reduction of Capping Layer Resistance Area Product for Magnetic Device Applications	Jan	13441156	4/6/2012				
US9349934	High Thermal Stability Free Layer with High Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	13459455	4/27/2012	5/24/2016			
US8852760	High Thermal Stability Free Layer Structure with Out-of Plane Anisotropy for Magnetic Device Applications	Wang	13448557	4/17/2012	10/7/2014			
US8748187	Reverse Partial Etching Scheme for Magnetic Device Applications	Wang	13418507	3/14/2012	6/10/2014			
	Improve MTJ CD Variation by HM Trimming	Shen	15/968183	5/22/2018				
US8039908	Method to Make Small Isolated Features with Pseudo-Planarization for TMR and MRAM	Pan	10/719723	11/21/2003	5/16/2006	O	O	
US8884511	Novel Method to Connect a Magnetic Device to CMOS Transistor	Zhong	13871679	5/10/2013	5/6/2013			
	Multi-layer Structure for Reducing Film Roughness in Magnetic Devices	Zhu	15/597755	5/17/2017				
US9806177	Method to Minimize MTJ Sidewall Damage and Bottom Electrode Redeposition using IBE Trimming	Annapragada	14/948378	5/9/2016	2/23/2017			
	Perpendicularly Magnetized Ferromagnetic Layers having an Oxide Interface Allowing for Improved Control of the Oxidation	Thomas	15/199867	6/29/2016				
US9972385	Seed Layer for Growth of <111> Magnetic Materials	Liu	15/079459	3/24/2016	5/8/2017			
US9880473	New Surface Treatment Method for DARC to Enable Photo Resist CD	Hao	15/199286	6/29/2016	1/30/2018			
	Scanning Ferromagnetic Resonance for Wafer-Level Characterization of Magnetic Thin Films and Multilayers	Gubbins	15/463014	3/20/2017				
	Protective Passivation Layer for Magnetic Tunnel Junctions	Jones	15/463113	3/20/2017				
US9972777	MTJ Device Process/Integration Method with Pre-Patterned Seed Layer	Hao	15/479497	4/5/2017	5/15/2018			
	Post Treatment to Reduce Shunting Devices for Physical Etching Process	Wang	15/472614	4/5/2017				
US9935261	Dielectric Encapsulation Layer for Magnetic Tunnel Junction (MTJ) Devices using Radio Frequency (RF) Sputtering	Patel	15/478622	4/5/2017	4/3/2018			
	A Method to Remove Sidewall Damage after MTJ Etching	Zhongliang	15/468642	3/23/2017				
	Combined Physical and Chemical Etch to Reduce Magnetic Tunnel Junction (MTJ) Sidewall Damage	Shen	15/588484	5/15/2017				
	Cavity-Based Encapsulation Layer for Magnetic Tunnel Junctions	Sundar	15/619828	6/12/2017				
US10014466	Maintaining Coercive Field After High Temperature Anneal for Magnetic Device Applications with Perpendicular Magnetic Anisotropy	Liu	15/477218	4/3/2017	7/3/2018			
	Maintaining Coercive Field After High Temperature Anneal for Magnetic Device Applications with Perpendicular Magnetic Anisotropy	Liu	16/022808	6/29/2018				
US10038136	High Temperature Volatilization of Sidewall Materials from Patterned Magnetic Tunnel Junctions	Patel	15/720639	10/10/2017	7/31/2018			
US10043851	Improve Etch Selectivity by Introducing Oxidants to Noble Gas During Physical MTJ Etching	Shen	15/668113	8/3/2017	8/7/2018			
	Low Resistance MgO Capping Layer for Perpendicularly Magnetized magnetic Tunnel Junctions	Patel	15/841479	12/14/2017				
	Etch-Less Self Aligned Magnetic Tunnel Junction (MTJ) Device Structure	Hao	15/653195	7/18/2017				
	Pulse Writing in Perpendicular Magnetic Recording	Tang	15/933486	3/23/2018				
	Electrical Testing Apparatus for Spintronics Devices	Jan	15/932407	2/22/2018				
	Improving MTJ Device Performance by Controlling Device Shape's	Hao	15/810484	11/13/2017				
	Ferromagnetic Resonance (FMR) Electrical Testing Apparatus for Spintronic Devices	Jan	15/875208	1/19/2018				
US10193067	Improved Magnetic Tunnel Junction (MTJ) Performance by Introducing Oxidants to Methanol with or without Novel Gas during MTJ Etch	Shen	15/850129	12/28/2017	10/11/2018			

U.S.

	Improvement of MTJ Device Performance by Adding Stress Modulation Layer to MTJ Device Structure	Hsu	16/988,038	5/23/2018				
US8716839	Engineered Magnetic Layer Having Improved Perpendicular Anisotropy Using Glassing Agents for Spintronics Applications	Jan	13/406,556	2/29/2012	4/29/2014			
US8969983	Engineered Magnetic Layer Having Improved Perpendicular Anisotropy Using Glassing Agents for Spintronics Applications	Jan	13/548,669	7/13/2012	4/18/2014			
US9202710	Free Layer with Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	13/689,169	11/27/2012	2/2/2016			
US9437268	Free Layer with Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	14/868,871	10/15/2015	9/6/2016			
US9691505	Mg Discontinuous Insertion Layer for Improving MTJ Stack	Moriyama	13/730,918	9/11/2013	3/17/2015			
US9082960	Fully Compensated SyntheticAntiferromagnet for Spintronics Applications	Jan	13/668,542	5/16/2013	7/14/2015			
US9147833	Hybridized Oxide Capping Layer for Perpendicular Magnetic Anisotropy	Ki	13/838,999	3/15/2013	9/29/2015			
US9236559	Hybridized Oxide Capping Layer for Perpendicular Magnetic Anisotropy	Pi	14/842,098	9/1/2015	1/12/2016			
US9478601	Hybridized Oxide Capping Layer for Perpendicular Magnetic Anisotropy	Pi	14/817,047	8/3/2015	9/1/2016			
US9422387	Maintain Coercive Field after High Temperature Anneal for Magnetic Device Applications with Perpendicular Magnetic Anisotropy	Liu	14/847,433	9/8/2015	8/23/2016			
US9490054	Seed Layer for Multilayer Magnetic Materials	Jan	13/648,327	10/11/2012	11/8/2016			
	Improved Seed Layer for Multilayer Magnetic Materials	Jan	13/944,918	7/17/2013				
	Multiple Hard Mask Patterning to Fabricate 20nm and Below MRAM Devices	Yang	15/799,849	10/31/2017				
	Dual Magnetic Tunnel Junction Stack Design	Sundar	16/133,864	9/18/2018				
	Improved CD Uniformity of Island Photo Resist Pattern (Isolated) Using Alternating Phase Shifting Mask	Hsu	16/133,880	9/18/2018				
	Self-Aligned Encapsulation Hard Mask to Separate Physically Under-Etched MTJ Cells to Reduce Conductive Re-Deposition	Yang	16/133,079	9/27/2018				
	Large Height Trim-Like Sub 50nm Vias to Reduce Conductive Material Re-Deposition for Sub 60nm MRAM Devices	Yang	16/133,088	9/27/2018				
	Highly Physical Etch Resistive Photoresist Mask to Define Large Height Sub 30nm Via and Metal Hard Mask for MRAM Devices	Yang	16/133,955	9/18/2018				
	Dual Magnetic Tunnel Junction Devices for Magnetic Random Access Memory (MRAM)	Sundar	16/056,791	8/7/2018				
	Multi-Probe Ferromagnetic Resonance (FMR) Apparatus for Wafer Level Characterization of Magnetic Films	Gubbala	16/056,783	8/7/2018				
	Improved Magnetic Layer for Magnetic Random Access Memory (MRAM) by Moment Enhancement	Jan	16/106,063	8/22/2018				
	Avoiding Oxygen Plasma Damage During Hard Mask Etching in Magnetic Tunnel Junction (MTJ) Fabrication Process	Shen	16/056,770	8/7/2018				
	Method for Measuring Saturation Magnetization of Magnetic Films and Multilayer Films	Gubbala	16/161,150	10/16/2018				
	Monolayer-by-Monolayer Growth of MgO Layers Using Mg Sublimation and Oxidation	Patel	16/161,161	10/16/2018				
	Multiple Spacer Assisted Physical Etching of Sub 60nm MRAM Devices	Yang	16/161,139	10/16/2018				
	Multi-layer Structure for Reducing Film Roughness in Magnetic Devices	Zhu	16/173,601	10/29/2018				
	Coating for PMA (Perpendicular Magnetic Anisotropy) Enhancement of STT-MRAM (Spin-Torque Transfer-Magnetic Random Access Memory) Devices	Liu	16/184,839	11/9/2018				
US8650468	Method of Forming a Magnetic Tunneling Junction (MTJ) MRAM Device and a TMR Read Head	Horng	10/846,510	5/16/2004	11/11/2005			
US7736908	Method of Forming a Magnetic Tunneling Junction (MTJ) MRAM	Horng	11/280,049	5/16/2004	7/3/2007			
US8802203	Method to Reduce Magnetic Film Stress for Better Yield	Zhong	13/439,533	5/11/2012	8/12/2014			

U.S.

US9691542	Method to Reduce Magnetic Film Stress for Better Yield	Zhong	14454524	6/7/2014	1/13/2015			
	Seed Layer for PMA Thin Film	Morgunov	13863545	4/16/2013				
	Reduction of Barrier Resistance X Area (RA) Product and Protection of (PMA) for Magnetic Device Applications	Liu	14276243	5/15/2014				
US9697993	MTJ Etching with Improved Uniformity and Profile for Acting Passivation Step	Shen	14726546	5/31/2015	2/6/2018			
US9842990	Magnetic Tunnel Junction with Low Defect Rate after High Temperature Anneal for Magnetic Device Applications	Liu	14609111	7/29/2015	12/12/2017			
	Magnetic Tunnel Junction with Low Defect Rate after High Temperature Anneal for Magnetic Device Applications	Liu	15835952	12/8/2017				
	Physical Cleaning with In-Situ Dielectric Encapsulation Layer for Spintronic Device Application	Wang	14813854	7/30/2015				
	Title Multilayer Structure for Reducing Film Roughness in Magnetic Devices	Zhu	16221908	12/17/2018				HT18-008_CIP/E_CON Contin of s/n 16170251
	Minimal Thickness Synthetic Antiferromagnetic (SAF) Structure with Perpendicular Magnetic Anisotropy for STT-MRAM	Beach	16236770	1/30/2019				HT18-01188 Div of s/n 14466507

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1	Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	IBM	Renesas
2	[illegible]	Reference Cell Scheme for MRAM	Yang	2008-314868	11/21/2008	3/2/2012	O	O
3	[illegible]	Spacer Structure in MRAM Cell And Method Of Fabricating The Same	Yuan	2008-323678	11/30/2008	7/3/2013	O	O
4	[illegible]	A Configurable MRAM	Yang	2008-342720	12/25/2008	8/5/2013	O	O
5	[illegible]	A Novel Oxidation Structure/Method To Form MgO/NiFe(free layer)-MTJ for high performance MRAM appli	Horng	2006-346048	10/23/2006	8/24/2012	O	O
6	[illegible]	A Novel Method To Form Non-magnetic NiFeMg Cap for the NiFe(free)-MTJ Stack to Enhance dR/R	Horng	2007-105481	4/13/2007	8/24/2012	O	O
7	[illegible]	Paramagnetic-NiFeHf Capping Layer Is Deposited By Co-Sputtering of NiFe and Hf	Horng	2007-199432	7/31/2007	8/23/2013	O	O
8	[illegible]	Hafnium Doped Cap and Free Layer for MRAM Device	Horng	2007-270868	10/17/2007	8/1/2012	O	O
9	[illegible]	Spin Transfer MRAM Device With Novel Magnetic Synthetic Free Layer	Guo	2008-80960	3/26/2008	8/20/2014	O	O
10	[illegible]	Spin Torque Switching MRAM, SpinRAM, Array	Yang	2008-114685	4/24/2008	7/19/2013	O	O
11	[illegible]	A Novel SyAF Structure To Fabricate Mbit MTJ MRAM	Horng	2008-[illegible]	2/10/2008	1/15/2014	O	O
12	[illegible]	A High Performance MTJ Element for STT-RAM And Method For Making the Same	Horng	2008-190028	7/23/2008	8/21/2013	O	O
13	[illegible]	Method Of Magnetic Tunneling Layer Processes For Spin-Transfer Torque MRAM Devices	Zhong	2008-286048	10/17/2008	5/6/2014	O	O
14	[illegible]	Spin Transfer MRAM Device with Separated CPP Assisted Writing	Guo	2010-334684	5/21/2010	1/24/2014	O	O
15	[illegible]	A Low Switching Current MTJ Element For Ultra-High STT-RAM and Method For Making The Same	Horng	2009-48227	4/8/2009	12/13/2013	O	O
16	[illegible]	Boosted Gate Voltage Programming for Spin-RAM Array	Hsu	2011-637409	5/20/2011	7/8/2014	O	
17	[illegible]	Gate Drive Voltage Boost Schemes For Memory Array	Yang	2010-154047	7/6/2010	3/7/2014	O	O
18	[illegible]	STT-RAM with A Magnetic Tunnel Junction Written in Thermally Assisted Method	Horng	2010-[illegible]	7/20/2010	7/2/2013	O	O
19	[illegible]	A Read Disturb Free SMT MRAM Reference Cell Circuit	Yang	2012-551677	8/5/2012	1/8/2015	O	O
20	[illegible]	Magnetic Element with Improved Out-of-Plane Anisotropy for Spintronic Applications	Jan	2013-[illegible]	9/8/2013	4/24/2015	O	
21	[illegible]	MAGNETIC MEMORY STRUCTURE AND TUNNEL MAGNETORESISTANCE EFFECT REPRODUCTION HEAD AND MANUFACTURING METHOD THEREFOR	Hong	2012-332207	10/16/2012	1/8/2015	O	O
22	[illegible]	MRAM Cell With Flat Topography and Controlled Bit Line to Free Layer Distance and Method of Manufact	Han	2004-[illegible]	12/2/2004	8/6/2010	O	O
23	[illegible]	A Novel Buffer (Seed) Layer for Making a High-Performance Magnetic Tunneling Junction MRAM	Horng	2011-041735	2/28/2011	10/4/2013		
24	[illegible]	Adaptive Algorithm for MRAM Manufacturing	Yang	2010-186793	7/23/2010	1/18/2013	O	O
25	[illegible]	Adaptive Algorithm for MRAM Manufacturing	Yang	2010-189753	7/28/2010	1/18/2013	O	O
26	[illegible]	A Novel Underlayer For High Performance Magnetic Tunneling Junction MRAM	Horng	2005-[illegible]	[illegible]	12/14/2012	O	O
27	[illegible]	Method of Fabricating MRAM Cell Structure Containing Sidewall Spacers	Yang	2008-112850	4/14/2008	7/12/2012	O	O

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1	Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	IBM	Rasmus
2	1793433	Spacer Structure in MRAM Cell And Method Of Fabricating The Same	Yuan	06292015.1	2006/11/7	2013/1/16	O	O
3	EP1901310	A Configurable MRAM	Yang	[illegible]	[illegible]	[illegible]	O	O
4		A Novel Oxidation Structure/Method To Form MgO/NiFe(free layer)-MTJ for high performance MRAM, spell	Horng	06080019.3	2006/12/30		O	O
5	EP1885006	Paramagnetic-NiFeHf Capping Layer to Deposited By Co-Sputtering of NiFe and Hf	Horng	07392004.3	2007/7/30	2009/1/28	O	O
6	EP1818147	Hafnium Doped Cap and Free Layer for MRAM Device	Horng	07392007.6	2007/5/27	2017/12/13	O	O
7		MRAM with Enhanced Programming Margin	Min	08392002.5	2008/3/27		O	O
8	EP1988106	Spin Torque Switching MRAM, SpinRAM, Array	Yang	08392003.3	2008/3/27	2013/6/17	O	O
9	EP1988130	A Novel SyAF Structure To Fabricate Mbit MTJ MRAM	Horng	08390002.2	2008/3/7	2013/10/2	O	O
10	EP2073285	A High Performance MTJ Element for STT-RAM And Method For Making the Same	Horng	08392010.8	2008/7/3	2015/4/29	O	O
11		Boosted Gate Voltage Programming for Spin-RAM Array	Hsu	09827345.8	2009/10/19		O	O
12		Gate Drive Voltage Boost Schemes for Memory Array II	Yang	10810253.3	2010/7/2		O	O
13		Method and Apparatus for Scrubbing Accumulated Data Errors from a Memory System	Yang	10782437.5	2011/12/28		O	O
14	EP2377128	A Novel Free Layer/Capping Layer for High Performance MRAM MTJ	Horng	10731523.4	2011/7/8	2017/3/27	O	O
15	EP2412003	METHOD OF DOUBLE PATTERNING AND ETCHING MAGNETIC TUNNEL JUNCTION STRUCTURES FOR SPIN-TRANSFER TORQUE MRAM DEVICES	Balan	10728494.4	2011/10/24	2017/10/18	O	O
16		Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines	Yang	11803932.8	2011/6/28		O	O
17		A Read Disturb Free SMT MRAM Reference Cell Circuit	Yang	11740183.8	2012/7/28		O	O
18		A Novel Bit Line Preparation Method in MRAM Fabrication	Guomin	10825330.3	2012/5/20		O	O
19		Replaceable, Precise-Tracking Reference Lines	Pu	11827069.0	2013/4/22		O	O
20		Reference Cell Architectures for Small Memory Array Block Activation	Guenge	11834756.6	2013/6/21		O	
21		Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	13748182	2012/7/30			
22		Co/Ni Multilayers with Improved Out-of-Plane Anisotropy for Magnetic Device Applications	Jan	13748182.8	2013/7/30		O	
23		Magnetic Element with Improved Out-of-Plane Anisotropy for Spintronic Applications	Jan	12744681.8	2012/2/10		O	
24	EP2705518	Multilayers Having Reduced Perpendicular Demagnetizing Field using Moment Dilution for Spintronic Applications	Jan	12778616	2013/4/26	2017/4/19	O	
25	EP3058344	Storage Element for STT MRAM Applications	Kula	13780012	2013/8/13	2018/1/10	O	O
26		Storage Element for STT MRAM Applications	Kula	18150884.1	2018/1/8		O	O
27	EP2820681	High Thermal Stability Reference Structure with Out-of-Plane Anisotropy to Magnetic Device Applications	Wang	13754577	2013/1/24	2017/12/20		
28	EP2834315	Reduction of Capping Layer Resistance Area Product for Magnetic Device Applications	Jan	12772801.4	2013/3/27	2017/11/15		
29	EP2820649	High Thermal Stability Free Layer with High Out-of-Plane Anisotropy for Magnetic Device Applications	Wang	13755626	2013/2/27	2017/11/15		
30	2839841	Free Layer with High Thermal Stability for Magnetic Device Applications by Insertion of a Boron Dusting Layer	Wang	13777520.4	2013/4/17	2018/12/21		
31	EP1834450	Adaptive Algorithm for MRAM Manufacturing	Yang	05820005.4	2005/8/14	2013/4/22	O	O
32	EP1815028	A Novel Underlayer For High Performance Magnetic Tunneling Junction MRAM	Horng	05802007.0	2005/5/14	2013/11/14	O	O

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1	Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	IDR	Renesas
33	EP1607980	A Novel Capping Structure for Enhancing dR/R of the MTJ Device	Horng	05392105.2	2005/6/14	2010/2/24	O	O
34		MTJ Incorporating CoFe/Ni Multilayer Film with Perpendicular Magnetic Anisotropy for MRAM Application	Zhang	10837271	2010/10/26		O	O
35		Improved Seed Layer for Multilayer Magnetic Materials	Jan	13783498.2	2012/10/11			
36		An Adaptive Reference Scheme for magnetic Memory Applications	Jan	13786114.2	2013/10/23			
37		Implementation of One Time Programmable Memory using a MRAM Stack Design	Jan	16715705.7	2016/9/22			
38								
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None

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1	Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	SSK	Remarks
2	[illegible]	Magnetic Random Access Memory Array with Coupled Soft Adjacent Magnetic Layer	Guo	[illegible]	[illegible]	[illegible]	O	O
3	[illegible]	Adaptive Algorithm for MRAM Manufacturing	Yang	[illegible]	[illegible]	[illegible]	O	O
4	[illegible]	Adaptive Algorithm for MRAM Manufacturing	Yang	[illegible]	[illegible]	[illegible]	O	O
5	[illegible]	A Novel Underlayer For High Performance Magnetic Tunneling Junction MRAM	Hong	[illegible]	[illegible]	[illegible]	O	O
6	[illegible]	Adaptive Algorithm for MRAM Manufacturing	Yang	[illegible]	[illegible]	[illegible]	O	O

China

	A	B	C	D	E	F	G
1	Issued Patent Number	Title	First Inventor	Serial Number	File Date	Issue Date	Status
2	2649742	Improved Seed Layer for Multilayer Magnetic Materials	Jan	201380061498.2	2013/9/29	2018/3/20	Issued
3		Implementation of One Time Programmable Memory Using a MRAM Stack Design	Jan	201680062700.2	2017/11/15		Pending

Status

Reading Docket Number	Attorney Ref. Number	Title	Filed Country	Applicant	Priority Date	Serial Number	Filing Date	Patent Number	Issue Date	Status
[illegible]		[illegible]		[illegible]	[illegible]	[illegible]	[illegible]			
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]			
[illegible]		[illegible]		[illegible]	[illegible]	[illegible]	[illegible]			

PCT

PCT Applications not yet at National Stage						
	Title	Inventor	Appl No	Filing Date	Docket Number	National Stage Deadline (30 mo)
	MgO Insertion into Free Layer for Magnetic Memory Applications	Iwata	PCT/US2018/016841	2/27/2018	HT2016025PCT	8/27/2019
	Protective Passivation Layer for Magnetic Tunnel Junctions	Iwata	PCT/US2018/020875	2/28/2018	HT2018014PCT	8/29/2019
	Scanning Ferromagnetic Resonance (FMR) for Wafer-Level Characterization of Magnetic Films and Multilayers	Quinsan	PCT/US2018/020381	3/1/2018	HT2018012PCT	8/29/2019
	Spacer Assisted Ion Beam Etching of Spin Torque Magnetic Random Access Memory	Yang	PCT/US2018/020984	3/5/2018	HT2017007PCT	8/22/2019
	Method to Remove Sidewall Damage after MTJ Etching	Yang	PCT/US2018/020854	3/5/2018	HT2017004PCT	8/22/2019
	Maintaining Coercive Field after High Temperature Anneal for Magnetic Device Applications with Perpendicular Magnetic Anisot	Liu	PCT/US2018/021007	3/5/2018	HT2017008PCT	10/3/2019
	MTJ Device Processing/Integration Method with Pre-Patterned Seed Layer	Haq	PCT/US2018/021288	3/7/2018	HT2017001PCT	10/8/2019
	Dielectric Encapsulation Layer for Magnetic Tunnel Junction (MTJ) Devices Using Radio Frequency (RF) Sputtering	Patel	PCT/US2018/021398	3/7/2018	HT2017003PCT	10/8/2019
	Post Treatment to Reduce Shunting Devices for Physical Etching Process	Wang	PCT/US2018/021452	3/8/2018	HT2017002PCT	10/8/2019
	Combined Physical and Chemical Etch to Reduce Magnetic Tunnel Junction (MTJ) Sidewall Damage	Shen	PCT/US2018/032196	5/11/2018	HT2017005PCT	11/15/2019
	Multilayer Structure for Reducing Film Roughness in Magnetic Devices	Zhu	PCT/US2018/032837	5/15/2018	HT2016005DIP_PCT	11/19/2019
	Etch-Less Self-Aligned Magnetic Tunnel Junction (MTJ) Device Structure	Haq	PCT/US2018/035101	5/30/2018	HTS017015PCT	1/18/2020
	Silicon Oxynitride Based Encapsulation Layer for Magnetic Tunnel Junctions	Sundar	PCT/US2018/035097	5/30/2018	HT2017006PCT	12/13/2019
	High Thermal Stability by Dosing of Oxide Capping Layer for Spin Torque Transfer (STT) Magnetic Random Access Memory (MRAM) A	Jan	PCT/US2018/055043	10/9/2018	HT2017034PCT	4/10/2020
	High Temperature Volatilization of Sidewall Materials from Patterned Magnetic Tunnel Junctions	Patel	PCT/US2018/055042	10/9/2018	HT2017010PCT	4/10/2020
	Multiple Hard Mask Patterning to Fabricate 20NM and Below MRAM Devices	Yang	PCT/US2018/056480	10/18/2018	HT2017027PCT	4/23/2020
	Free Layer Sidewall Oxidation and Spacer Assisted Magnetic Tunnel Junction (MTJ) Etch for High Performance Magnetoresistive R	Yang	PCT/US2018/056447	10/18/2018	HTS017030PCT	4/30/2020
	Planarization Process for Magnetic Random Access Memory (MRAM) Production	Lee	PCT/US2018/059603	11/8/2018	HT2017022PCT	5/20/2020
	Improving MTJ Device Performance by Controlling Device Shape	Haq	PCT/US2018/059602	11/8/2018	HT2017023PCT	5/13/2020
	Low Resistance MgO Capping Layer for Perpendicularly Magnetized Magnetic Tunnel Junctions	Patel	PCT/US18/64428	12/7/2018	HT2017014PCT	6/14/2020
	Improved Magnetic Tunnel Junction (MTJ) Performance by Introducing Oxidants to Methanol with or without Noble Gas During MTJ	Shen	PCT/US2018/064429	12/7/2018	HT2017061PCT	6/28/2020
	STT-MRAM Heat Sink and Magnetic Shield Structure Design for More Robust Read/Write Performance	Zhong	PCT/US2018/067551	12/26/2018	HT2017039PCT	6/28/2020
	Ferromagnetic Resonance (FMR) Electrical Testing Apparatus for Spintronic Devices	Ian	PCT/US2019/013563	1/17/2019	HT2017025PCT	7/15/2020
	Nitride Capping Layer for Spin Torque Transfer (STT) Magnetoresistive Random Access Memory (MRAM)	Iwata	PCT/US2019/015129	1/25/2019	HT2017037PCT	7/30/2020