PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6385436

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ACORN TECHNOLOGIES, INC.	05/30/2019

RECEIVING PARTY DATA

Name:	ACORN SEMI, LLC
Street Address:	455 CAMBRIDGE AVE.
City:	PALO ALTO
State/Country:	CALIFORNIA
Postal Code:	94306

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17089429

CORRESPONDENCE DATA

Fax Number: (408)773-6177

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 866-877-4883
Email: patents@ascendalaw.com
Correspondent Name: ASCENDA LAW GROUP
Address Line 1: 2150 N. FIRST STREET
Address Line 2: SUITE 420
Address Line 4: SAN JOSE, CALIFORNIA 95131

ATTORNEY DOCKET NUMBER:	3771-0023-XC2
NAME OF SUBMITTER:	TAREK N. FAHMI
SIGNATURE:	/Tarek N. Fahmi/
DATE SIGNED:	11/04/2020

Total Attachments: 17
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page1.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page2.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page3.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page4.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page5.tif

source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page6.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page7.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page8.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page9.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page10.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page11.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page12.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page13.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page14.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page15.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page16.tif
source=Acorn Assignment Agreement Acorn Semi LLC 05302019 Final & signed_Redacted#page17.tif

ASSIGNMENT AGREEMENT

THIS ASSIGNMENT AGREEMENT ("**Agreement**") is made by and between ACORN TECHNOLOGIES, INC., Delaware corporation ("**Assignor**"), and ACORN SEMI, LLC, a Delaware limited liability company ("**Assignee**"), effective this 30th day of May, 2019 (the "**Effective Date**").

RECITALS

A. WHEREAS, Assignor is the sole owner of certain property pertaining to the Semiconductor business of the Assignor (the "**Semiconductor Business**"), including but not limited to those assets, trade secrets, and intellectual property of as set forth on Exhibit A attached hereto (collectively, the "**Assets**" as that term is defined below); and

B. WHEREAS, Assignor desires to irrevocably transfer all right, title, and interest in and to the Assets to Assignee and Assignee wishes to accept ownership of such Assets.

AGREEMENT

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the parties agree as follows:

1. **Definitions**

1.1 Assets. All Tangible Assets, Contracts, Employees, Intellectual Property and Claims of the Semiconductor Business as further detailed on Exhibit A attached hereto.

1.2 Tangible Assets. All personal tangible property of the Semiconductor Business, including but not limited to personal computers, servers, computer peripherals, zip drives, flash drives, furniture, furnishing, business machines and supplies (hereafter collectively referred to as the "**Tangible Assets**").

1.3 Claims. All claims, refunds, causes of action, choses in action, rights of recovery, rights of set off and rights of recoupment in connection with the Assets.

1.4 Contracts. All right, title and interest in, and all remedies and claims of Assignor under the contracts utilized by or relating to the Semiconductor Business (collectively, the "**Contracts**").

1.5 Employees. All employees of the Semiconductor Business detailed on Exhibit A will be transferred to Assignee.

1.6 Intellectual Property. Any and all of the following of the Semiconductor Business: (a) inventions (whether patentable or unpatentable and whether or not reduced to practice), all improvements thereto, and all patents, patent applications, and patent disclosures, together with all reissuances, continuations, continuations-in-part, revisions, extensions, and reexaminations thereof, (b) all trademarks, service marks, trade dress, logos, slogans, trade names, corporate names, Internet domain names and rights in telephone numbers, together with all translations, adaptations, derivations, and

combinations thereof and including all goodwill associated therewith, and all applications, registrations, and renewals in connection therewith (the "**Trademarks**"), (c) all copyrightable works, all copyrights, and all applications, registrations, and renewals in connection therewith, (d) all mask works and all applications, registrations, and renewals in connection therewith, (e) all trade secrets and confidential business information (including ideas, research and development, know-how, formulas, compositions, manufacturing and production processes and techniques, technical data, designs, drawings, specifications, customer and supplier lists, pricing and cost information, and business and marketing plans and proposals), (f) all computer software (including source code, executable code, data, databases, and related documentation), (g) all web sites, domain names and advertising materials, (h) all other proprietary rights, and (i) all copies and tangible embodiments thereof (in whatever form or medium)(each item hereinafter referred to as the "**Intellectual Property**" and collectively as the "**Intellectual Properties**").

2. **Assignment**

2.1 Assignor hereby irrevocably grants, conveys and assigns to Assignee, by execution hereof (or, where appropriate or required, by execution of separate instruments of assignment), all right, title and interest in and to the Assets, to be held and enjoyed by Assignee, its successors and assigns. Assignee hereby assumes all liabilities and obligations under the Assets.

2.2 Assignor further grants, conveys and assigns to Assignee all right, title and interest in and to any and all causes of action and rights of recovery for past infringement of the Intellectual Property. Assignor will, without demanding any further consideration therefor, at the request and expense of Assignee (except for the value of the time of Assignor employees), do all lawful and just acts, for evidencing, maintaining, recording and perfecting Assignee's rights to said Assets, including but not limited to execution and acknowledgement of assignments and other instruments in a form reasonably required by Assignee.

2.3 The right, title and interest in and to the Assets is to be held and enjoyed by Assignee and Assignee's successors and assigns as fully and exclusively as it would have been held and enjoyed by the Assignor had this assignment not been made.

3. **Consideration.** In full consideration of Assignor's assignment of the Assets to Assignee and the promises and covenants made herein, Assignor will receive one hundred percent (100%) of the equity ownership of Assignee thereby making Assignee a wholly-owned subsidiary of Assignor.

4. **Representations and Warranties.** Assignor hereby expressly represents and warrants that:

4.1 Assignor exclusively owns all right, title and interest in and to the Assets.

4.2 Assignor has not granted any license to the Intellectual Property and is under no obligation to grant any such license to any third party.

4.3 There are no outstanding liens, encumbrances, agreements or understandings of any kind, either written, oral or implied, without encumbrance or threat of future interference by others claiming ownership therein and that no security interests to any third party exists therein and that there is no other

agreement the contrary regarding the Assets that may be inconsistent or in conflict with any provision of this Agreement.

4.4 Assignor has not received and is not aware of any third party claims that Intellectual Property infringes any proprietary rights of such third party.

5. Miscellaneous

5.1 This Agreement and that certain Patent Assignment Agreement entered into between the parties contemporaneously herewith constitutes the entire agreement between the parties regarding the subject matter hereof, and supersedes all prior or contemporaneous understandings or agreements, whether oral or written.

5.2 This Agreement shall be modified or amended only by a writing signed by each of Assignor and Assignee.

5.3 The headings of the paragraphs are for convenience of reference only and are not intended to be part of, or to affect the meaning or interpretation of, this Agreement.

5.4 This Agreement may be executed in two or more counterparts, either by original signature or facsimile, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument.

5.5 Any signature page delivered by a fax machine or email shall be binding to the same extent as an original signature page, with regard to any agreement subject to the terms hereof or any amendment thereto. Any Party who delivers such a signature page agrees to later deliver an original counterpart to any Party that so requests.

5.6 The failure of a Party to enforce any of its rights hereunder or at law shall not be deemed a waiver or a continuing waiver of any of its rights or remedies against the other Party, unless such waiver is in writing and signed by the Party to be charged.

5.7 Assignee recognizes and agrees that Assignor may not have an adequate remedy at law in that injunctive relief, in addition to any other appropriate relief, may therefore be obtained by Assignor.

5.8 Nothing in this Agreement, expressed or implied gives any person, other than Assignor and Assignee any right, remedy, claim under, or by reason of, this Agreement. Any covenants, stipulations, promises or agreements in this Agreement contained by or on behalf of Assignor and Assignee shall be for the sole and exclusive benefit of Assignor and Assignee.

5.9 Each party's execution and delivery of, and performance of its obligations under, this Agreement: (i) are within the power and authority of each party; and (ii) have been duly authorized by all requisite corporate proceedings on the part of the party (if any).

[SIGNATURE PAGE FOLLOWS]

IN WITNESS WHEREOF, the Parties have signed and executed this Assignment Agreement and have caused this Assignment Agreement to become effective as of the Effective Date.

ACORN TECHNOLOGIES, INC.

By: Tom Horgan
Its: C.E.O.
Date: 05/30/2019

ACORN SEMI, LLC

By: Tom Horgan
Its: C.E.O.
Date: 05/30/2019

EXHIBIT A

PATENTS

Patent Description	Registration No.	Issue Date
ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR	6,198,113	06-Mar-2001
ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR	7,615,402	10-Nov-2009
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	DE60034328.6	11-Apr-2007
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	EP1173896	11-Apr-2007
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	GB1173896	11-Apr-2007
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	7,084,423	01-Aug-2006
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,462,860	09-Dec-2008
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	CN100530682	19-Aug-2009
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,884,003	08-Feb-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	10,090,395	02-Oct-2018

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	10,186,592	22-Jan-2019
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	8,431,469	30-Apr-2013
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,425,277	23-Aug-2016
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	8,766,336	01-Jul-2014
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,209,261	08-Dec-2015
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,905,691	27-Feb-2018
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,461,167	04-Oct-2016
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,812,542	07-Nov-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	DE60350090.0	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	EP1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	GB1543561	05-Apr-2017

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	IE1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	JP4847699	21-Oct-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	KR10-1025378	21-Mar-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	NL1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	TW I327376	11-Jul-2010
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,176,483	13-Feb-2007
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	TW I286343	01-Sep-2007
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	6,833,556	21-Dec-2004
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	CN100557816	04-Nov-2009
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	7,112,478	26-Sep-2006
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	7,883,980	08-Feb-2011

INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	8,377,767	19-Feb-2013
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	8,916,437	23-Dec-2014
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	9,583,614	28-Feb-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	JP4713884	01-Apr-2011
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	KR10-1018103	21-Feb-2011
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	TW I310608	01-Jun-2009
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	6,891,234	10-May-2005
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	DE602004046314.0	10-Dec-2014
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	EP1709689	10-Dec-2014
INSULATED GATE FIELD-EFFECT TRANSISTOR HAVING III-VI SOURCE/DRAIN LAYER(S)	7,382,021	03-Jun-2008
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	7,902,029	08-Mar-2011

PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	8,263,467	11-Sep-2012
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	DE602005030278.6	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	EP1787320	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	FR1787320	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	GB1787320	28-Sep-2011
METHOD FOR MAKING SEMICONDUCTOR INSULATED-GATE FIELD-EFFECT TRANSISTOR HAVING MULTILAYER DEPOSITED METAL SOURCE(S) AND/OR DRAIN(S)	7,816,240	19-Oct-2010
METHOD FOR MAKING SEMICONDUCTOR INSULATED-GATE FIELD-EFFECT TRANSISTOR HAVING MULTILAYER DEPOSITED METAL SOURCE(S) AND/OR DRAIN(S)	8,658,523	25-Feb-2014
CHANNEL STRAIN INDUCED BY STRAINED METAL IN FET SOURCE OR DRAIN	8,263,466	11-Sep-2012
FIELD EFFECT TRANSISTOR SOURCE OR DRAIN WITH A MULTI-FACET SURFACE	8,212,336	03-Jul-2012
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,362,376	07-Jun-2016
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,755,038	05-Sep-2017

IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	CN104170058	08-Aug-2017
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,484,426	01-Nov-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2526951	20-Apr-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2526950	29-Apr-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	KR10-1898027	06-Sep-2018
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2511245	20-Jan-2016
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	8,731,017	20-May-2014
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	9,036,672	19-May-2015
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	9,270,083	23-Feb-2016
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	10,008,827	26-Jun-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	10,193,307	29-Jan-2019

TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	CN102957091	17-Jun-2015
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	CN105047735	12-Apr-2017
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	FR2979037	07-Dec-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	KR1374485	07-Mar-2014
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	8,395,213	12-Mar-2013
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	9,406,798	02-Aug-2016
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	9,673,327	06-Jun-2017
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	10,084,091	25-Sep-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	DE112011102840	18-Feb-2016
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	KR10-1476066	17-Dec-2014
MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	10,147,798	04-Dec-2018

MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	9,620,611	11-Apr-2017
NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	10,170,627	01-Jan-2019
STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	8,450,133	28-May-2013
STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	9,029,686	12-May-2015

PATENT APPLICATIONS

Application Description	Application No.	Application Date
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	EP16156295.4	08-Aug-2003
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	EP16154220.4	08-Aug-2003
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	15/728,002	09-Oct-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	15/418,360	27-Jan-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	EP3785158.1	08-Aug-2003

METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	15/684,707	23-Aug-2017
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	CN201710569473.7	13-Jul-2017
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	DE112012004882.2	18-Oct-2012
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	KR10-2014-7017274	18-Oct-2012
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	TW102116259	07-May-2013
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	16/213,876	07-Dec-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	DE102012025727.9	02-Aug-2012
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	DE102012015309.0	02-Aug-2012
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	FR18 59821	24-Oct-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	16/105,277	20-Aug-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	DE112011106092.0	25-Aug-2011
MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	16/175,637	30-Oct-2018
SOI WAFERS AND DEVICES WITH BURIED STRESSOR	15/655,710	20-Jul-2017
SOI WAFERS AND DEVICES WITH BURIED STRESSOR	16/283,578	22-Feb-2019

NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	16/202,507	28-Nov-2018
NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	PCT/US2017/062296	17-Nov-2017
STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	DE112010002206.2	02-Mar-2010
STRAINED SEMICONDUCTOR-ON-INSULATOR BY DEFORMATION OF BURIED INSULATOR INDUCED BY BURIED STRESSOR	15/877,273	22-Jan-2018
STRAINED SEMICONDUCTOR-ON-INSULATOR BY DEFORMATION OF BURIED INSULATOR INDUCED BY BURIED STRESSOR	PCT/US2018/014740	22-Jan-2018

List of Direct Employees

[redacted]

Leases

[redacted]

Contractors and Contracts List

NDAs