PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
GLOBALFOUNDRIES INC.	05/15/2020

RECEIVING PARTY DATA

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PROPERTY NUMBERS Total: 28

Property Type	Number
Patent Number:	8703620
Patent Number:	10262099
Patent Number:	10217633
Patent Number:	10198550
Patent Number:	10402524
Patent Number:	10261109
Patent Number:	10332745
Patent Number:	10248754
Patent Number:	10431732
Patent Number:	10235492
Patent Number:	10325824
Patent Number:	10354045
Patent Number:	10199261
Patent Number:	10297546
Patent Number:	10192791
Patent Number:	10372871
Patent Number:	10199271
Patent Number:	10276461
Patent Number:	10311201
Patent Number:	10229850

Property Type	Number
Patent Number:	10276374
Patent Number:	10401837
Patent Number:	10386726
Patent Number:	10386715
Patent Number:	10401724
Patent Number:	10373942
Patent Number:	10423078
Patent Number:	10324381

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DATE SIGNED:	11/17/2020

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Patent Assignment and Reservation

For good and valuable consideration, the receipt of which is hereby acknowledged, and subject to the reservations stated in the Patent Assignment Agreement Reference No. PA20200002 between the parties with an Effective Date of March 31, 2020, GLOBALFOUNDRIES Inc., a Cayman Islands corporation, GLOBALFOUNDRIES Dresden Module One LLC & CO. KG, a German corporation, and GLOBALFOUNDRIES SINGAPORE PTE. LTD. (hereinafter collectively "ASSIGNOR"), hereby confirm their grant and assignment on April 10, 2020 to TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED, an entity organized under the laws of the Republic of China ("BUYER"), a corporation having a place of business at Hsinchu, Taiwan (hereinafter "ASSIGNEE"), all of ASSIGNOR's right, title and interest in and to (a) the United States Letters Patents identified in the attached Exhibit A, (b) the non-United States Letters Patents identified in Exhibit B, (c) the United States and non-United States patent applications identified in the attached Exhibit C ("Assigned Patent Applications"), (d) patents issuing from the Assigned Patent Applications, and (e) patents that may reissue from any of the foregoing, (hereinafter, collectively, "ASSIGNED PATENTS"), to have and to hold the same, unto ASSIGNEE for its own use and enjoyment and for the use and enjoyment of its successors and assigns, including but not limited to the right to sue for injunctive relief and all damages for infringement of any of the Assigned Patents accruing on and after the Assignment Date and the right to sue therefore under such Assigned Patents, for the full term or terms of all such ASSIGNED PATENTS, subject to all rights granted under the ASSIGNED PATENTS to third parties prior to said Assignment.

ASSIGNOR hereby reserves and retains, for the benefit of itself and its subsidiaries and its and their successors and assigns, the rights and licenses set forth in the Patent Assignment Agreement between the parties.

IN WITNESS WHEREOF, ASSIGNOR has caused this Patent Assignment and Reservation to be duly signed on its behalf.

GLOBALFOUNDRIES INC.
GLOBALFOUNDRIES Dresden Module One LLC & CO. KG
GLOBALFOUNDRIES SINGAPORE, PTE. LTD.

Signature: _____ Date: May 15, 2020

Name: Adam P. Noah
Title: VP and Chief IP Counsel, GLOBALFOUNDRIES US Inc.

EXHIBIT A

LISTED PATENTS (United States)

Document No.	App Serial No.	File Date	Grant Date	Selected Patent	Title
US10008597	14/505536	10/3/2014	6/26/2018	540	Semiconductor devices with asymmetric halo implantation and method of manufacture
US10062762	14/581857	12/23/2014	8/28/2018	541	Semiconductor devices having low contact resistance and low current leakage
US10066303	14/634535	2/27/2015	9/4/2018	542	Thin NiB or CoB capping layer for non-noble metallic bonding landing pads
US10091909	14/632180	2/26/2015	10/2/2018	543	Method and device for cooling a heat generating component
US10109516	15/164204	5/25/2016	10/23/2018	544	Overhead substrate handling and storage system
US10134903	15/343021	11/3/2016	11/20/2018	545	Vertical slit transistor with optimized AC performance
US10168612	15/375623	12/12/2016	1/1/2019	546	Photomask blank including a thin chromium hardmask
US10170553	15/626241	6/19/2017	1/1/2019	547	Shaped terminals for a bipolar junction transistor
US10191112	15/355256	11/18/2016	1/29/2019	548	Early development of a database of fail signatures for systematic defects in integrated circuit (IC) chips
US10192748	15/297848	10/19/2016	1/29/2019	549	Controlling of etch depth in deep via etching processes and resultant structures
US10192791	15/913547	3/6/2018	1/29/2019	550	Semiconductor devices with robust low-k sidewall spacers and method for producing the same
US10192822	14/623115	2/16/2015	1/29/2019	551	Modified tungsten silicon
US10198550	15/478377	4/4/2017	2/5/2019	552	SRAF insertion with artificial neural network
US10199261	15/653638	7/19/2017	2/5/2019	553	Via and skip via structures
US10199271	15/693651	9/1/2017	2/5/2019	554	Self-aligned metal wire on contact structure and method for forming same
US10217633	15/456757	3/13/2017	2/26/2019	555	Substantially defect-free polysilicon gate arrays
US10229850	15/860231	1/2/2018	3/12/2019	556	Cut-first approach with self-alignment during line patterning

US10229918	15/662594	7/28/2017	3/12/2019	557	Methods of forming semiconductor devices using semi-bidirectional patterning
US10235492	15/617403	6/8/2017	3/19/2019	558	Matching IC design patterns using weighted XOR density
US10241502	15/374453	12/9/2016	3/26/2019	559	Methods of error detection in fabrication processes
US10243047	15/372929	12/8/2016	3/26/2019	560	Active and passive components with deep trench isolation structures
US10245667	15/654130	7/19/2017	4/2/2019	561	Chip joining by induction heating
US10248754	15/602810	5/23/2017	4/2/2019	562	Multi-stage pattern recognition in circuit designs
US10256126	15/272924	9/22/2016	4/9/2019	563	Gas flow process control system and method using crystal microbalance(s)
US10261109	15/597202	5/17/2017	4/16/2019	564	Probe card support insert, container, system and method for storing and transporting one or more probe cards
US10262099	15/444899	2/28/2017	4/16/2019	565	Methodology for model-based self-aligned via awareness in optical proximity correction
US10262905	14/867797	9/28/2015	4/16/2019	566	Simplified multi-threshold voltage scheme for fully depleted SOI MOSFETs
US10276374	15/709730	9/20/2017	4/30/2019	567	Methods for forming fins
US10276390	15/097861	4/13/2016	4/30/2019	568	Method and apparatus for reducing threshold voltage mismatch in an integrated circuit
US10276461	15/665974	8/1/2017	4/30/2019	569	Split probe pad structure and method
US10278306	14/632194	2/26/2015	4/30/2019		Method and device for cooling a heat generating component
US10283407	15/817554	11/20/2017	5/7/2019		Two-dimensional self-aligned super via integration on self-aligned gate contact
US10283423	15/292184	10/13/2016	5/7/2019	570	Test structure macro for monitoring dimensions of deep trench isolation regions and local trench isolation regions
US10289109	15/258217	9/7/2016	5/14/2019	571	Methods of error detection in fabrication processes
US10297546	15/652594	7/18/2017	5/21/2019	572	Interconnect structures for a security application
US10302414	14/852897	9/14/2015	5/28/2019	573	Scatterometry method and system
US10311186	15/096551	4/12/2016	6/4/2019	574	Three-dimensional pattern risk scoring

US10311201	15/670158	8/7/2017	6/4/2019	575	Alignment key design rule check for correct placement of abutting cells in an integrated circuit
US10322493	15/046496	2/18/2016	6/18/2019	576	Chemical mechanical polishing apparatus
US10324381	16/159877	10/15/2018	6/18/2019	577	FinFET cut isolation opening revision to compensate for overlay inaccuracy
US10325808	15/858691	12/29/2017	6/18/2019		Crack prevent and stop for thin glass substrates
US10325824	15/622061	6/13/2017	6/18/2019	578	Methods, apparatus and system for threshold voltage control in FinFET devices
US10325862	15/657666	7/24/2017	6/18/2019	579	Wafer rigidity with reinforcement structure
US10331844	15/290569	10/11/2016	6/25/2019	580	Methods of tuning current ratio in a current mirror for transistors formed with the same FEOL layout and a modified BEOL layout
US10332745	15/597277	5/17/2017	6/25/2019	581	Dummy assist features for pattern support
US10345694	15/658721	7/25/2017	7/9/2019	582	Model-based generation of dummy features
US10347740	15/367366	12/2/2016	7/9/2019	583	Fin structures and multi-Vt scheme based on tapered fin and method to form
US10354045	15/624764	6/16/2017	7/16/2019	584	Modeling 3D physical connectivity into planar 2D domain to identify via redundancy
US10355020	15/180860	6/13/2016	7/16/2019	585	FinFETs having strained channels, and methods of fabricating finFETs having strained channels
US10372871	15/662419	7/28/2017	8/6/2019	586	IC layout post-decomposition mask allocation optimization
US10373942	15/829459	12/1/2017	8/6/2019	587	Logic layout with reduced area and method of making the same
US10379191	15/868248	1/11/2018	8/13/2019	588	Apparatus and method for vector s-parameter measurements
US10381339	15/927422	3/21/2018	8/13/2019	589	Integrated circuits with memory cell test circuits and methods for producing the same
US10381826	15/135585	4/22/2016	8/13/2019	590	Integrated circuit electrostatic discharge protection
US10386714	15/401299	1/9/2017	8/20/2019	591	Creating knowledge base for optical proximity correction to reduce sub-resolution assist feature printing

US10386715	15/730830	10/12/2017	8/20/2019	592	Methodology for post-integration awareness in optical proximity correction
US10386726	15/720182	9/29/2017	8/20/2019	593	Geometry vectorization for mask process correction
US10395955	15/432925	2/15/2017	8/27/2019	594	Method and system for detecting a coolant leak in a dry process chamber wafer chuck
US10396000	14/789476	7/1/2015	8/27/2019		Test structure macro for monitoring dimensions of deep trench isolation regions and local trench isolation regions
US10401724	15/805179	11/7/2017	9/3/2019	595	Pellicle replacement in EUV mask flow
US10401837	15/719680	9/29/2017	9/3/2019	596	Generating risk inventory and common process window for adjustment of manufacturing tool
US10402524	15/588984	5/8/2017	9/3/2019	597	Prediction of process-sensitive geometries with machine learning
US10423078	16/398841	4/30/2019	9/24/2019		FinFET cut isolation opening revision to compensate for overlay inaccuracy
US10431732	15/609621	5/31/2017	10/1/2019	598	Shielded magnetoresistive random access memory devices and methods for fabricating the same
US10460067	15/791210	10/23/2017	10/29/2019	599	Method of patterning target layer
US6258659	09/725412	11/29/2000	7/10/2001	1	Embedded vertical DRAM cells and dual workfunction logic gates
US6335152	09/564408	5/1/2000	1/1/2002	2	Use of RTA furnace for photoresist baking
US6342414	09/734189	12/12/2000	1/29/2002	3	Damascene NiSi metal gate high-k transistor
US6372635	09/776736	2/6/2001	4/16/2002	4	Method for making a slot via filled dual damascene low k interconnect structure without middle stop layer
US6376343	09/812695	3/21/2001	4/23/2002	5	Reduction of metal silicide/silicon interface roughness by dopant implantation processing
US6392432	09/602859	6/26/2000	5/21/2002	6	Automated protection of IC devices from EOS (electro over stress) damage due to an undesired DC transient
US6461878	09/614666	7/12/2000	10/8/2002	7	Feedback control of strip time to reduce post strip critical dimension variation in a transistor gate electrode
US6475874	09/731031	12/7/2000	11/5/2002	8	Damascene NiSi metal gate high-k transistor

US6534224	09/772577	1/30/2001	3/18/2003	9	Phase shift mask and system and method for making the same
US6555397	09/660723	9/13/2000	4/29/2003	10	Dry isotropic removal of inorganic anti-reflective coating after poly gate etching
US6560764	09/624494	7/24/2000	5/6/2003	11	Dynamic pulse width programming of programmable logic devices
US6579788	09/664238	9/18/2000	6/17/2003	12	Method of forming conductive interconnections on an integrated circuit device
US6603206	10/105509	3/26/2002	8/5/2003		Slot via filled dual damascene interconnect structure without middle etch stop layer
US6649426	09/893824	6/28/2001	11/18/2003	13	System and method for active control of spacer deposition
US6656019	09/668142	9/25/2000	12/2/2003	14	Grooved polishing pads and methods of use
US6685548	10/424840	4/29/2003	2/3/2004		Grooved polishing pads and methods of use
US6686668	09/764833	1/17/2001	2/3/2004	15	Structure and method of forming bitline contacts for a vertical DRAM array using a line bitline contact mask
US6703853	09/811501	3/19/2001	3/9/2004	16	Test contact mechanism
US6712681	09/715184	11/20/2000	3/30/2004	17	Polishing pads with polymer filled fibrous web, and methods for fabricating and using same
US6714556	09/618057	7/17/2000	3/30/2004	18	In-band management of a stacked group of switches by a single CPU
US6727534	10/022847	12/20/2001	4/27/2004	19	Electrically programmed MOS transistor source/drain series resistance
US6746822	10/050484	1/16/2002	6/8/2004	20	Use of surface coupling agent to improve adhesion
US6756276	10/335522	12/31/2002	6/29/2004	21	Strained silicon MOSFET having improved source/drain extension dopant diffusion resistance and method for its fabrication
US6791697	10/104675	3/21/2002	9/14/2004	22	Scatterometry structure with embedded ring oscillator, and methods of using same
US6794620	10/039525	11/7/2001	9/21/2004	23	Feedforward temperature control of device under test
US6798028	09/847622	5/2/2001	9/28/2004	24	Field effect transistor with reduced gate delay and method of fabricating the same
US6812159	10/420635	4/22/2003	11/2/2004	25	Method of forming a low leakage dielectric layer providing an increased capacitive coupling
US6815997	09/829160	4/9/2001	11/9/2004	26	Field effect transistor square multiplier

US6818358	10/016439	12/11/2001	11/16/2004		Method of extending the areas of clear field phase shift generation
US6888944	09/777506	2/5/2001	5/3/2005	27	Method for assigning encryption keys
US6905919	10/628913	7/29/2003	6/14/2005	28	Method of forming a partially depleted silicon on insulator (PDSOI) transistor with a pad lock body extension
US6924180	10/361934	2/10/2003	8/2/2005	29	Method of forming a pocket implant region after formation of composite insulator spacers
US6927104	10/662674	9/15/2003	8/9/2005	30	Method of forming double-gated silicon-on-insulator (SOI) transistors with corner rounding
US6947563	09/789451	2/20/2001	9/20/2005		Method for assigning encryption keys
US6957404	10/328112	12/20/2002	10/18/2005	31	Model checking with layered localization reduction
US6967715	10/310759	12/6/2002	11/22/2005	32	Method and apparatus for optical film measurements in a controlled environment
US6982215	09/186388	11/5/1998	1/3/2006	33	N type impurity doping using implantation of P2+ ions or As2+ Ions
US6991890	10/773930	2/6/2004	1/31/2006	34	Negative photoresist composition involving non-crosslinking chemistry
US6995376	10/604204	7/1/2003	2/7/2006	35	Silicon-on-insulator latch-up pulse-radiation detector
US6998682	11/128010	5/12/2005	2/14/2006		Method of forming a partially depleted silicon on insulator (PDSOI) transistor with a pad lock body extension
US7063931	10/753989	1/8/2004	6/20/2006	36	Positive photoresist composition with a polymer including a fluorosulfonamide group and process for its use
US7064074	10/624712	7/22/2003	6/20/2006	37	Technique for forming contacts for buried doped regions in a semiconductor device
US7064409	10/605885	11/4/2003	6/20/2006	38	Structure and programming of laser fuse
US7119401	10/707722	1/7/2004	10/10/2006	39	Tunable semiconductor diodes
US7122439	10/904582	11/17/2004	10/17/2006	40	Method of fabricating a bottle trench and a bottle trench capacitor
US7132896	10/981155	11/4/2004	11/7/2006	41	Circuit for minimizing filter capacitance leakage induced jitter in phase locked loops (PPLs)
US7138701	10/605483	10/2/2003	11/21/2006	42	Electrostatic discharge protection networks for triple well semiconductor devices
US7141854	11/174857	7/5/2005	11/28/2006		Double-gated silicon-on-insulator (SOI) transistors with corner rounding

US7217988	10/709905	6/4/2004	5/15/2007	43	Bipolar transistor with isolation and direct contacts
US7240322	10/907494	4/4/2005	7/3/2007	44	Method of adding fabrication monitors to integrated circuit chips
US7250667	11/306663	1/5/2006	7/31/2007	45	Selectable open circuit and anti-fuse element
US7263716	10/066948	2/4/2002	8/28/2007	46	Remote management mechanism to prevent illegal system commands
US7265018	10/711486	9/21/2004	9/4/2007	47	Method to build self-aligned NPN in advanced BiCMOS technology
US7278083	10/604141	6/27/2003	10/2/2007	48	Method and system for optimized instruction fetch to protect against soft and hard errors
US7294869	11/308541	4/4/2006	11/13/2007	49	Silicon germanium emitter
US7323278	11/687731	3/19/2007	1/29/2008		Method of adding fabrication monitors to integrated circuit chips
US7326610	11/271032	11/10/2005	2/5/2008	50	Process options of forming silicided metal gates for advanced CMOS devices
US7340712	11/142566	6/1/2005	3/4/2008	51	System and method for creating a standard cell library for reduced leakage and improved performance
US7348641	10/711182	8/31/2004	3/25/2008	52	Structure and method of making double-gated self-aligned finFET having gates of different lengths
US7348657	11/425491	6/21/2006	3/25/2008		Electrostatic discharge protection networks for triple well semiconductor devices
US7358035	11/159946	6/23/2005	4/15/2008	53	Topcoat compositions and methods of use thereof
US7365412	11/279434	4/12/2006	4/29/2008	54	Vertical parallel plate capacitor using spacer shaped electrodes and method for fabrication thereof
US7375413	11/420527	5/26/2006	5/20/2008	55	Trench widening without merging
US7378895	10/996312	11/23/2004	5/27/2008	56	On-chip electrically alterable resistor
US7382162	11/181954	7/14/2005	6/3/2008	57	High-density logic techniques with reduced-stack multi-gate field effect transistors
US7384714	10/973526	10/25/2004	6/10/2008	58	Anti-reflective sidewall coated alternating phase shift mask and fabrication method
US7384824	11/362680	2/27/2006	6/10/2008		Structure and programming of laser fuse
US7385257	11/411280	4/26/2006	6/10/2008	59	Hybrid orientation SOI substrates, and method for forming the same
US7387930	11/458120	7/18/2006	6/17/2008		Method of fabricating a bottle trench and a bottle trench capacitor

US7394218	11/240833	10/3/2005	7/1/2008	60	Servo system for a two-dimensional micro-electromechanical system (MEMS)-based scanner and method therefor
US7397081	10/905041	12/13/2004	7/8/2008	61	Sidewall semiconductor transistors
US7402854	11/496120	7/31/2006	7/22/2008	62	Three-dimensional cascaded power distribution in a semiconductor device
US7410090	11/409244	4/21/2006	8/12/2008	63	Conductive bonding material fill techniques
US7419611	11/219095	9/2/2005	9/2/2008	64	Processes and materials for step and flash imprint lithography
US7422983	11/064561	2/24/2005	9/9/2008	65	Ta-TaN selective removal process for integrated device fabrication
US7424691	11/279312	4/11/2006	9/9/2008	66	Method for verifying performance of an array by simulating operation of edge cells in a full array model
US7473593	11/275514	1/11/2006	1/6/2009	67	Semiconductor transistors with expanded top portions of gates
US7485539	11/332564	1/13/2006	2/3/2009	68	Strained semiconductor-on-insulator (sSOI) by a simox method
US7504299	10/597432	1/30/2004	3/17/2009	69	Folded node trench capacitor
US7504301	11/536126	9/28/2006	3/17/2009	70	Stressed field effect transistor and methods for its fabrication
US7514370	11/419217	5/19/2006	4/7/2009	71	Compressive nitride film and method of manufacturing thereof
US7518190	11/308408	3/22/2006	4/14/2009	72	Grounding front-end-of-line structures on a SOI substrate
US7518191	12/173280	7/15/2008	4/14/2009	73	Silicon on insulator devices having body-tied-to-source and methods of making
US7521377	11/329560	1/11/2006	4/21/2009	74	SiCOH film preparation using precursors with built-in porogen functionality
US7521763	11/619357	1/3/2007	4/21/2009	75	Dual stress STI
US7525161	11/669902	1/31/2007	4/28/2009	76	Strained MOS devices using source/drain epitaxy
US7526698	11/277306	3/23/2006	4/28/2009	77	Error detection and correction in semiconductor structures
US7531293	11/445326	6/2/2006	5/12/2009	78	Radiation sensitive self-assembled monolayers and uses thereof
US7531367	11/333997	1/18/2006	5/12/2009	79	Utilizing sidewall spacer features to form magnetic tunnel junctions in an integrated circuit
US7541288	11/683590	3/8/2007	6/2/2009	80	Methods of forming integrated circuit structures using insulator deposition and insulator gap filling techniques

US7541290	11/683648	3/8/2007	6/2/2009	81	Methods of forming mask patterns on semiconductor wafers that compensate for nonuniform center-to-edge etch rates during photolithographic processing
US7545667	11/393270	3/30/2006	6/9/2009	82	Programmable via structure for three dimensional integration technology
US7552413	12/166811	7/2/2008	6/23/2009		System and computer program for verifying performance of an array by simulating operation of edge cells in a full array model
US7556996	11/736622	4/18/2007	7/7/2009	83	Field effect transistor comprising a stressed channel region and method of forming the same
US7560141	12/268562	11/11/2008	7/14/2009	84	Method of positioning patterns from block copolymer self-assembly
US7560798	11/276369	2/27/2006	7/14/2009	85	High performance tapered varactor
US7562284	11/212208	8/26/2005	7/14/2009	86	Apparatus, system, and method for mandatory end to end integrity checking in a storage system
US7566921	11/838941	8/15/2007	7/28/2009		Silicon germanium emitter
US7569475	11/560044	11/15/2006	8/4/2009	87	Interconnect structure having enhanced electromigration reliability and a method of fabricating same
US7572689	11/937637	11/9/2007	8/11/2009	88	Method and structure for reducing induced mechanical stresses
US7575970	11/470809	9/7/2006	8/18/2009	89	Deep trench capacitor through SOI substrate and methods of forming
US7583044	12/141121	6/18/2008	9/1/2009		Servo system for a two-dimensional micro-electromechanical system (MEMS)-based scanner and method therefor
US7583833	11/341701	1/27/2006	9/1/2009	90	Method and apparatus for manufacturing data indexing
US7585759	11/382135	5/8/2006	9/8/2009	91	Technique for efficiently patterning an underbump metallization layer using a dry etch process
US7590901	11/419271	5/19/2006	9/15/2009	92	Apparatus, system, and method for dynamic recovery and restoration from design defects in an integrated circuit
US7591902	11/615080	12/22/2006	9/22/2009	93	Recirculation and reuse of dummy dispensed resist
US7592258	11/619235	1/3/2007	9/22/2009	94	Metallization layer of a semiconductor device having differently thick metal lines and a method of forming the same
US7595247	11/753862	5/25/2007	9/29/2009	95	Halo-first ultra-thin SOI FET for superior short channel control

US7598540	11/451869	6/13/2006	10/6/2009	96	High performance CMOS devices comprising gapped dual stressors with dielectric gap fillers, and methods of fabricating the same
US7600209	11/673298	2/9/2007	10/6/2009	97	Generating constraint preserving testcases in the presence of dead-end constraints
US7601569	11/761568	6/12/2007	10/13/2009	98	Partially depleted SOI field effect transistor having a metallized source side halo region
US7601645	11/872399	10/15/2007	10/13/2009	99	Methods for fabricating device features having small dimensions
US7605447	11/162780	9/22/2005	10/20/2009	100	Highly manufacturable SRAM cells in substrates with hybrid crystal orientation
US7615418	11/380688	4/28/2006	11/10/2009	101	High performance stress-enhance MOSFET and method of manufacture
US7615433	11/304455	12/15/2005	11/10/2009	102	Double anneal with improved reliability for dual contact etch stop liner scheme
US7618755	11/419852	5/23/2006	11/17/2009	103	Method and system for automatically detecting exposed substrates having a high probability for defocused exposure fields
US7618891	11/415922	5/1/2006	11/17/2009	104	Method for forming self-aligned metal silicide contacts
US7622389	11/411353	4/25/2006	11/24/2009	105	Selective contact formation using masking and resist patterning techniques
US7630235	11/692627	3/28/2007	12/8/2009	106	Memory cells, memory devices and integrated circuits incorporating the same
US7633106	11/164072	11/9/2005	12/15/2009	107	Light shield for CMOS imager
US7638424	11/536730	9/29/2006	12/29/2009	108	Technique for non-destructive metal delamination monitoring in semiconductor devices
US7642125	11/855979	9/14/2007	1/5/2010	109	Phase change memory cell in via array with self-aligned, self-converged bottom electrode and method for manufacturing
US7645641	11/781854	7/23/2007	1/12/2010	110	Cooling device with a preformed compliant interface
US7646470	12/013511	1/14/2008	1/12/2010	111	Immersion lithographic process using a variable scan speed
US7649243	11/556833	11/6/2006	1/19/2010	112	Semiconductor structures incorporating multiple crystallographic planes and methods for fabrication thereof

US7651831	12/136163	6/10/2008	1/26/2010		Positive photoresist composition with a polymer including a fluorosulfonamide group and process for its use
US7655388	11/028421	1/3/2005	2/2/2010	113	Mask and method to pattern chromeless phase lithography contact hole
US7655972	11/164378	11/21/2005	2/2/2010	114	Structure and method for MOSFET with reduced extension resistance
US7655983	11/757472	6/4/2007	2/2/2010	115	SOI FET with source-side body doping
US7655994	11/259644	10/26/2005	2/2/2010	116	Low threshold voltage semiconductor device with dual threshold voltage control means
US7657339	11/251604	10/14/2005	2/2/2010	117	Product-related feedback for process control
US7659170	11/620406	1/5/2007	2/9/2010	118	Method of increasing transistor drive current by recessing an isolation trench
US7659174	11/930230	10/31/2007	2/9/2010	119	Method to enhance device performance with selective stress relief
US7659534	11/833354	8/3/2007	2/9/2010	120	Programmable via devices with air gap isolation
US7659599	12/049258	3/14/2008	2/9/2010	121	Patterned silicon-on-insulator layers and methods for forming the same
US7667263	11/672109	2/7/2007	2/23/2010	122	Semiconductor structure including doped silicon carbon liner layer and method for fabrication thereof
US7669748	12/173346	7/15/2008	3/2/2010		Conductive bonding material fill techniques
US7670938	11/381219	5/2/2006	3/2/2010	123	Methods of forming contact openings
US7673173	12/212577	9/17/2008	3/2/2010	124	System and program for transmitting input/output requests from a first controller to a second controller
US7673195	11/866502	10/3/2007	3/2/2010	125	Circuits and methods for characterizing device variation in electronic memory circuits
US7674562	11/297532	12/7/2005	3/9/2010	126	Angled-wedge chrome-face wall for intensity balance of alternating phase shift mask
US7675342	12/060889	4/2/2008	3/9/2010		On-chip electrically alterable resistor
US7682961	11/422979	6/8/2006	3/23/2010	127	Methods of forming solder connections and structure thereof
US7688058	12/212247	9/17/2008	3/30/2010	128	Integrated spectrum analyzer circuits and methods for providing on-chip diagnostics
US7696025	11/867840	10/5/2007	4/13/2010		Sidewall semiconductor transistors

US7696057	11/618974	1/2/2007	4/13/2010	129	Method for co-alignment of mixed optical and electron beam lithographic fabrication levels
US7700377	11/862345	9/27/2007	4/20/2010	130	Method for reducing etch-induced process uniformities by omitting deposition of an endpoint detection layer during patterning of stressed overlayers in a semiconductor device
US7701037	11/831208	7/31/2007	4/20/2010	131	Orientation-independent multi-layer BEOL capacitor
US7718500	11/305584	12/16/2005	5/18/2010	132	Formation of raised source/drain structures in NFET with embedded SiGe in PFET
US7719079	11/624436	1/18/2007	5/18/2010	133	Chip carrier substrate capacitor and method for fabrication thereof
US7724578	11/639865	12/15/2006	5/25/2010	134	Sensing device for floating body cell memory and method thereof
US7727827	11/942400	11/19/2007	6/1/2010	135	Method of forming a semiconductor structure
US7727856	11/615980	12/24/2006	6/1/2010	136	Selective STI stress relaxation through ion implantation
US7728089	12/035462	2/22/2008	6/1/2010		Topcoat compositions and methods of use thereof
US7729161	11/833143	8/2/2007	6/1/2010	137	Phase change memory with dual word lines and source lines and method of operating same
US7732281	11/410695	4/24/2006	6/8/2010	138	Methods for fabricating dual bit flash memory devices
US7732291	11/608591	12/8/2006	6/8/2010	139	Semiconductor device having stressed etch stop layers of different intrinsic stress in combination with PN junctions of different design in different device regions
US7732798	12/178921	7/24/2008	6/8/2010		Programmable via structure for three dimensional integration technology
US7736841	12/233245	9/18/2008	6/15/2010	140	Reflective film interface to restore transverse magnetic wave contrast in lithographic processing
US7737752	11/750267	5/17/2007	6/15/2010	141	Techniques for integrated circuit clock management
US7741191	11/951092	12/5/2007	6/22/2010	142	Method for preventing the formation of electrical shorts via contact ILD voids
US7745320	12/124177	5/21/2008	6/29/2010	143	Method for reducing silicide defects in integrated circuits
US7751924	11/830349	7/30/2007	7/6/2010	144	C4NP servo controlled solder fill head

US7763476	11/672146	2/7/2007	7/27/2010	145	Test structure for determining characteristics of semiconductor alloys in SOI transistors by x-ray diffraction
US7763515	11/843358	8/22/2007	7/27/2010	146	Transistor with embedded silicon/germanium material on a strained semiconductor on insulator substrate
US7764078	11/623372	1/16/2007	7/27/2010	147	Test structure for monitoring leakage currents in a metallization layer
US7772071	11/383951	5/17/2006	8/10/2010	148	Strained channel transistor and method of fabrication thereof
US7776682	11/110165	4/20/2005	8/17/2010	149	Ordered porosity to direct memory element formation
US7781343	11/757575	6/4/2007	8/24/2010	150	Semiconductor substrate having a protection layer at the substrate back side
US7784012	11/849908	9/4/2007	8/24/2010		System and method for creating a standard cell library for use in circuit designs
US7787108	11/856799	9/18/2007	8/31/2010	151	Inline stress evaluation in microstructure devices
US7791057	12/107573	4/22/2008	9/7/2010	152	Memory cell having a buried phase change region and method for fabricating the same
US7795104	12/030598	2/13/2008	9/14/2010	153	Method for fabricating device structures having a variation in electrical conductivity
US7799682	11/697890	4/9/2007	9/21/2010	154	Transistor having a locally provided metal silicide region in contact areas and a method of forming the transistor
US7816274	12/057072	3/27/2008	10/19/2010	155	Methods for normalizing strain in a semiconductor device
US7821098	12/103000	4/15/2008	10/26/2010		Trench widening without merging
US7825460	11/516208	9/6/2006	11/2/2010	156	Vertical field effect transistor arrays and methods for fabrication thereof
US7829965	10/908601	5/18/2005	11/9/2010	157	Touching microlens structure for a pixel sensor and method of fabrication
US7831324	11/746320	5/9/2007	11/9/2010	158	Method and system for randomizing wafers in a complex process line
US7833849	11/323564	12/30/2005	11/16/2010	159	Method of fabricating a semiconductor structure including one device region having a metal gate electrode located atop a thinned polygate electrode
US7834384	12/060922	4/2/2008	11/16/2010	160	Simultaneous conditioning of a plurality of memory cells through series resistors
US7834425	12/115065	5/5/2008	11/16/2010		Hybrid orientation SOI substrates, and method for forming the same

US7838384	11/970665	1/8/2008	11/23/2010	161	Structure for symmetrical capacitor
US7843007	12/539842	8/12/2009	11/30/2010	162	Metal high-k transistor having silicon sidewall for reduced parasitic capacitance
US7844931	12/032728	2/18/2008	11/30/2010	163	Method and computer system for optimizing the signal time behavior of an electronic circuit design
US7846502	12/482583	6/11/2009	12/7/2010		Method of positioning patterns from block copolymer self-assembly
US7847402	11/676522	2/20/2007	12/7/2010	164	BEOL interconnect structures with improved resistance to stress
US7855135	12/539860	8/12/2009	12/21/2010		Method to reduce parastic capacitance in a metal high dielectric constant (MHK) transistor
US7858500	12/062972	4/4/2008	12/28/2010		Low threshold voltage semiconductor device with dual threshold voltage control means
US7859113	11/679483	2/27/2007	12/28/2010	165	Structure including via having refractory metal collar at copper wire and dielectric layer liner-less interface and related method
US7860695	12/173070	7/15/2008	12/28/2010	166	Method of creating a load balanced spatial partitioning of a structured, diffusing system of particles
US7863186	12/334746	12/15/2008	1/4/2011	167	Fully and uniformly silicided gate structure and method for forming same
US7867862	11/855168	9/14/2007	1/11/2011	168	Semiconductor structure including high voltage device
US7875502	12/788521	5/27/2010	1/25/2011	169	Semiconductor chips with crack stop regions for reducing crack propagation from chip edges/corners
US7879732	11/959034	12/18/2007	2/1/2011	170	Thin film etching method and semiconductor device fabrication using same
US7880157	12/544089	8/19/2009	2/1/2011	171	Four-terminal reconfigurable devices
US7880229	11/874454	10/18/2007	2/1/2011	172	Body tie test structure for accurate body effect measurement
US7888780	12/688470	1/15/2010	2/15/2011		Semiconductor structures incorporating multiple crystallographic planes and methods for fabrication thereof
US7897444	12/363239	1/30/2009	3/1/2011		Strained semiconductor-on-insulator (sSOI) by a simox method
US7910450	11/276282	2/22/2006	3/22/2011	173	Method of fabricating a precision buried resistor

US7911001	11/778045	7/15/2007	3/22/2011	174	Methods for forming self-aligned dual stress liners for CMOS semiconductor devices
US7919812	12/554344	9/4/2009	4/5/2011		Partially depleted SOI field effect transistor having a metallized source side halo region
US7932128	11/771854	6/29/2007	4/26/2011	175	Polymeric material, method of forming the polymeric material, and method of forming a thin film using the polymeric material
US7932506	12/177533	7/22/2008	4/26/2011	176	Fully self-aligned pore-type memory cell having diode access device
US7934181	12/130472	5/30/2008	4/26/2011	177	Method and apparatus for improving SRAM cell stability by using boosted word lines
US7935593	12/366356	2/5/2009	5/3/2011	178	Stress optimization in dual embedded epitaxially grown semiconductor processing
US7939417	12/536636	8/6/2009	5/10/2011	179	Bipolar transistor and back-gated transistor structure and method
US7951678	12/190123	8/12/2008	5/31/2011	180	Metal-gate high-k reference structure
US7955936	12/172756	7/14/2008	6/7/2011	181	Semiconductor fabrication process including an SiGe rework method
US7955940	12/551797	9/1/2009	6/7/2011	182	Silicon-on-insulator substrate with built-in substrate junction
US7955950	11/874565	10/18/2007	6/7/2011	183	Semiconductor-on-insulator substrate with a diffusion barrier
US7955958	12/027675	2/7/2008	6/7/2011	184	Method for fabrication of polycrystalline diodes for resistive memories
US7960283	12/825325	6/28/2010	6/14/2011		Method for reducing silicide defects in integrated circuits
US7964497	12/163172	6/27/2008	6/21/2011	185	Structure to facilitate plating into high aspect ratio vias
US7964970	11/964494	12/26/2007	6/21/2011	186	Technique for enhancing transistor performance by transistor specific contact design
US7973409	11/625576	1/22/2007	7/5/2011	187	Hybrid interconnect structure for performance improvement and reliability enhancement
US7977203	12/544964	8/20/2009	7/12/2011		Programmable via devices with air gap isolation
US7978509	12/759479	4/13/2010	7/12/2011		Phase change memory with dual word lines and source lines and method of operating same

US7981748	12/541495	8/14/2009	7/19/2011		Method for fabricating a vertical field effect transistor array comprising a plurality of semiconductor pillars
US7993997	11/865563	10/1/2007	8/9/2011	188	Poly profile engineering to modulate spacer induced stress for device enhancement
US7999320	12/342527	12/23/2008	8/16/2011	189	SOI radio frequency switch with enhanced signal fidelity and electrical isolation
US8003460	12/028895	2/11/2008	8/23/2011	190	Method of forming a semiconductor structure comprising a formation of at least one sidewall spacer structure
US8008744	12/790975	5/31/2010	8/30/2011		Selective STI stress relaxation through ion implantation
US8018312	12/369036	2/11/2009	9/13/2011	191	Inductor and method of operating an inductor by combining primary and secondary coils with coupling structures
US8030635	12/353219	1/13/2009	10/4/2011	192	Polysilicon plug bipolar transistor for phase change memory
US8030687	11/764948	6/19/2007	10/4/2011	193	Field effect transistor incorporating at least one structure for imparting temperature-dependent strain on the channel region and associated method of forming the transistor
US8030971	12/102097	4/14/2008	10/4/2011		High-density logic techniques with reduced-stack multi-gate field effect transistors
US8039338	12/397574	3/4/2009	10/18/2011	194	Method for reducing defects of gate of CMOS devices during cleaning processes by modifying a parasitic PN junction
US8039908	12/616389	11/11/2009	10/18/2011	195	Damascene gate having protected shorting regions
US8053303	13/075552	3/30/2011	11/8/2011	196	SOI body contact using E-DRAM technology
US8053348	12/547537	8/26/2009	11/8/2011	197	Method of forming a semiconductor device using a sacrificial uniform vertical thickness spacer structure
US8053819	12/120899	5/15/2008	11/8/2011		Three-dimensional cascaded power distribution in a semiconductor device
US8054986	12/543306	8/18/2009	11/8/2011	198	Method and apparatus for computer communication using audio signals
US8064247	12/488795	6/22/2009	11/22/2011	199	Rewritable memory device based on segregation/re-absorption
US8086974	12/176536	7/21/2008	12/27/2011	200	Structure for fractional-N phased-lock-loop (PLL) system
US8091614	11/558842	11/10/2006	1/10/2012	201	Air/fluid cooling system

US8098536	12/019240	1/24/2008	1/17/2012	202	Self-repair integrated circuit and repair method
US8110901	12/851232	8/5/2010	2/7/2012		Vertical field effect transistor arrays including gate electrodes annularly surrounding semiconductor pillars
US8115251	11/741898	4/30/2007	2/14/2012	203	Recessed gate channel with low Vt corner
US8119464	12/561638	9/17/2009	2/21/2012	204	Fabrication of semiconductors with high-K/metal gate electrodes
US8125049	12/618830	11/16/2009	2/28/2012	205	MIM capacitor structure in FEOL and related method
US8129256	12/194065	8/19/2008	3/6/2012	206	3D integrated circuit device fabrication with precisely controllable substrate removal
US8129843	12/853354	8/10/2010	3/6/2012	207	Methods to mitigate plasma damage in organosilicate dielectrics using a protective sidewall spacer
US8138072	12/500022	7/9/2009	3/20/2012	208	Semiconductor structures and methods of manufacture
US8138102	12/195524	8/21/2008	3/20/2012	209	Method of placing a semiconducting nanostructure and semiconductor device including the semiconducting nanostructure
US8138607	12/632838	12/8/2009	3/20/2012	210	Metal fill structures for reducing parasitic capacitance
US8143132	12/899333	10/6/2010	3/27/2012	211	Transistor including a high-K metal gate electrode structure formed on the basis of a simplified spacer regime
US8143612	12/621000	11/18/2009	3/27/2012		Phase change memory cell in via array with self-aligned, self-converged bottom electrode and method for manufacturing
US8148214	12/360961	1/28/2009	4/3/2012		Stressed field effect transistor and methods for its fabrication
US8148221	12/581207	10/19/2009	4/3/2012		Double anneal with improved reliability for dual contact etch stop liner scheme
US8158003	12/547874	8/26/2009	4/17/2012	212	Precision peak matching in liquid chromatography-mass spectroscopy
US8158461	12/490872	6/24/2009	4/17/2012	213	Continuously referencing signals over multiple layers in laminate packages
US8159015	12/686403	1/13/2010	4/17/2012	214	Method and structure for forming capacitors and memory devices on semiconductor-on-insulator (SOI) substrates
US8159248	12/542935	8/18/2009	4/17/2012	215	Interposer structures and methods of manufacturing the same

US8164188	12/624065	11/23/2009	4/24/2012		Methods of forming solder connections and structure thereof
US8168449	12/612258	11/4/2009	5/1/2012	216	Template-registered diblock copolymer mask for MRAM device formation
US8170704	12/400174	3/9/2009	5/1/2012	217	Method and system for automatic generation of throughput models for semiconductor tools
US8173331	12/685491	1/11/2010	5/8/2012	218	Method and apparatus for sub-pellicle defect reduction on photomasks
US8173501	12/964136	12/9/2010	5/8/2012	219	Reduced STI topography in high-K metal gate transistors by using a mask after channel semiconductor alloy deposition
US8173541	12/542269	8/17/2009	5/8/2012		Chip carrier substrate including capacitor and method for fabrication thereof
US8174106	11/511815	8/29/2006	5/8/2012	220	Through board stacking of multiple LGA-connected components
US8178386	11/855983	9/14/2007	5/15/2012	221	Phase change memory cell array with self-converged bottom electrode and method for manufacturing
US8185859	11/763781	6/15/2007	5/22/2012	222	System and method to improve chip yield, reliability and performance
US8188786	12/565802	9/24/2009	5/29/2012	223	Modularized three-dimensional capacitor array
US8198190	12/103765	4/16/2008	6/12/2012	224	Semiconductor device and method for patterning vertical contacts and metal lines in a common etch process
US8227333	12/948092	11/17/2010	7/24/2012	225	Ni plating of a BLM edge for Pb-free C4 undercut control
US8231692	12/266329	11/6/2008	7/31/2012	226	Method for manufacturing an electronic device
US8232151	13/167303	6/23/2011	7/31/2012	227	Structure and method for manufacturing asymmetric devices
US8232599	12/683456	1/7/2010	7/31/2012	228	Bulk substrate FET integrated on CMOS SOI
US8232604	12/113510	5/1/2008	7/31/2012	229	Transistor with high-k dielectric sidewall spacer
US8236610	12/471656	5/26/2009	8/7/2012	230	Forming semiconductor chip connections
US8236710	12/899638	10/7/2010	8/7/2012	231	Technique to create a buried plate in embedded dynamic random access memory device
US8237086	12/014959	1/16/2008	8/7/2012	232	Removing material from defective opening in glass mold
US8237144	13/252152	10/3/2011	8/7/2012		Polysilicon plug bipolar transistor for phase change memory

US8241970	12/197459	8/25/2008	8/14/2012	233	CMOS with channel P-FinFET and channel N-FinFET having different crystalline orientations and parallel fins
US8242542	12/644895	12/22/2009	8/14/2012	234	Semiconductor switching device employing a quantum dot structure
US8242591	12/540510	8/13/2009	8/14/2012	235	Electrostatic chucking of an insulator handle substrate
US8247271	12/200352	8/28/2008	8/21/2012	236	Formation of alpha particle shields in chip packaging
US8250515	12/770420	4/29/2010	8/21/2012	237	Clock alias for timing analysis of an integrated circuit design
US8252673	12/643454	12/21/2009	8/28/2012	238	Spin-on formulation and method for stripping an ion implanted photoresist
US8262961	12/055513	3/26/2008	9/11/2012	239	Aromatic vinyl ether based reverse-tone step and flash imprint lithography
US8266556	12/849171	8/3/2010	9/11/2012	240	Fracturing continuous photolithography masks
US8273886	12/199607	8/27/2008	9/25/2012		Radiation sensitive self-assembled monolayers and uses thereof
US8276102	12/718567	3/5/2010	9/25/2012	241	Spatial correlation-based estimation of yield of integrated circuits
US8278745	12/543104	8/18/2009	10/2/2012		Through board stacking of multiple LGA-connected components
US8283623	11/927073	10/29/2007	10/9/2012	242	Robust spectral analyzer for one-dimensional and multi-dimensional data analysis
US8288222	12/582139	10/20/2009	10/16/2012	243	Application of cluster beam implantation for fabricating threshold voltage adjusted FETs
US8288825	12/780962	5/17/2010	10/16/2012		Formation of raised source/drain structures in NFET with embedded SiGe in PFET
US8288923	12/557122	9/10/2009	10/16/2012	244	Piezoelectric based energy supply using independent piezoelectric components
US8293451	12/543003	8/18/2009	10/23/2012	245	Near-infrared absorbing film compositions
US8293546	12/477448	6/3/2009	10/23/2012	246	Integrated circuit system with sub-geometry removal and method of manufacture thereof
US8293606	12/973377	12/20/2010	10/23/2012		Body tie test structure for accurate body effect measurement
US8298882	12/563032	9/18/2009	10/30/2012	247	Metal gate and high-K dielectric devices with PFET channel SiGe
US8299561	12/764244	4/21/2010	10/30/2012	248	Shielding for high-voltage semiconductor-on-insulator devices

US8304301	12/621299	11/18/2009	11/6/2012	249	Implant free extremely thin semiconductor devices
US8309445	12/616861	11/12/2009	11/13/2012	250	Bi-directional self-aligned FET capacitor
US8328892	11/930236	10/31/2007	12/11/2012	251	Solution for forming polishing slurry, polishing slurry and related methods
US8334195	12/556139	9/9/2009	12/18/2012	252	Pixel sensors of multiple pixel size and methods of implant dose control
US8339803	12/630993	12/4/2009	12/25/2012	253	High-speed ceramic modules with hybrid referencing scheme for improved performance and reduced cost
US8343836	13/363944	2/1/2012	1/1/2013		Recessed gate channel with low Vt corner
US8349715	12/696417	1/29/2010	1/8/2013	254	Nanoscale chemical templating with oxygen reactive materials
US8354351	12/610630	11/2/2009	1/15/2013	255	Serial irradiation of a substrate by multiple radiation sources
US8357584	12/615796	11/10/2009	1/22/2013	256	Metal capacitor design for improved reliability and good electrical connection
US8357932	12/731469	3/25/2010	1/22/2013		Test pad structure for reuse of interconnect level masks
US8367485	12/551941	9/1/2009	2/5/2013	257	Embedded silicon germanium n-type filed effect transistor for reduced floating body effect
US8368890	12/707962	2/18/2010	2/5/2013	258	Polarization monitoring reticle design for high numerical aperture lithography systems
US8373239	12/795962	6/8/2010	2/12/2013	259	Structure and method for replacement gate MOSFET with self-aligned contact using sacrificial mandrel dielectric
US8377722	12/703211	2/10/2010	2/19/2013	260	Methods of forming structures with a focused ion beam for use in atomic force probing and structures for use in atomic force probing
US8383443	12/780193	5/14/2010	2/26/2013	261	Non-uniform gate dielectric charge for pixel sensor cells and methods of manufacturing
US8383501	13/185055	7/18/2011	2/26/2013		Vertical field effect transistor arrays and methods for fabrication thereof
US8389300	12/753270	4/2/2010	3/5/2013	262	Controlling ferroelectricity in dielectric films by process induced uniaxial strain
US8395196	12/946915	11/16/2010	3/12/2013	263	Hydrogen barrier liner for ferro-electric random access memory (FRAM) chip
US8410553	12/964753	12/10/2010	4/2/2013		Semiconductor structure including high voltage device

US8413083	12/465431	5/13/2009	4/2/2013	264	Mask system employing substantially circular optical proximity correction target and method of manufacture thereof
US8415236	12/648309	12/29/2009	4/9/2013	265	Methods for reducing loading effects during film formation
US8415748	12/766468	4/23/2010	4/9/2013	266	Use of epitaxial Ni silicide
US8420460	12/055686	3/26/2008	4/16/2013	267	Method, structure and design structure for customizing history effects of SOI circuits
US8420468	13/220753	8/30/2011	4/16/2013		Strain-compensated field effect transistor and associated method of forming the transistor
US8421218	12/983377	1/3/2011	4/16/2013	268	Method for direct heat sink attachment
US8426262	12/862203	8/24/2010	4/23/2013	269	Stress adjustment in stressed dielectric materials of semiconductor devices by stress relaxation based on radiation
US8426278	12/797420	6/9/2010	4/23/2013	270	Semiconductor devices having stressor regions and related fabrication methods
US8426316	12/204412	9/4/2008	4/23/2013		Ta-TaN selective removal process for integrated device fabrication
US8431955	12/840689	7/21/2010	4/30/2013	271	Method and structure for balancing power and performance using fluorine and nitrogen doped substrates
US8435878	12/754917	4/6/2010	5/7/2013	272	Field effect transistor device and fabrication
US8436425	12/915168	10/29/2010	5/7/2013	273	SOI semiconductor device comprising substrate diodes having a topography tolerant contact structure
US8438509	12/621564	11/19/2009	5/7/2013	274	Automated generation of oxide pillar slot shapes in silicon-on-insulator formation technology
US8440561	12/844263	7/27/2010	5/14/2013	275	Three-dimensional semiconductor device comprising an inter-die connection on the basis of functional molecules
US8440579	13/178587	7/8/2011	5/14/2013	276	Re-establishing surface characteristics of sensitive low-k dielectrics in microstructure device by using an in situ surface modification
US8441042	12/561827	9/17/2009	5/14/2013	277	BEOL compatible FET structure
US8444774	12/731369	3/25/2010	5/21/2013	278	Flux composition and process for use thereof
US8445342	12/821507	6/23/2010	5/21/2013	279	Short channel semiconductor devices with reduced halo diffusion

US8445344	12/787461	5/26/2010	5/21/2013	280	Uniform high-k metal gate stacks by adjusting threshold voltage for sophisticated transistors by diffusing a metal species prior to gate patterning
US8445377	13/229250	9/9/2011	5/21/2013	281	Mechanically robust metal/low-k interconnects
US8445378	12/839455	7/20/2010	5/21/2013	282	Method of manufacturing a CMOS device including molecular storage elements in a via level
US8445964	13/349883	1/13/2012	5/21/2013		Fabrication of semiconductors with high-K/metal gate electrodes
US8445967	13/534462	6/27/2012	5/21/2013		Semiconductor switching device employing a quantum dot structure
US8448098	13/453262	4/23/2012	5/21/2013		Fracturing continuous photolithography masks
US8450046	12/392093	2/24/2009	5/28/2013	283	Methods for enhancing photolithography patterning
US8450168	12/823728	6/25/2010	5/28/2013	284	Ferro-electric capacitor modules, methods of manufacture and design structures
US8450172	12/823660	6/25/2010	5/28/2013	285	Non-insulating stressed material layers in a contact level of semiconductor devices
US8450197	12/962968	12/8/2010	5/28/2013	286	Contact elements of a semiconductor device formed by electroless plating and excess material removal with reduced sheer forces
US8450206	12/839026	7/19/2010	5/28/2013	287	Method of forming a semiconductor device including a stress buffer material formed above a low-k metallization system
US8450779	12/719058	3/8/2010	5/28/2013	288	Graphene based three-dimensional integrated circuit device
US8450822	12/564996	9/23/2009	5/28/2013	289	Thick bond pad for chip with cavity package
US8455420	13/535466	6/28/2012	6/4/2013		Spin-on formulation and method for stripping an ion implanted photoresist
US8456006	13/174841	7/1/2011	6/4/2013		Hybrid interconnect structure for performance improvement and reliability enhancement
US8458641	13/031754	2/22/2011	6/4/2013	290	Method, system, and design structure for making voltage environment consistent for reused sub modules in chip design
US8464130	12/330012	12/8/2008	6/11/2013	291	Memory device and method thereof
US8470676	12/350469	1/8/2009	6/25/2013	292	Programmable element, and memory device or logic circuit

US8471340	12/627343	11/30/2009	6/25/2013	293	Silicon-on-insulator (SOI) structure configured for reduced harmonics and method of forming the structure
US8476674	13/010009	1/20/2011	7/2/2013	294	Gate conductor with a diffusion barrier
US8476762	13/463879	5/4/2012	7/2/2013		Ni plating of a BLM edge for Pb-free C4 undercut control
US8481164	12/061283	4/2/2008	7/9/2013	295	Materials having predefined morphologies and methods of formation thereof
US8481374	12/914123	10/28/2010	7/9/2013	296	Semiconductor element comprising a low variation substrate diode
US8481380	12/888828	9/23/2010	7/9/2013	297	Asymmetric wedge JFET, related method and design structure
US8481912	13/614930	9/13/2012	7/9/2013		Robust spectral analyzer for one-dimensional and multi-dimensional data analysis
US8482009	13/093034	4/25/2011	7/9/2013		Silicon-on-insulator substrate with built-in substrate junction
US8482075	13/468270	5/10/2012	7/9/2013		Structure and method for manufacturing asymmetric devices
US8482076	12/560585	9/16/2009	7/9/2013	298	Method and structure for differential silicide and recessed or raised source/drain to improve field effect transistor
US8482101	12/488899	6/22/2009	7/9/2013	299	Bipolar transistor structure and method including emitter-base interface impurity
US8482132	12/575980	10/8/2009	7/9/2013	300	Pad bonding employing a self-aligned plated liner for adhesion enhancement
US8486268	13/406956	2/28/2012	7/16/2013		Precision peak matching in liquid chromatography-mass spectroscopy
US8487696	13/438230	4/3/2012	7/16/2013		Modularized three-dimensional capacitor array
US8490037	13/280853	10/25/2011	7/16/2013	301	Method and apparatus for tracking uncertain signals
US8490045	13/354715	1/20/2012	7/16/2013	302	Method and device for selectively adding timing margin in an integrated circuit
US8491739	12/878297	9/9/2010	7/23/2013	303	Implementing interleaved-dielectric joining of multi-layer laminates
US8492199	13/252424	10/4/2011	7/23/2013	304	Reworkable underfills for ceramic MCM C4 protection
US8492234	12/825791	6/29/2010	7/23/2013	305	Field effect transistor device
US8492265	13/431254	3/27/2012	7/23/2013		Pad bonding employing a self-aligned plated liner for adhesion enhancement
US8492270	12/885665	9/20/2010	7/23/2013	306	Structure for nano-scale metallization and method for fabricating same

US8492279	13/164899	6/21/2011	7/23/2013	307	Method of controlling critical dimensions of vias in a metallization system of a semiconductor device during silicon-ARC etch
US8492816	12/685156	1/11/2010	7/23/2013	308	Deep trench decoupling capacitor
US8492823	12/473627	5/28/2009	7/23/2013		High performance tapered varactor
US8492848	13/432716	3/28/2012	7/23/2013		Application of cluster beam implantation for fabricating threshold voltage adjusted FETs
US8492880	13/078305	4/1/2011	7/23/2013	309	Multilayered low k cap with conformal gap fill and UV stable compressive stress properties
US8492892	12/963139	12/8/2010	7/23/2013	310	Solder bump connections
US8497583	12/964448	12/9/2010	7/30/2013	311	Stress reduction in chip packaging by a stress compensation region formed around the chip
US8501545	12/963134	12/8/2010	8/6/2013	312	Reduction of mechanical stress in metal stacks of sophisticated semiconductor devices during die-substrate soldering by an enhanced cool down regime
US8504186	13/354883	1/20/2012	8/6/2013		Method for automatic generation of throughput models for semiconductor tools
US8504971	13/355099	1/20/2012	8/6/2013		Method and device for selectively adding timing margin in an integrated circuit
US8506770	12/645583	12/23/2009	8/13/2013	313	Electrochemical planarization system comprising enhanced electrolyte flow
US8507346	12/949148	11/18/2010	8/13/2013	314	Method of forming a semiconductor device having a cut-way hole to expose a portion of a hardmask layer
US8507953	12/956291	11/30/2010	8/13/2013	315	Body controlled double channel transistor and circuits comprising the same
US8507962	12/897230	10/4/2010	8/13/2013	316	Isolation structures for global shutter imager pixel, methods of manufacture and design structures
US8508053	12/964359	12/9/2010	8/13/2013	317	Chip package including multiple sections for reducing chip package interaction
US8512849	11/836253	8/9/2007	8/20/2013	318	Corrugated interfaces for multilayered interconnects
US8513084	12/967268	12/14/2010	8/20/2013	319	Transistor structure with a sidewall-defined intrinsic base to extrinsic base link-up region and method of forming the transistor

US8513109	13/052956	3/21/2011	8/20/2013	320	Method of manufacturing an interconnect structure for a semiconductor device
US8513117	13/296444	11/15/2011	8/20/2013	321	Process to remove Ni and Pt residues for NiPtSi applications
US8513122	13/759146	2/5/2013	8/20/2013		Method and structure for differential silicide and recessed or raised source/drain to improve field effect transistor
US8513739	13/103197	5/9/2011	8/20/2013		Metal-gate high-k reference structure
US8513769	12/765275	4/22/2010	8/20/2013	322	Electrical fuses and resistors having sublithographic dimensions
US8515567	11/313594	12/21/2005	8/20/2013	323	Enhanced state estimation based upon information credibility
US8518720	12/854995	8/12/2010	8/27/2013	324	UV irradiance monitoring in semiconductor processing using a temperature dependent signal
US8518765	13/489244	6/5/2012	8/27/2013	325	Aqua regia and hydrogen peroxide HCl combination to remove Ni and NiPt residues
US8518766	13/536366	6/28/2012	8/27/2013	326	Method of forming switching device having a molybdenum oxynitride metal gate
US8518782	12/963054	12/8/2010	8/27/2013	327	Semiconductor device including asymmetric lightly doped drain (LDD) region, related method and design structure
US8518784	12/648744	12/29/2009	8/27/2013	328	Adjusting of strain caused in a transistor channel by semiconductor material provided for threshold adjustment
US8519260	12/832375	7/8/2010	8/27/2013	329	Method to evaluate effectiveness of substrate cleanness and quantity of pin holes in an antireflective coating of a solar cell
US8519445	13/182455	7/14/2011	8/27/2013		Poly profile engineering to modulate spacer induced stress for device enhancement
US8519497	13/396998	2/15/2012	8/27/2013		Template-registered diblock copolymer mask for MRAM device formation
US8522173	13/590300	8/21/2012	8/27/2013		Spatial correlation-based estimation of yield of integrated circuits
US8529779	12/057565	3/28/2008	9/10/2013	330	Methods for forming surface features using self-assembling masks
US8530310	12/650561	12/31/2009	9/10/2013	331	Memory cell with improved retention
US8533344	11/653975	1/17/2007	9/10/2013	332	Live connection enhancement for data source interface

US8535991	12/688254	1/15/2010	9/17/2013	333	Methods and systems involving electrically reprogrammable fuses
US8536036	12/905711	10/15/2010	9/17/2013	334	Predoped semiconductor material for a high-K metal gate electrode structure of P- and N-channel transistors
US8536041	13/559182	7/26/2012	9/17/2013		Method for fabricating transistor with high-K dielectric sidewall spacer
US8536069	13/612159	9/12/2012	9/17/2013		Multilayered low k cap with conformal gap fill and UV stable compressive stress properties
US8540890	13/675442	11/13/2012	9/24/2013	335	Protective treatment for porous materials
US8541273	12/888434	9/23/2010	9/24/2013	336	Dielectric stack
US8541842	13/442087	4/9/2012	9/24/2013	337	High-k transistors with low threshold voltage
US8541885	13/107515	5/13/2011	9/24/2013		Technique for enhancing transistor performance by transistor specific contact design
US8542058	12/983352	1/3/2011	9/24/2013	338	Semiconductor device including body connected FETs
US8546062	13/301841	11/22/2011	10/1/2013	339	Self-forming top anti-reflective coating compositions and, photoresist mixtures and method of imaging using same
US8546274	12/835967	7/14/2010	10/1/2013	340	Interlayer dielectric material in a semiconductor device comprising stressed layers with an intermediate buffer material
US8551313	11/940720	11/15/2007	10/8/2013	341	Method and apparatus for electroplating on soi and bulk semiconductor wafers
US8555216	12/100592	4/10/2008	10/8/2013	342	Structure for electrically tunable resistor
US8557693	12/793046	6/3/2010	10/15/2013	343	Contact resistivity reduction in transistor devices by deep level impurity formation
US8558313	13/425681	3/21/2012	10/15/2013		Bulk substrate FET integrated on CMOS SOI
US8558637	12/778130	5/12/2010	10/15/2013	344	Circuit device with signal line transition element
US8563336	12/342430	12/23/2008	10/22/2013	345	Method for forming thin film resistor and terminal bond pad simultaneously
US8563369	13/560340	7/27/2012	10/22/2013		CMOS with channel P-FinFET and channel N-FinFET having different crystalline orientations and parallel fins
US8563398	12/977134	12/23/2010	10/22/2013	346	Electrically conductive path forming below barrier oxide layer and integrated circuit

US8563408	13/535528	6/28/2012	10/22/2013		Spin-on formulation and method for stripping an ion implanted photoresist
US8563446	13/474790	5/18/2012	10/22/2013		Technique to create a buried plate in embedded dynamic random access memory device
US8564066	12/818828	6/18/2010	10/22/2013	347	Interface-free metal gate stack
US8564067	13/772402	2/21/2013	10/22/2013		Silicon-on-insulator (SOI) structure configured for reduced harmonics and method of forming the structure
US8564113	13/444193	4/11/2012	10/22/2013		Electrostatic chucking of an insulator handle substrate
US8566759	12/046750	3/12/2008	10/22/2013	348	Structure for on chip shielding structure for integrated circuits or devices on a substrate
US8569131	12/949888	11/19/2010	10/29/2013	349	Source/drain-to-source/drain recessed strap and methods of manufacture of same
US8569616	13/237386	9/20/2011	10/29/2013	350	Method of concetrating solar energy
US8569803	13/572742	8/13/2012	10/29/2013		BEOL compatible FET structrure
US8572524	11/943591	11/21/2007	10/29/2013	351	Statistical optical proximity correction
US8575008	12/873058	8/31/2010	11/5/2013	352	Post-fabrication self-aligned initialization of integrated devices
US8575655	13/431328	3/27/2012	11/5/2013	353	Method and structure for PMOS devices with high K metal gate integration and SiGe channel engineering
US8575668	13/116416	5/26/2011	11/5/2013	354	Charge breakdown avoidance for MIM elements in SOI base technology and method
US8583796	09/750475	12/28/2000	11/12/2013		Data source interface enhanced error recovery
US8585465	12/969969	12/16/2010	11/19/2013	355	Planarization of a material system in a semiconductor device by using a non-selective in situ prepared slurry
US8586283	13/608409	9/10/2012	11/19/2013		Near-infrared absorbing film compositions
US8586960	12/142239	6/19/2008	11/19/2013	356	Integrated circuit including vertical diode
US8586971	13/050519	3/17/2011	11/19/2013		Polymeric material, method of forming the polymeric material, and method of forming a thin film using the polymeric material
US8587288	12/823984	6/25/2010	11/19/2013	357	Digital interface for fast, inline, statistical characterization of process, MOS device and circuit variations
US8589832	11/844397	8/24/2007	11/19/2013	358	On chip shielding structure for integrated circuits or devices on a substrate and method of shielding

US8589843	13/355065	1/20/2012	11/19/2013		Method and device for selectively adding timing margin in an integrated circuit
US8595919	13/095973	4/28/2011	12/3/2013	359	Silicon chicklet pedestal
US8597991	13/568689	8/7/2012	12/3/2013		Embedded silicon germanium n-type filed effect transistor for reduced floating body effect
US8597993	12/048461	3/14/2008	12/3/2013	360	Electrostatic discharge (ESD) device and method of fabricating
US8598027	12/690467	1/20/2010	12/3/2013		High-K transistors with low threshold voltage
US8599642	12/822021	6/23/2010	12/3/2013	361	Port enable signal generation for gating a memory array device output
US8603303	12/723842	3/15/2010	12/10/2013	362	Nanopore based device for cutting long DNA molecules into fragments
US8603894	13/423716	3/19/2012	12/10/2013	363	Stressed source/drain CMOS and method for forming same
US8603895	13/610263	9/11/2012	12/10/2013	364	Methods of forming isolation structures for semiconductor devices by performing a deposition-etch-deposition sequence
US8604337	13/604230	9/5/2012	12/10/2013		Method to evaluate effectiveness of substrate cleanness and quantity of pin holes in an antireflective coating of a solar cell
US8604559	13/077216	3/31/2011	12/10/2013		Method of placing a semiconducting nanostructure and semiconductor device including the semiconducting nanostructure
US8609498	13/006148	1/13/2011	12/17/2013	365	Transistor with embedded Si/Ge material having reduced offset and superior uniformity
US8609505	13/359032	1/26/2012	12/17/2013		Method of forming MIM capacitor structure in FEOL
US8609524	12/894469	9/30/2010	12/17/2013	366	Method for making semiconductor device comprising replacement gate electrode structures with an enhanced diffusion barrier
US8610185	13/736505	1/8/2013	12/17/2013		Non-uniform gate dielectric charge for pixel sensor cells and methods of manufacturing
US8612904	13/682771	11/21/2012	12/17/2013	367	Use of polarization and composite illumination source for advanced optical lithography
US8617786	13/026168	2/11/2011	12/31/2013	368	Poly-oxycarbosilane compositions for use in imprint lithography

US8618581	13/365577	2/3/2012	12/31/2013	369	Nanofludic field effect transistor based on surface charge modulated nanochannel
US8618617	13/783526	3/4/2013	12/31/2013		Field effect transistor device
US8618663	11/858636	9/20/2007	12/31/2013	370	Patternable dielectric film structure with improved lithography and method of fabricating same
US8624204	13/658861	10/24/2012	1/7/2014		Serial irradiation of a substrate by multiple radiation sources
US8624395	13/400900	2/21/2012	1/7/2014	371	Redundancy design with electro-migration immunity and method of manufacture
US8626328	13/012179	1/24/2011	1/7/2014	372	Discrete sampling based nonlinear control system
US8629010	13/278552	10/21/2011	1/14/2014	373	Carbon nanotube transistor employing embedded electrodes
US8629501	13/370898	2/10/2012	1/14/2014	374	Stress-generating structure for semiconductor-on-insulator devices
US8629553	13/398505	2/16/2012	1/14/2014		3D integrated circuit device fabrication with precisely controllable substrate removal
US8633096	12/943987	11/11/2010	1/21/2014	375	Creating anisotropically diffused junctions in field effect transistor devices
US8633117	13/671186	11/7/2012	1/21/2014	376	Sputter and surface modification etch processing for metal patterning in integrated circuits
US8633633	13/570692	8/9/2012	1/21/2014		Piezoelectric based energy supply using independent piezoelectric components
US8634063	12/637048	12/14/2009	1/21/2014	377	Wafer with design printed outside active region and spaced by design tolerance of reticle blind
US8635483	13/079842	4/5/2011	1/21/2014	378	Dynamically tune power proxy architectures
US8635575	13/471627	5/15/2012	1/21/2014		System and method to improve chip yield, reliability and performance
US8636917	12/876518	9/7/2010	1/28/2014		Solution for forming polishing slurry, polishing slurry and related methods
US8637602	12/335575	12/16/2008	1/28/2014	379	Stabilization of vinyl ether materials
US8637844	13/097307	4/29/2011	1/28/2014		Method for fabrication of crystalline diodes for resistive memories
US8637871	12/939462	11/4/2010	1/28/2014	380	Asymmetric hetero-structure FET and method of manufacture
US8640076	12/906707	10/18/2010	1/28/2014	381	Methodology on developing metal fill as library device and design structure

US8641877	13/570470	8/9/2012	2/4/2014		Nanopore based device for cutting long DNA molecules into fragments
US8642420	13/219331	8/26/2011	2/4/2014	382	Fabrication of a semiconductor device with extended epitaxial semiconductor regions
US8642454	13/475503	5/18/2012	2/4/2014	383	Low temperature selective epitaxy of silicon germanium alloys employing cyclic deposit and etch
US8643401	12/432162	4/29/2009	2/4/2014	384	Integrated circuit communication system with differential signal and method of manufacture thereof
US8647945	12/959824	12/3/2010	2/11/2014	385	Method of forming substrate contact for semiconductor on insulator (SOI) substrate
US8647946	12/621527	11/19/2009	2/11/2014	386	Control gate
US8648647	13/922854	6/20/2013	2/11/2014		Determining current of a first FET of body connected FETs
US8652762	13/423838	3/19/2012	2/18/2014	387	Organic graded spin on BARC compositions for high NA lithography
US8652941	13/474090	5/17/2012	2/18/2014	388	Wafer dicing employing edge region underfill removal
US8652969	13/281715	10/26/2011	2/18/2014	389	High aspect ratio and reduced undercut trench etch process for a semiconductor substrate
US8653602	12/880085	9/11/2010	2/18/2014	390	Transistor having replacement metal gate and process for fabricating the same
US8658435	13/748038	1/23/2013	2/25/2014		Hydrogen barrier liner for ferro-electric random access memory (FRAM) chip
US8658461	13/566050	8/3/2012	2/25/2014	391	Self aligned carbide source/drain FET
US8658530	13/612240	9/12/2012	2/25/2014		Method of fabricating an epitaxial Ni silicide film
US8658543	13/368055	2/7/2012	2/25/2014	392	Methods for pFET fabrication using APM solutions
US8660681	13/006522	1/14/2011	2/25/2014	393	Method and system for excursion monitoring in optical lithography processes in micro device fabrication
US8661664	12/838597	7/19/2010	3/4/2014	394	Techniques for forming narrow copper filled vias having improved conductivity
US8664025	13/187076	7/20/2011	3/4/2014	395	Substrate dicing technique for separating semiconductor dies with reduced area consumption
US8664049	12/776879	5/10/2010	3/4/2014	396	Semiconductor element formed in a crystalline substrate material and comprising an embedded in situ doped semiconductor material

US8664711	14/019508	9/5/2013	3/4/2014		Dielectric stack
US8664721	13/569741	8/8/2012	3/4/2014	397	FET with FUSI gate and reduced source/drain contact resistance
US8666529	12/869973	8/27/2010	3/4/2014	398	Controlling non-process of record (POR) process limiting yield (PLY) inspection work
US8668833	12/125030	5/21/2008	3/11/2014	399	Method of forming a nanostructure
US8673723	13/761610	2/7/2013	3/18/2014	400	Methods of forming isolation regions for FinFET semiconductor devices
US8673726	13/762445	2/8/2013	3/18/2014		Transistor structure with a sidewall-defined intrinsic base to extrinsic base link-up region and method of forming the transistor
US8673760	13/925200	6/24/2013	3/18/2014	401	Methods of forming structures on an integrated circuit product
US8673766	13/476692	5/21/2012	3/18/2014	402	Methods of forming copper-based conductive structures by forming a copper-based seed layer having an as-deposited thickness profile and thereafter performing an etching process and electroless copper deposition
US8674456	13/442090	4/9/2012	3/18/2014		High-K transistors with low threshold voltage
US8677613	12/774223	5/20/2010	3/25/2014	403	Enhanced modularity in heterogeneous 3D stacks
US8678271	11/823056	6/26/2007	3/25/2014	404	Method for preventing void formation in a solder joint
US8679708	13/659236	10/24/2012	3/25/2014		Polarization monitoring reticle design for high numerical aperture lithography systems
US8679899	13/226681	9/7/2011	3/25/2014	405	Multipath soldered thermal interface between a chip and its heat sink
US8679906	12/612035	11/4/2009	3/25/2014	406	Asymmetric multi-gated transistor and method for forming
US8680617	12/574126	10/6/2009	3/25/2014	407	Split level shallow trench isolation for area efficient body contacts in SOI MOSFETS
US8680871	13/869662	4/24/2013	3/25/2014	408	Alignment correction system and method of use
US8681254	13/283819	10/28/2011	3/25/2014	409	Methods for enhancing quality of pixel sensor image frames for global shutter imaging
US8681310	12/958678	12/2/2010	3/25/2014	410	Mechanical fixture of pellicle to lithographic photomask
US8683264	13/080773	4/6/2011	3/25/2014	411	Processing execution requests within different computing environments

US8683402	13/676174	11/14/2012	3/25/2014		Clock alias for timing analysis of an integrated circuit design
US8683413	13/621242	9/15/2012	3/25/2014		Method for making high-speed ceramic modules with hybrid referencing scheme for improved performance and reduced cost
US8685806	13/908048	6/3/2013	4/1/2014		Silicon-on-insulator substrate with built-in substrate junction
US8687170	13/414954	3/8/2012	4/1/2014	412	Asymmetric complementary dipole illuminator
US8687445	13/846229	3/18/2013	4/1/2014		Self-repair integrated circuit and repair method
US8691696	13/476860	5/21/2012	4/8/2014	413	Methods for forming an integrated circuit with straightened recess profile
US8692380	13/657797	10/22/2012	4/8/2014		Integrated circuit system with sub-geometry removal and method of manufacture thereof
US8698244	12/634893	12/10/2009	4/15/2014	414	Silicon-on-insulator (SOI) structure configured for reduced harmonics, design structure and method
US8698245	12/967329	12/14/2010	4/15/2014	415	Partially depleted (PD) semiconductor-on-insulator (SOI) field effect transistor (FET) structure with a gate-to-body tunnel current region for threshold voltage (VT) lowering and method of forming the structure
US8703274	12/244067	10/2/2008	4/22/2014	416	Microcavity structure and process
US8703552	13/419624	3/14/2012	4/22/2014		Method and structure for forming capacitors and memory devices on semiconductor-on-insulator (SOI) substrates
US8703620	13/564071	8/1/2012	4/22/2014	417	Methods for PFET fabrication using APM solutions
US8704325	13/611423	9/12/2012	4/22/2014		Pixel sensors of multiple pixel size and methods of implant dose control
US8709882	12/683759	1/7/2010	4/29/2014	418	Method to dynamically tune precision resistance
US8710588	13/595025	8/27/2012	4/29/2014		Implant free extremely thin semiconductor devices
US8712569	12/147489	6/27/2008	4/29/2014	419	System for determining potential lot consolidation during manufacturing
US8713387	13/658148	10/23/2012	4/29/2014	420	Channel marking for chip mark overflow and calibration errors
US8716071	13/775570	2/25/2013	5/6/2014		Methods and systems involving electrically reprogrammable fuses

US8716079	12/891403	9/27/2010	5/6/2014	421	Superior fill conditions in a replacement gate approach by corner rounding based on a sacrificial fill material
US8716102	13/584981	8/14/2012	5/6/2014	422	Methods of forming isolation structures for semiconductor devices by performing a dry chemical removal process
US8716798	12/779100	5/13/2010	5/6/2014	423	Methodology for fabricating isotropically recessed source and drain regions of CMOS transistors
US8716851	13/417879	3/12/2012	5/6/2014		Continuously referencing signals over multiple layers in laminate packages
US8722470	14/046316	10/4/2013	5/13/2014		CMOS with channel p-FinFET and channel n-FinFET having different crystalline orientations and parallel fins
US8722548	12/890051	9/24/2010	5/13/2014	424	Structures and techniques for atomic layer deposition
US8723233	14/046340	10/4/2013	5/13/2014		CMOS with channel P-FinFET and channel N-FinFET having different crystalline orientations and parallel fins
US8725483	13/008935	1/19/2011	5/13/2014	425	Minimizing the maximum required link capacity for three-dimensional interconnect routing
US8735243	11/834641	8/6/2007	5/27/2014	426	FET device with stabilized threshold modifying material
US8736023	13/775369	2/25/2013	5/27/2014		Field effect transistor device and fabrication
US8736061	13/490840	6/7/2012	5/27/2014	427	Integrated circuits having a continuous active area and methods for fabricating same
US8736816	13/415106	3/8/2012	5/27/2014		Asymmetric complementary dipole illuminator
US8738167	13/398481	2/16/2012	5/27/2014		3D integrated circuit device fabrication with precisely controllable substrate removal
US8739098	13/771478	2/20/2013	5/27/2014	428	EUV mask defect reconstruction and compensation repair
US8741722	13/605136	9/6/2012	6/3/2014	429	Formation of dividers between gate ends of field effect transistor devices
US8741725	12/943084	11/10/2010	6/3/2014	430	Butted SOI junction isolation structures and devices and method of fabrication
US8741730	13/565294	8/2/2012	6/3/2014		Bi-directional self-aligned FET capacitor
US8741770	13/468083	5/10/2012	6/3/2014		Semiconductor device and method for patterning vertical contacts and metal lines in a common etch process

US8741787	12/842548	7/23/2010	6/3/2014	431	Increased density of low-K dielectric materials in semiconductor devices by applying a UV treatment
US8742475	13/554294	7/20/2012	6/3/2014		Field effect transistor device and fabrication
US8743586	13/364759	2/2/2012	6/3/2014	432	Method and structure for ultra-high density, high data rate ferroelectric storage disk technology using stabilization by a surface conducting layer
US8748281	12/907596	10/19/2010	6/10/2014	433	Enhanced confinement of sensitive materials of a high-K metal gate electrode structure
US8749057	13/663836	10/30/2012	6/10/2014		Methods of forming structures with a focused ion beam for use in atomic force probing and structures for use in atomic force probing
US8749760	12/396503	3/3/2009	6/10/2014		Asymmetric complementary dipole illuminator
US8753917	12/967625	12/14/2010	6/17/2014	434	Method of fabricating photoconductor-on-active pixel device
US8753929	13/866162	4/19/2013	6/17/2014		Structure fabrication method
US8754526	13/839020	3/15/2013	6/17/2014		Hybrid interconnect structure for performance improvement and reliability enhancement
US8758962	13/443427	4/10/2012	6/24/2014		Method and apparatus for sub-pellicle defect reduction on photomasks
US8759200	13/135031	6/23/2011	6/24/2014	435	Methods and apparatus for selective epitaxy of Si-containing materials and substitutionally doped crystalline Si-containing material
US8759415	13/564812	8/2/2012	6/24/2014		Aromatic vinyl ether based reverse-tone step and flash imprint lithography
US8759894	11/189765	7/27/2005	6/24/2014	436	System and method for reducing cross-coupling noise between charge storage elements in a semiconductor device
US8765542	13/765797	2/13/2013	7/1/2014	437	Methods of forming a semiconductor device while preventing or reducing loss of active area and/or isolation regions
US8765613	13/281688	10/26/2011	7/1/2014	438	High selectivity nitride etch process
US8766257	13/607674	9/8/2012	7/1/2014		Test pad structure for reuse of interconnect level masks
US8767411	13/469487	5/11/2012	7/1/2014		Electronic device with aerogel thermal isolation
US8769464	13/415372	3/8/2012	7/1/2014	439	Metal density aware signal routing

US8772102	13/455616	4/25/2012	7/8/2014	440	Methods of forming self-aligned contacts for a semiconductor device formed using replacement gate techniques
US8772178	11/082156	3/16/2005	7/8/2014	441	Technique for forming a dielectric interlayer above a structure including closely spaced lines
US8772843	13/183549	7/15/2011	7/8/2014	442	Oxide deposition by using a double liner approach for reducing pattern density dependence in sophisticated semiconductor devices
US8775981	13/770287	2/19/2013	7/8/2014	443	Correcting for overexposure due to overlapping exposures in lithography
US8776868	12/550090	8/28/2009	7/15/2014	444	Thermal ground plane for cooling a computer
US8778772	13/348101	1/11/2012	7/15/2014	445	Method of forming transistor with increased gate width
US8778792	13/758386	2/4/2013	7/15/2014		Solder bump connections
US8784966	11/950453	12/5/2007	7/22/2014		Method of forming a material having a predefined morphology
US8785287	12/803754	7/6/2010	7/22/2014	446	Method to tune narrow width effect with raised S/D structure
US8786088	12/966302	12/13/2010	7/22/2014	447	Semiconductor device including ultra low-K (ULK) metallization stacks with reduced chip-package interaction
US8790989	13/905556	5/30/2013	7/29/2014		Modularized three-dimensional capacitor array
US8791372	13/426892	3/22/2012	7/29/2014	448	Reducing impedance discontinuity in packages
US8796041	12/549799	8/28/2009	8/5/2014	449	Pillar-based interconnects for magnetoresistive random access memory
US8796057	13/766952	2/14/2013	8/5/2014		Isolation structures for global shutter imager pixel, methods of manufacture and design structures
US8796596	12/901079	10/8/2010	8/5/2014	450	Heater and memory cell, memory device and recording head including the heater
US8796771	14/053708	10/15/2013	8/5/2014		Creating anisotropically diffused junctions in field effect transistor devices
US8796773	13/539700	7/2/2012	8/5/2014		Metal gate and high-K dielectric devices with PFET channel SiGe
US8796854	13/838956	3/15/2013	8/5/2014		Hybrid interconnect structure for performance improvement and reliability enhancement

US8800952	13/432966	3/28/2012	8/12/2014		Removing material from defective opening in glass mold and related glass mold for injection molded solder
US8802357	13/326404	12/15/2011	8/12/2014	451	Method for using a topcoat composition
US8802360	13/560012	7/27/2012	8/12/2014	452	Reticles for use in forming implant masking layers and methods of forming implant masking layers
US8802497	13/432963	3/28/2012	8/12/2014		Forming semiconductor chip connections
US8803276	14/073119	11/6/2013	8/12/2014		Electrostatic discharge (ESD) device and method of fabricating
US8806445	13/429981	3/26/2012	8/12/2014	453	Thread serialization and disablement tool
US8806740	13/095969	4/28/2011	8/19/2014		Silicon chicklet pedestal
US8808453	11/737447	4/19/2007	8/19/2014	454	System for abating the simultaneous flow of silane and arsine
US8809142	13/453165	4/23/2012	8/19/2014	455	Structure and method to form E-fuse with enhanced current crowding
US8815475	13/735470	1/7/2013	8/26/2014	456	Reticle carrier
US8815729	13/783715	3/4/2013	8/26/2014		Methods of forming structures on an integrated circuit product
US8819860	13/920676	6/18/2013	8/26/2014	457	Device comprising a cantilever and scanning system
US8826095	13/041248	3/4/2011	9/2/2014	458	Method and system for providing an improved store-in cache
US8828521	13/912593	6/7/2013	9/9/2014		Corrugated interfaces for multilayered interconnects
US8828826	14/015531	8/30/2013	9/9/2014	459	Method for manufacturing a transistor device comprising a germanium based channel layer
US8828869	13/852043	3/28/2013	9/9/2014	460	Methods of forming masking layers for use in forming integrated circuit products
US8829612	12/983477	1/3/2011	9/9/2014	461	Method of forming asymmetric spacers and methods of fabricating semiconductor device using asymmetric spacers
US8829645	12/137640	6/12/2008	9/9/2014		Structure and method to form e-fuse with enhanced current crowding
US8835229	13/749745	1/25/2013	9/16/2014	462	Chip identification for organic laminate packaging and methods of manufacture
US8841652	12/627120	11/30/2009	9/23/2014		Self aligned carbide source/drain FET
US8846476	13/766922	2/14/2013	9/30/2014	463	Methods of forming multiple N-type semiconductor devices with different threshold voltages on a semiconductor substrate

US8847404	13/858198	4/8/2013	9/30/2014		Three-dimensional semiconductor device comprising an inter-die connection on the basis of functional molecules
US8859398	12/749890	3/30/2010	10/14/2014	464	Enhancing adhesion of interlayer dielectric materials of semiconductor devices by suppressing silicide formation at the substrate edge
US8860111	13/445194	4/12/2012	10/14/2014		Phase change memory cell array with self-converged bottom electrode and method for manufacturing
US8866257	14/190514	2/26/2014	10/21/2014		System involving electrically reprogrammable fuses
US8871635	13/466895	5/8/2012	10/28/2014	465	Integrated circuits and processes for forming integrated circuits having an embedded electrical interconnect within a substrate
US8872236	13/195155	8/1/2011	10/28/2014	466	Scaling of bipolar transistors
US8877552	13/076192	3/30/2011	11/4/2014	467	Method and apparatus for manufacturing electronic integrated circuit chip
US8877582	13/771294	2/20/2013	11/4/2014	468	Methods of inducing a desired stress in the channel region of a transistor by performing ion implantation/anneal processes on the gate electrode
US8877642	13/756689	2/1/2013	11/4/2014	469	Double-pattern gate formation processing with critical dimension control
US8877645	13/233064	9/15/2011	11/4/2014	470	Integrated circuit structure having selectively formed metal cap
US8878300	14/030048	9/18/2013	11/4/2014	471	Semiconductor device including outwardly extending source and drain silicide contact regions and related methods
US8879221	13/406537	2/28/2012	11/4/2014	472	ESD protection without latch-up
US8883631	13/905271	5/30/2013	11/11/2014	473	Methods of forming conductive structures using a sacrificial material during a metal hard mask removal process
US8884379	12/711322	2/24/2010	11/11/2014	474	Strain engineering in semiconductor devices by using a piezoelectric material
US8884387	13/568670	8/7/2012	11/11/2014		Pillar-based interconnects for magnetoresistive random access memory
US8890112	13/557385	7/25/2012	11/18/2014		Controlling ferroelectricity in dielectric films by process induced uniaxial strain
US8890246	13/596410	8/28/2012	11/18/2014		Shielding for high-voltage semiconductor-on-insulator devices

US8895372	13/557501	7/25/2012	11/25/2014		Graphene based three-dimensional integrated circuit device
US8896138	13/749744	1/25/2013	11/25/2014		Chip identification for organic laminate packaging and methods of manufacture
US8896810	12/649212	12/29/2009	11/25/2014	475	Liquid immersion scanning exposure system using an immersion liquid confined within a lens hood
US8898597	13/835339	3/15/2013	11/25/2014	476	Etch failure prediction based on wafer resist top loss
US8900961	12/907186	10/19/2010	12/2/2014	477	Selective deposition of germanium spacers on nitride
US8906794	13/956844	8/1/2013	12/9/2014	478	Gate silicidation
US8911920	13/840790	3/15/2013	12/16/2014	479	Methods for fabricating EUV masks and methods for fabricating integrated circuits using such EUV masks
US8912102	12/396441	3/2/2009	12/16/2014	480	Laser annealing
US8912567	12/852995	8/9/2010	12/16/2014		Strained channel transistor and method of fabrication thereof
US8916467	13/116396	5/26/2011	12/23/2014		SOI radio frequency switch with enhanced signal fidelity and electrical isolation
US8921190	12/099175	4/8/2008	12/30/2014	481	Field effect transistor and method of manufacture
US8928145	13/533182	6/26/2012	1/6/2015		Formation of alpha particle shields in chip packaging
US8932920	13/904060	5/29/2013	1/13/2015	482	Self-aligned gate electrode diffusion barriers
US8933435	13/727547	12/26/2012	1/13/2015	483	Tunneling transistor
US8936978	12/955388	11/29/2010	1/20/2015	484	Multigate structure formed with electroless metal deposition
US8940608	13/529898	6/21/2012	1/27/2015	485	Methods for fabricating integrated circuits with drift regions and replacement gates
US8962430	13/907237	5/31/2013	2/24/2015	486	Method for the formation of a protective dual liner for a shallow trench isolation structure
US8963225	14/024820	9/12/2013	2/24/2015	487	Band engineered semiconductor device and method for manufacturing thereof
US8969966	13/866077	4/19/2013	3/3/2015	488	Defective P-N junction for backgated fully depleted silicon on insulator MOSFET
US8987103	12/776674	5/10/2010	3/24/2015	489	Multi-step deposition of a spacer material for reducing void formation in a dielectric material of a contact level of a semiconductor device

US8987144	13/198107	8/4/2011	3/24/2015	490	High-K metal gate electrode structures formed by cap layer removal without sacrificial spacer
US8987827	13/907690	5/31/2013	3/24/2015	491	Prevention of faceting in epitaxial source drain transistors
US8993445	13/740343	1/14/2013	3/31/2015	492	Selective removal of gate structure sidewall(s) to facilitate sidewall spacer protection
US9006705	13/914514	6/10/2013	4/14/2015	493	Device with strained layer for quantum well confinement and method for manufacturing thereof
US9006835	14/074905	11/8/2013	4/14/2015		Transistor with embedded Si/Ge material having reduced offset and superior uniformity
US9012277	13/346043	1/9/2012	4/21/2015	494	In situ doping and diffusionless annealing of embedded stressor regions in PMOS and NMOS devices
US9024286	14/087183	11/22/2013	5/5/2015	495	RRAM cell with bottom electrode(s) positioned in a semiconductor substrate
US9029217	14/592412	1/8/2015	5/12/2015		Band engineered semiconductor device and method for manufacturing thereof
US9034746	14/524023	10/27/2014	5/19/2015		Gate silicidation
US9040369	13/752567	1/29/2013	5/26/2015		Structure and method for replacement gate MOSFET with self-aligned contact using sacrificial mandrel dielectric
US9040383	13/772993	2/21/2013	5/26/2015	496	Devices with gate-to-gate isolation structures and methods of manufacture
US9041107	13/833735	3/15/2013	5/26/2015		Devices with gate-to-gate isolation structures and methods of manufacture
US9043438	14/059005	10/21/2013	5/26/2015		Data source interface enhanced error recovery
US9058417	14/457537	8/12/2014	6/16/2015		Thread serialization and disablement tool
US9059017	13/776911	2/26/2013	6/16/2015		Source/drain-to-source/drain recessed strap and methods of manufacture of same
US9059180	13/737611	1/9/2013	6/16/2015		Thick bond pad for chip with cavity package
US9059318	12/551286	8/31/2009	6/16/2015		Stressed source/drain CMOS and method of forming same
US9064702	13/956273	7/31/2013	6/23/2015	497	Method for manufacturing semiconductor devices
US9064794	14/073919	11/7/2013	6/23/2015		Integrated circuit including vertical diode
US9076735	14/092217	11/27/2013	7/7/2015	498	Methods for fabricating integrated circuits using chemical mechanical polishing

US9076810	14/508011	10/7/2014	7/7/2015		Scaling of bipolar transistors
US9087813	14/174804	2/6/2014	7/21/2015		Control gate
US9089080	13/912591	6/7/2013	7/21/2015		Corrugated interfaces for multilayered interconnects
US9099327	13/568839	8/7/2012	8/4/2015		Multigate structure formed with electroless metal deposition
US9105718	14/224384	3/25/2014	8/11/2015		Butted SOI junction isolation structures and devices and method of fabrication
US9105722	14/486108	9/15/2014	8/11/2015	499	Tucked active region without dummy poly for performance boost and variation reduction
US9142640	14/306864	6/17/2014	9/22/2015	500	Containment structure for epitaxial growth in non-planar semiconductor structure
US9166023	13/964009	8/9/2013	10/20/2015	501	Bulk finFET semiconductor-on-nothing integration
US9196475	14/253906	4/16/2014	11/24/2015	502	Methods for fabricating integrated circuits including fluorine incorporation
US9196829	13/833139	3/15/2013	11/24/2015		Post-fabrication self-aligned initialization of integrated devices
US9219037	13/603008	9/4/2012	12/22/2015	503	Low k porous SiCOH dielectric and integration with post film formation treatment
US9219078	13/865795	4/18/2013	12/22/2015		Simplified multi-threshold voltage scheme for fully depleted SOI MOSFETs
US9231045	13/874200	4/30/2013	1/5/2016	504	Methods for fabricating integrated circuits with polycrystalline silicon resistor structures using a replacment gate process flow, and the integrated circuits fabricated thereby
US9245791	14/754190	6/29/2015	1/26/2016	505	Method for fabricating a contact
US9257557	14/282463	5/20/2014	2/9/2016	506	Semiconductor structure with self-aligned wells and multiple channel materials
US9263582	14/502428	9/30/2014	2/16/2016		Strain engineering in semiconductor devices by using a piezoelectric material
US9269710	13/796674	3/12/2013	2/23/2016		Semiconductor devices having stressor regions and related fabrication methods
US9287345	14/013409	8/29/2013	3/15/2016		Semiconductor structure with thin film resistor and terminal bond pad
US9299665	14/519235	10/21/2014	3/29/2016		Formation of alpha particle shields in chip packaging
US9305999	13/778419	2/27/2013	4/5/2016		Stress-generating structure for semiconductor-on-insulator devices
US9312142	14/300705	6/10/2014	4/12/2016		Chemical mechanical polishing method and apparatus

US9324631	13/870411	4/25/2013	4/26/2016		Semiconductor device including a stress buffer material formed above a low-k metallization system
US9324722	14/797757	7/13/2015	4/26/2016	507	Utilization of block-mask and cut-mask for forming metal routing in an IC device
US9337338	14/820938	8/7/2015	5/10/2016		Tucked active region without dummy poly for performance boost and variation reduction
US9343354	13/970124	8/19/2013	5/17/2016		Middle of line structures and methods for fabrication
US9348216	14/261687	4/25/2014	5/24/2016	508	Test pad structure for reuse of interconnect level masks
US9349852	14/520445	10/22/2014	5/24/2016		Method, structure and design structure for customizing history effects of SOI circuits
US9372392	14/325515	7/8/2014	6/21/2016		Reticles for use in forming implant masking layers and methods of forming implant masking layers
US9373507	14/618498	2/10/2015	6/21/2016		Defective P-N junction for backgated fully depleted silicon on insulator mosfet
US9373557	13/535675	6/28/2012	6/21/2016		Enhanced modularity in heterogeneous 3D stacks
US9377251	14/301623	6/11/2014	6/28/2016		Thermal ground plane for cooling a computer
US9379198	14/494699	9/24/2014	6/28/2016		Integrated circuit structure having selectively formed metal cap
US9385019	13/529264	6/21/2012	7/5/2016		Overhead substrate handling and storage system
US9385179	13/765105	2/12/2013	7/5/2016		Deep trench decoupling capacitor and methods of forming
US9390989	13/535694	6/28/2012	7/12/2016		Enhanced modularity in heterogeneous 3D stacks
US9391200	14/308045	6/18/2014	7/12/2016		FinFETs having strained channels, and methods of fabricating finFETs having strained channels
US9392690	14/177530	2/11/2014	7/12/2016		Method and structure to improve the conductivity of narrow copper filled vias
US9397174	14/516623	10/17/2014	7/19/2016		Self-aligned gate electrode diffusion barriers
US9399753	14/574995	12/18/2014	7/26/2016		Aqua regia and hydrogen peroxide HCL combination to remove Ni and NiPt residues
US9406751	14/296818	6/5/2014	8/2/2016	509	Method for making strained semiconductor device and related methods

US9431540	14/288766	5/28/2014	8/30/2016	510	Method for making a semiconductor device with sidewall spacers for confining epitaxial growth
US9478489	14/138881	12/23/2013	10/25/2016		Semiconductor dies with reduced area consumption
US9478600	14/175587	2/7/2014	10/25/2016		Method of forming substrate contact for semiconductor on insulator (SOI) substrate
US9484248	13/219144	8/26/2011	11/1/2016		Patternable dielectric film structure with improved lithography and method of fabricating same
US9502518	14/312418	6/23/2014	11/22/2016	511	Multi-channel gate-all-around FET
US9515180	14/588318	12/31/2014	12/6/2016		Vertical slit transistor with optimized AC performance
US9583625	14/523548	10/24/2014	2/28/2017		Fin structures and multi-Vt scheme based on tapered fin and method to form
US9601565	14/578523	12/22/2014	3/21/2017	512	Zig-zag trench structure to prevent aspect ratio trapping defect escape
US9613855	15/091196	4/5/2016	4/4/2017	513	Methods of forming MIS contact structures on transistor devices in CMOS applications
US9613906	14/311457	6/23/2014	4/4/2017	514	Integrated circuits including modified liners and methods for fabricating the same
US9620380	14/972804	12/17/2015	4/11/2017	515	Methods for fabricating integrated circuits using self-aligned quadruple patterning
US9627272	14/833813	8/24/2015	4/18/2017	516	Patterning scheme to minimize dry/wets strip induced device degradation
US9633911	14/668482	3/25/2015	4/25/2017		Simplified multi-threshold voltage scheme for fully depleted SOI MOSFETs
US9633942	14/939365	11/12/2015	4/25/2017	517	Conductively doped polymer pattern placement error compensation layer
US9633962	14/048483	10/8/2013	4/25/2017	518	Plug via formation with grid features in the passivation layer
US9634142	15/076699	3/22/2016	4/25/2017	519	Method for improving boron diffusion in a germanium-rich fin through germanium concentration reduction in fin S/D regions by thermal mixing
US9639652	14/148234	1/6/2014	5/2/2017	520	Compact model for device/circuit/chip leakage current (IDDQ) calculation including process induced uplift factors
US9640552	14/519596	10/21/2014	5/2/2017	521	Multi-height fin field effect transistors

US9646838	14/293627	6/2/2014	5/9/2017	522	Method of forming a semiconductor structure including silicided and non-silicided circuit elements
US9646962	15/285985	10/5/2016	5/9/2017	523	Low leakage gate controlled vertical electrostatic discharge protection device integration with a planar FinFET
US9647063	14/797945	7/13/2015	5/9/2017		Nanoscale chemical templating with oxygen reactive materials
US9653356	14/822340	8/10/2015	5/16/2017	524	Methods of forming self-aligned device level contact structures
US9653365	15/093888	4/8/2016	5/16/2017	525	Methods for fabricating integrated circuits with low, medium, and/or high voltage transistors on an extremely thin silicon-on-insulator substrate
US9653571	14/739662	6/15/2015	5/16/2017	526	Freestanding spacer having sub-lithographic lateral dimension and method of forming same
US9660020	14/285774	5/23/2014	5/23/2017	527	Integrated circuits with laterally diffused metal oxide semiconductor structures and methods for fabricating the same
US9660083	14/560,255	12/4/2014	5/23/2017	600	LDMOS finFET device and method of manufacture using a trench confined epitaxial growth process
US9673083	14/608729	1/29/2015	6/6/2017	528	Methods of forming fin isolation regions on FinFET semiconductor devices by implantation of an oxidation-retarding material
US9679029	12/942011	11/8/2010	6/13/2017	529	Optimizing storage cloud environments through adaptive statistical modeling
US9685334	15/134917	4/21/2016	6/20/2017	530	Methods of forming semiconductor fin with carbon dopant for diffusion control
US9685370	14/574889	12/18/2014	6/20/2017	531	Titanium tungsten liner used with copper interconnects
US9685529	15/189476	6/22/2016	6/20/2017	532	III-V NFETs including channel barrier layers to reduce band-to-band leakage current
US9691626	15/077384	3/22/2016	6/27/2017	533	Method of forming a pattern for interconnection lines in an integrated circuit wherein the pattern includes gamma and beta block mask portions
US9691664	15/170126	6/1/2016	6/27/2017	534	Dual thick EG oxide integration under aggressive SG fin pitch
US9698262	15/072130	3/16/2016	7/4/2017	535	Vertical fin field-effect semiconductor device

US9740092	14/467489	8/25/2014	8/22/2017		Model-based generation of dummy features
US9748251	15/352102	11/15/2016	8/29/2017		Methods of forming semiconductor devices using semi-bidirectional patterning
US9748352	14/984688	12/30/2015	8/29/2017		Multi-channel gate-all-around FET
US9761539	14/753768	6/29/2015	9/12/2017		Wafer rigidity with reinforcement structure
US9776270	14/043047	10/1/2013	10/3/2017		Chip joining by induction heating
US9786557	15/096818	4/12/2016	10/10/2017	536	Two-dimensional self-aligned super via integration on self-aligned gate contact
US9793168	14/977387	12/21/2015	10/17/2017		Semiconductor structure with self-aligned wells and multiple channel materials
US9818816	13/716693	12/17/2012	11/14/2017		Metal capacitor design for improved reliability and good electrical connection
US9847415	14/523076	10/24/2014	12/19/2017		Field effect transistor and method of manufacture
US9865564	14/624601	2/18/2015	1/9/2018	537	Laser ashing of polyimide for semiconductor manufacturing
US9887133	15/623758	6/15/2017	2/6/2018		Two-dimensional self-aligned super via integration on self-aligned gate contact
US9892971	15/392042	12/28/2016	2/13/2018	538	Crack prevent and stop for thin glass substrates
US9910124	15/015176	2/4/2016	3/6/2018		Apparatus and method for vector s-parameter measurements
US9917087	13/961554	8/7/2013	3/13/2018	539	Integrated circuits with a partially-depleted region formed over a bulk silicon substrate and methods for fabricating the same
US9922883	15/180158	6/13/2016	3/20/2018		Method for making strained semiconductor device and related methods
US9929253	15/178853	6/10/2016	3/27/2018		Method for making a semiconductor device with sidewal spacers for confinig epitaxial growth
US9947532	15/425338	2/6/2017	4/17/2018		Forming zig-zag trench structure to prevent aspect ratio trapping defect escape
US9953872	15/699138	9/8/2017	4/24/2018		Semiconductor structure with self-aligned wells and multiple channel materials
US8146046	12/120701	2008-05-15	3/27/20127		Structures for semiconductor structures with error detection and correction
US8405186	12/817249	2010-06-17	3/26/2013		Transistor structure with a sidewall-defined intrinsic base to extrinsic base link-up region and method of forming the structure

US8815674	14/172135	2014-02-04	8/26/2014		Methods of forming a semiconductor device by performing a wet acid etching process while preventing or reducing loss of active area and/or isolation regions

END OF EXHIBIT A

EXHIBIT B

LISTED PATENTS (Non-US Patents)

Document No.	App Serial Number	Grant Date	Country Code
CN100440480	CN200310118724A	12/3/2008	CN
CN100499130	CN200480032173A	6/10/2009	CN
CN100504796	CN200610109133A	6/24/2009	CN
CN100505275	CN200610143976A	6/24/2009	CN
CN100570884	CN200610001285A	12/16/2009	CN
CN101140931	CN200710146550A	4/6/2011	CN
CN101170106	CN200710181659A	6/2/2010	CN
CN101217143	CN200810002202A	3/2/2011	CN
CN101226914	CN200810002917A	6/2/2010	CN
CN101359649	CN200810144109A	6/23/2010	CN
CN101536176	CN200780032524A	9/21/2011	CN
CN101573791	CN200780049143A	6/15/2011	CN
CN101681666	CN200780046338A	7/23/2014	CN
CN101711411	CN200880016711A	11/6/2013	CN
CN101730939	CN200880013012A	9/26/2012	CN
CN101764092	CN200910221772A	4/17/2013	CN
CN101952964	CN200980103580A	10/3/2012	CN
CN102326059	CN201080008167A	5/21/2014	CN
CN102341755	CN201080010182A	8/6/2014	CN
CN102365735	CN201080013955A	3/19/2014	CN
CN102412131	CN201110291111A	4/8/2015	CN
CN102640290	CN201080054255A	6/17/2015	CN
CN102782856	CN201180011564A	11/25/2015	CN
CN103098200	CN201180043465A	3/9/2016	CN
CN103210493	CN201180053813A	1/6/2016	CN
CN103890918	CN201280052538A	8/31/2016	CN
CN105551959	CN201510696311A	6/18/2019	CN
CN108945717	CN201810473230A	12/7/2018	CN
CN1178430	CN01812866A	12/1/2004	CN
CN1983608	CN200610143972A	5/12/2010	CN
DE102006040764	DE102006040764	11/11/2010	DE
DE102006062036	DE102006062036A	10/5/2017	DE
DE102007004861	DE102007004861	2/18/2010	DE
DE102007020258	DE102007020258A	6/28/2018	DE
DE102007020268	DE102007020268	11/6/2008	DE
DE102007025340	DE102007025340A	12/5/2019	DE
DE102007052049	DE102007052049	5/7/2009	DE
DE102008007029	DE102008007029A	7/3/2014	DE

DE102009021490	DE102009021490A	4/4/2013	DE
DE102009046260	DE102009046260	5/12/2011	DE
DE102009047890	DE102009047890A	2/2/2012	DE
DE102010028459	DE102010028459A	1/11/2018	DE
DE102010030759	DE102010030759A	10/18/2018	DE
DE102010038740	DE102010038740A	8/14/2019	DE
DE112006002918	DE112006002918	9/2/2010	DE
DE112007002306	DE112007002306	9/15/2011	DE
DE112007003085	DE112007003085T	3/26/2015	DE
DE112010001383	DE112010001383T	7/16/2015	DE
DE112011103730	DE112011103730T	6/9/2016	DE
DE112012004143	DE112012004143T	10/24/2019	DE
DE60129605	DE60129605		DE
EP1303381	EP20010950744	3/2/2005	EP
EP1396010	EP20010995964	7/25/2007	EP
EP1456888	EP20020794406	7/21/2010	EP
EP1687851	EP20040810291	8/7/2013	EP
EP1869595	EP20050855609	8/7/2013	EP
EP1946375	EP20060777968	4/1/2009	EP
EP2005340	EP20070727370	12/19/2012	EP
EP2022085	EP20070755161	10/15/2014	EP
EP2089909	EP20070844145	12/10/2014	EP
EP2102907	EP20070855216	5/21/2014	EP
EP2188837	EP20080807504	10/28/2015	EP
EP2313923	EP20090808777	11/21/2018	EP
EP2389359	EP20100756762	12/11/2013	EP
EP2399105	EP20100744347	10/31/2018	EP
EP2449580	EP20100800212	1/6/2016	EP
EP2595182	EP20110189233	9/14/2016	EP
EP2693462	EP20120005685		EP
EP2701198	EP20130170002		EP
EP2704199	EP20120182800		EP
EP2709156	EP20130182639		EP
EP2924727	EP20150155702		EP
EP3312882	EP20160194923		EP
JP2010526437	JP2010506216A		JP
JP6317076	JP2013121060A	4/25/2018	JP
KR101333240	KR20070127680A		KR
KR101341590	KR20080004500A		KR
KR101373733	KR20080014484A	3/14/2014	KR
KR101669227	KR20100010565A		KR
TW200912975	TW97128610A		TW
TW200921835	TW97126841A		TW
TW200925540	TW97133731A		TW

TW200931525	TW97129790A		TW
TW200935558	TW97135597A		TW
TW200949843	TW98100117A		TW
TW201017821	TW98121240A		TW
TW201023342	TW98126324A		TW
TW201028239	TW98133276A		TW
TW201036109	TW98140578A		TW
TW201104360	TW99106001A		TW
TW201115701	TW99115312A		TW
TW201117377	TW99119871A		TW
TW201125027	TW99138150A		TW
TW201130135	TW99132810A		TW
TW201140771	TW99140073A		TW
TW201214526	TW100122054A		TW
TW201235836	TW100140608A		TW
TW201913941	TW107121315A	4/1/2019	TW
TW515909	TW90114022A	1/1/2003	TW
TWI409925	TW97101515A	9/21/2013	TW
TWI445162	TW97110943A	7/11/2014	TW
TWI446402	TW95146808A	7/21/2014	TW
TWI446414	TW96131775A	7/21/2014	TW
TWI446453	TW96135865A	7/21/2014	TW
TWI446720	TW97116739A	7/21/2014	TW
TWI453789	TW95134720A	9/21/2014	TW
TWI462222	TW98139781A	11/21/2014	TW
TWI469324	TW98103173A	1/11/2015	TW
TWI520282	TW99108290A	2/1/2016	TW
TWI533423	TW99125274A	5/11/2016	TW
TWI609428	TW104117399A	12/21/2017	TW
TWI675425	TW106124112	1/16/2019	TW
TWI676041	TW106116865	9/16/2018	TW
TWI676804	TW107116602	1/1/2019	TW
TWI678765	TW106103219A	6/16/2018	TW
TW517290B	TW090130177	1/11/2003	TW
TW529091B	TW091100728	4/21/2003	TW
TWI529809B	TW100121239	4/11/2016	TW

END OF EXHIBIT B

EXHIBIT C

ASSIGNED PATENT APPLICATIONS

US Assigned Patent Applications

None

Non-US Assigned Patent Applications

Document No.	App Serial Number	File Date	Country Code
CN106971953	CN201610876857A	9/30/2016	CN
CN107870197	CN201710525079A	6/30/2017	CN
CN108073674	CN201710780283A	9/1/2017	CN
CN108074799	CN201710840745A	9/18/2017	CN
CN108172544	CN201710985635A	10/20/2017	CN
CN108573864	CN201810204480A	3/13/2018	CN
CN109087889	CN201810579685A	6/7/2018	CN
CN109427742	CN201811009018A	8/31/2018	CN
CN109752920	CN201810889366A	8/7/2018	CN
DE102008023906	DE102008023906	5/16/2008	DE
DE102010003562	DE102010003562	3/31/2010	DE
DE102010029521	DE102010029521	5/31/2010	DE
DE102010029522	DE102010029522	5/31/2010	DE
DE102018207730	DE102018207730A	5/17/2018	DE
DE102018213190	DE102018213190A	8/7/2018	DE
DE102018222234	DE102018222234A	12/19/2018	DE
DE102019201288	DE102019201288A	2/1/2019	DE
DE112008001684T5	20081101684T	2008-06-26	DE
DE112011102131T5	201111102131T	2011-06-23	DE
DE112011101181T5	201111101181T	2011-03-15	DE
EP2545586	EP20110753755	2/4/2011	EP
EP3070737	EP20150159324	3/17/2015	EP
TW201901746	TW107100640	1/8/2018	TW
TW201918802	TW107117233A	5/21/2018	TW
TW201939589	TW107112082A		TW
TW201939669	TW107142967A		TW

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