PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6463984

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
INTEL CORPORATION	11/13/2020

RECEIVING PARTY DATA

Name:	GOOGLE LLC
Street Address:	1600 AMPHITHEATRE PARKWAY
City:	MOUNTAIN VIEW
State/Country:	CALIFORNIA
Postal Code:	94043

PROPERTY NUMBERS Total: 20

Property Type	Number
Application Number:	14916093
Application Number:	15335269
Application Number:	15024714
Application Number:	16108610
Application Number:	16785975
Application Number:	14913173
Application Number:	14517365
PCT Number:	US2011054428
PCT Number:	US2013063186
PCT Number:	US2013076651
PCT Number:	US2014069361
PCT Number:	US2011067226
PCT Number:	US2011067424
PCT Number:	US2013062314
PCT Number:	US2011066134
PCT Number:	US2011066132
PCT Number:	US2011067232
PCT Number:	US2011067223
PCT Number:	US2011067242
PCT Number:	US2011063190

CORRESPONDENCE DATA

Fax Number: (908)654-7866

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: (908) 654-5000

Email: assignment@lernerdavid.com

Correspondent Name: LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP

Address Line 1: 20 COMMERCE DR.

Address Line 4: CRANFORD, NEW JERSEY 07016

ATTORNEY DOCKET NUMBER:	GOOGLE 3.3-3289
NAME OF SUBMITTER:	CINDY CORB
SIGNATURE:	/Cindy Corb/
DATE SIGNED:	12/22/2020

Total Attachments: 14

source=Intel-Google Assignment (003)#page1.tif
source=Intel-Google Assignment (003)#page2.tif
source=Intel-Google Assignment (003)#page3.tif
source=Intel-Google Assignment (003)#page4.tif
source=Intel-Google Assignment (003)#page5.tif
source=Intel-Google Assignment (003)#page6.tif
source=Intel-Google Assignment (003)#page7.tif
source=Intel-Google Assignment (003)#page8.tif
source=Intel-Google Assignment (003)#page9.tif
source=Intel-Google Assignment (003)#page10.tif
source=Intel-Google Assignment (003)#page11.tif
source=Intel-Google Assignment (003)#page12.tif
source=Intel-Google Assignment (003)#page13.tif
source=Intel-Google Assignment (003)#page14.tif

PATENT ASSIGNMENT AGREEMENT

This Patent Assignment Agreement (this "Assignment") is made and entered into as of November 13, 2020, ("Effective Date") by and between Google LLC, a Delaware limited liability company ("Buyer") and Intel Corporation, a Delaware corporation ("Seller") (Buyer and Seller, each a "Party" and collectively, the "Parties").

WHEREAS, the Parties are parties to a Patent Sale Agreement dated November 6, 2020 (the "PSA"), pursuant to which, among other things, Seller has agreed to transfer to Buyer the Transferred Assets (as defined in Section 4 of this Assignment); and

WHEREAS, in accordance with, and subject to, the terms and conditions of the PSA, the Parties wish to execute this Assignment.

NOW, THEREFORE, in consideration of the foregoing and the representations, warranties, covenants and agreements contained in the PSA, and of other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, and intending to be legally bound, the Parties hereby agree as follows:

1. Assignment. On the terms and subject to the conditions set forth herein and in the PSA, Seller hereby sells, conveys, transfers, assigns and delivers to Buyer, and Buyer hereby purchases from Seller, all of Seller's right, title and interest, as of the Effective Date, in and to the Transferred Assets.

2. Recording the Assignment. The Parties hereby authorize the relevant authority at the United States Patent and Trademark Office, or any foreign equivalent thereto, to record this Assignment. Buyer agrees that it is Buyer's responsibility to record this Assignment.

3. Exclusion of Warranties. EXCEPT AS SET FORTH IN THE REPRESENTATIONS AND WARRANTIES SET FORTH IN THE PSA, THE TRANSFERRED ASSETS ARE ASSIGNED "AS IS" AND WITHOUT ANY REPRESENTATION OR WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTIES OF OR RELATED TO TITLE, NON-INFRINGEMENT, MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, VALIDITY OR ENFORCEABILITY.

4. Definitions. Capitalized terms used in this Assignment but not defined in this Assignment shall have the meanings ascribed to such terms in the PSA.

(a) "Patent" means any and all classes and types of patents (including originals, reexaminations, reissue, and extensions) in all countries of the world, and all applications for any of the foregoing.

(b) "Transferred Assets" means (i) all of Seller's right, title and interest, as of the Effective Date, in and to the Transferred Patents, and (ii) any right that Seller has to sue for past, present or future infringement of the Transferred Patents and to retain any damages and profits due or accrued and obtain injunctive relief for any such past, present or future infringement of the Transferred Patents.

(c) "Transferred Patents" means the Patents specifically set forth on Table A.

5. Entire Agreement. This Assignment, together with the PSA, contains the entire agreement between the Parties with respect to the subject matters hereof and thereof and supersedes all prior agreements and understandings, oral or written, with respect to such matters. In the event of any conflict between this Assignment and the PSA, the terms of the PSA shall govern.

6. Counterparts. This Assignment may be executed in one or more counterparts, each of which shall be deemed an original, and all of which shall constitute one and the same Assignment.

[Signature page follows]

PATENT
REEL: 054721 FRAME: 0980

IN WITNESS WHEREOF, each Party has caused this Assignment to be executed on its behalf by an officer thereunto duly authorized, all as of the date first written above.

INTEL CORPORATION:	GOOGLE LLC:
By: ______________________	By: ______________________
Name: Kenneth Nelson	Name: ______________________
Title: Assistant Director, Intel Patent Group	Title: ______________________

[Signature Page to the Patent Assignment Agreement between Intel Corporation and Google LLC, dated November 13, 2020]

DocuSign Envelope ID: 09D61376-2903-496B-A1A6-4583DBF939DE

IN WITNESS WHEREOF, each Party has caused this Assignment to be executed on its behalf by an officer thereunto duly authorized, all as of the date first written above.

INTEL CORPORATION:

By:______________________________

Name: ______________________________

Title: ______________________________

GOOGLE LLC:

By:

Name: Michael Lee

Title: Director, Head of Patents

[Signature Page to the Patent Assignment Agreement between Intel Corporation and Google LLC, dated November 13, 2020]

TABLE A

TRANSFERRED PATENTS

Patent/Publication/ Application Number	Title	Country
US8188792	Techniques for current mirror circuits	United States of America
US8108614	Mechanism for effectively caching streaming and non-streaming data patterns	United States of America
US8065488	Mechanism for effectively caching streaming and non-streaming data patterns	United States of America
US8402290	Power management for multiple processor cores	United States of America
CN101923383	Power management for multiple processor cores	China
CN103440028	The power management of multiple processor cores	China
TWI430079	Apparatus, system and method for power management for multiple processor cores	Taiwan
US7296137	Memory management circuitry translation information retrieval during debugging	United States of America
US7299335	Translation information retrieval transparent to processor core	United States of America
CN101203947	Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate	China
DE112006001705	A method of fabricating an integrated complementary metal oxide semiconductor circuit using an elevated source drain and a replacement metal gate	Germany
US8148786	Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate	United States of America
US7569443	Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate	United States of America
CN101336472	Multigate device with recessed strain regions	China
DE112006003550	Semiconductor device in the form of a mehrgateanordnung with recessed and strained source and drain regions and manufacturing method for these	Germany
JP5461014	Semiconductor device and manufacturing method thereof	Japan
KR101215775	Multigate device with recessed strain regions	Korea
US7525160	Multigate device with recessed strain regions	United States of America
CN101743627	Methods of forming improved epi fill on narrow isolation bounded source/drain regions and structures formed thereby	China
DE112008000636	A method of forming improved epi fillings on narrow isolation-limited source / drain regions and structures formed thereby	Germany
US7691752	Methods of forming improved epi fill on narrow isolation bounded source/drain regions and structures formed thereby	United States of America

PATENT
REEL: 054721 FRAME: 0983

DE112008000638	Method of making a semiconductor device with self-aligned epitaxial extensions of sources and sinks	Germany
JP5198478	Semiconductor device having self-aligned epitaxial source and drain overhangs	Japan
KR101237664	Semiconductor device having self-aligned epitaxial source and drain extensions	Korea
SG154643	Semiconductor device having self-aligned epitaxial source and drain extensions	Singapore
US7732285	Semiconductor device having self-aligned epitaxial source and drain extensions	United States of America
VN49357	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	Vietnam
US7821061	Silicon germanium and germanium multigate and nanowire structures for logic and multilevel memory applications	United States of America
US8936974	Silicon germanium and germanium multigate and nanowire structures for logic and multilevel memory applications	United States of America
US7727830	Fabrication of germanium nanowire transistors	United States of America
US8110458	Fabrication of germanium nanowire transistors	United States of America
US8269209	Isolation for nanowire devices	United States of America
US8883573	Isolation for nanowire devices	United States of America
US10483385	Nanowire structures having wrap-around contacts	United States of America
US8994174	Structure having a planar bonding surface	United States of America
US9252111	Method for handling very thin device wafers	United States of America
US10186581	Group iii-n nanowire transistors	United States of America
US9240410	Group iii-n nanowire transistors	United States of America
US9691857	Group iii-n nanowire transistors	United States of America
US8896066	Tin doped iii-v material contacts	United States of America
US9059024	Self-aligned contact metallization for reduced contact resistance	United States of America
US9153583	Iii-v layers for n-type and p-type mos source-drain contacts	United States of America
US9224735	Self-aligned contact metallization for reduced contact resistance	United States of America
US9397102	Iii-v layers for n-type and p-type mos source-drain contacts	United States of America
US9705000	Iii-v layers for n-type and p-type mos source-drain contacts	United States of America

US9754940	Self-aligned contact metallization for reduced contact resistance	United States of America
US9966440	Tin doped iii-v material contacts	United States of America
US9087863	Nanowire structures having non-discrete source and drain regions	United States of America
US9564522	Nanowire structures having non-discrete source and drain regions	United States of America
US10424580	Semiconductor devices having modulated nanowire counts	United States of America
US9559160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition	United States of America
US9691843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition	United States of America
US9627357	Stacked memory allowing variance in device interconnects	United States of America
US8716859	Enhanced flip chip package	United States of America
US9059304	Enhanced flip chip package	United States of America
US9385105	Semiconductor devices	United States of America
EP2803086	Semiconductor devices	Germany
EP2803086	Semiconductor devices	France
EP2803086	Semiconductor devices	United Kingdom
EP2803086	Semiconductor devices	Netherlands
US9634007	Trench confined epitaxially grown device layer(s)	United States of America
US10026845	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United States of America
US9136343	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United States of America
US9337291	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United States of America
US9640671	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United States of America
US8907480	Chip arrangements	United States of America
US9056763	Stress buffer layer for integrated microelectromechanical systems (mems)	United States of America
US9550670	Stress buffer layer for integrated microelectromechanical systems (mems)	United States of America
US9508796	Internal spacers for nanowire transistors and method of fabrication thereof	United States of America
US9935205	Internal spacers for nanowire transistors and method of fabrication thereof	United States of America

US10586868	Non-planar semiconductor device having hybrid geometry-based active region	United States of America
US9711492	Three dimensional structures within mold compound	United States of America
US9741651	Redistribution layer lines	United States of America
US9859253	Integrated circuit package stack	United States of America
US20200035818	Nanowire structures having wrap-around contacts	United States of America
US10541305	Group iii-n nanowire transistors	United States of America
US9653559	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	United States of America
US20200152797	Nanowire structures having non-discrete source and drain regions	United States of America
US10580899	Nanowire structures having non-discrete source and drain regions	United States of America
US20170162453	Trench confined epitaxially grown device layer(s)	United States of America
US20180301563	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United States of America
US20200185526	Non-planar semiconductor device having hybrid geometry-based active region	United States of America
US10593804	Non-planar semiconductor device having hybrid geometry-based active region	United States of America
TWI474965	Nanowire structures having wrap-around contacts	Taiwan
TWI499019	Chip structure, 3d packaging structure and method for forming packaging structure	Taiwan
TWI483398	Group iii-n nanowire transistors	Taiwan
TWI556448	Group iii-n nanowire transistors	Taiwan
TWI592992	Group iii-n nanowire transistors	Taiwan
TWI562376	Composite high-k metal gate stack for enhancement mode gan semiconductor devices and fabrication method thereof	Taiwan
TWI525670	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	Taiwan
TWI590312	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	Taiwan
TWI628704	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	Taiwan
TWI525669	Self-aligned contact metallization for reduced contact resistance	Taiwan
TWI603451	Self-aligned contact metallization for reduced contact resistance	Taiwan
TWI567987	iii-v layers for n-type and p-type mos source-drain contacts	Taiwan
TWI505469	Nanowire structures having non-discrete source and drain regions	Taiwan

TWI651855	Nanowire structures having non-discrete source and drain regions	Taiwan
TWI493716	Semiconductor structure and method of fabricating nanowire semiconductor structure	Taiwan
TWI493715	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition	Taiwan
TWI549224	Stacked memory allowing variance in device interconnects	Taiwan
TWI525665	Trench confined epitaxially grown device layer(s)	Taiwan
TWI578383	Trench confined epitaxially grown device layer(s)	Taiwan
TWI565071	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	Taiwan
TWI599047	A non-planar semiconductor device and method thereof	Taiwan
TWI640097	A non-planar semiconductor device and method thereof	Taiwan
TWI556435	Internal spacers for nanowire transistors and method of fabrication thereof	Taiwan
TWI643340	Internal spacers for nanowire transistors and method of fabrication thereof	Taiwan
TWI565058	Non-planar semiconductor device having hybrid geometry-based active region	Taiwan
TWI619179	Three dimensional structures within mold compound	Taiwan
TW201740527	Redistribution layer lines	Taiwan
TW201810602	Integrated circuit package stack	Taiwan
SG11201603948S	Non-planar semiconductor device having hybrid geometry-based active region	Singapore
KR101384394	Isolation for nanowire devices	Korea
KR101631778	Nanowire structures having wrap-around contacts	Korea
KR101791368	Nanowire structures having wrap-around contacts	Korea
KR101649055	Structure and method for handling a device wafer during tsv processing and 3d packaging structure	Korea
KR20160061969	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	Korea
KR101648279	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	Korea
KR101790153	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	Korea
KR101560112	Self-aligned contact metallization for reduced contact resistance	Korea
KR101790605	Semiconductor device having iii-v semiconductor material layer	Korea
KR101891458	Semiconductor device having iii-v semiconductor material layer	Korea
KR101612658	Semiconductor devices having modulated nanowire counts	Korea
KR101767352	Semiconductor structures having modulated nanowire counts and methods for fabricating the same	Korea
KR101824971	Semiconductor structures having modulated nanowire counts and methods for fabricating the same	Korea

KR101669375	Trench confined epitaxially grown device layer(s)	Korea
KR101988707	Trench confined epitaxially grown device layer(s)	Korea
KR101710466	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	Korea
KR102049414	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	Korea
KR20190133060	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	Korea
KR101594009	Chip arrangements	Korea
KR102136234	Internal spacers for nanowire transistors and method of fabrication thereof	Korea
KR20160098175	Non-planar semiconductor device having hybrid geometry-based active region	Korea
KR101785306	Three dimensional structures within mold compound	Korea
JP5497193	Nanowire insulation structure and formation method	Japan
JP5970071	Device structure manufacturing method and structure	Japan
JP5970078	Stacked memory that enables device interconnect changes	Japan
JP6290464	Semiconductor device and manufacturing method of semiconductor device	Japan
JP6205432	Deep gate all-around semiconductor device with germanium active layer or iii-v active layer	Japan
JP6555622	Integrated circuit structure, non-planar semiconductor device, and method of manufacturing non-planar semiconductor device	Japan
JP5940578	Chip device	Japan
JP6163702	Method for manufacturing package substrate or device	Japan
HK1175029	Isolation for nanowire devices	Hong Kong
EP2513972	Isolation for nanowire devices	United Kingdom
GB2524677	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	United Kingdom
EP2513972	Isolation for nanowire devices	EPO
EP3050112	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	EPO
EP2803086	Semiconductor devices	EPO
EP2901472	Trench confined epitaxially grown device layer(s)	EPO
EP2804211	Chip arrangements	EPO
EP3053190	Three dimensional structures within mold compound	EPO
EP3420589	Redistribution layer lines	EPO
EP3479403	Integrated circuit package stack	EPO
DE602010033168.7	Isolation for nanowire devices	Germany
DE112011106006	Nanowire structures with all-round contacts	Germany
DE112011105945	Group iii-n nanowire transistors	Germany
DE112011105972	iii-v layers for n-type and p-type mos source / drain contacts	Germany

DE112011106023	Nanowire structures with non-discrete source and drain regions	Germany
DE112011105905	Memory device with stacked memory that allows variability in device interconnections	Germany
DE112014000536	Deep gate all-around semiconductor device with active germanium or group iii-v layer	Germany
DE112014007315.6	Deep gate all-around semiconductor device with active germanium or group iii-v layer	Germany
CN104011868	Group iii-n nanowire transistors	China
CN106887453	Group iii-n nanowire transistors	China
CN104011870	The self-aligned contacts metallization of the contact resistance reducing	China
CN106847811	The self-aligned contacts metallization of the contact resistance of reduction	China
CN104137237	Nano thread structure with non-discrete source area and drain region	China
CN109065611	Nanowire structure with non-discrete source area and drain region	China
CN104126221	Semiconductor devices having modulated nanowire counts	China
CN106952958	The semiconductor devices of nano wire number with modulation	China
CN103999200	Have and comprise different materials orientation or the nano wire of composition or the common substrate semiconductor device of semiconductor body	China
CN106847805	Common substrate semiconductor device with nanowires or semiconductor bodies having different material orientations or compositions	China
CN103946980	Allow the cellar of the change in device interconnecting	China
CN104603920	The epitaxial growth device layer that groove is limited	China
CN107275331	The epitaxial growth device layer that groove is limited	China
CN104885228	Deep ring gate semiconductor device with germanium or iii v races active layer	China
CN107833910	Deep ring gate semiconductor device with germanium or iii v races active layer	China
CN104051412	Chip apparatus	China
CN105518840	Internal spacers for nanowire transistors and methods of fabricating the same	China
CN105874572	Non-planar semiconductor device with the active area based on mixing geometry	China
CN105874595	Three-dimensional structures in casting mold materials	China
WO2007002427	Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate	WIPO
GB2444681	Multigate device with recessed strain regions	United Kingdom
KR20080075009	Multigate device with recessed strain regions	Korea
WO2007075309	Multigate device with recessed strain regions	WIPO

WO2008121855	Methods of forming improved epi fill on narrow isolation bounded source/drain regions and structures formed thereby	WIPO
CN101622690	Semiconductor device having self-aligned epitaxial source and drain extensions	China
WO2008121659	Semiconductor device having self-aligned epitaxial source and drain extensions	WIPO
US8722478	Silicon germanium and germanium multigate and nanowire structures for logic and multilevel memory applications	United States of America
US9343302	Silicon germanium and germanium multigate and nanowire structures for logic and multilevel memory applications	United States of America
US20130219196	Power management for multiple processor cores	United States of America
DE102009051387	Power management for multiprocessor cores	Germany
AE574/2012	Isolation for nanowire devices	United Arab Emirates
CN102652364	For the isolation of nano-wire devices	China
NL2513972	Isolation for nanowire devices	Netherlands
WO2011075228	Isolation for nanowire devices	WIPO
EP2761651	Method for handling a very thin device wafer with a solder bump using a support substrate with a planar wetting surface and a layer of thermosetting material	EPO
CN104137228	Nanowire structures having wrap-around contacts	China
WO2013095647	Nanowire structures having wrap-around contacts	WIPO
CN103988299	For the method handling very thin device wafer	China
DE602011059393.5	Method for handling a very thin device wafer with a solder bump using a support substrate with a planar wetting surface and a layer of thermosetting material	Germany
EP2761651	Method for handling a very thin device wafer with a solder bump using a support substrate with a planar wetting surface and a layer of thermosetting material	France
EP2761651	Method for handling a very thin device wafer with a solder bump using a support substrate with a planar wetting surface and a layer of thermosetting material	United Kingdom
EP2761651	Method for handling a very thin device wafer with a solder bump using a support substrate with a planar wetting surface and a layer of thermosetting material	Netherlands
WO2013048496	Method for handling very thin device wafers	WIPO
TWI550796	Method for handling very thin device wafers	Taiwan
WO2013095343	Group iii-n nanowire transistors	WIPO
US9397188	Group iii-n nanowire transistors	United States of America
CN105474401	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	China

WO2015047316	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	WIPO
US20160204207	Composite high-k metal gate stack for enhancement mode gan semiconductor devices	United States of America
WO2013/100914	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	WIPO
US15/593104	Methods to enhance doping concentration in near-surface layers of semiconductors and methods of making same	United States of America
WO2013095377	Self-aligned contact metallization for reduced contact resistance	WIPO
KR20140097464	iii-v layers for n-type and p-type mos source-drain contacts	Korea
WO2013095375	iii-v layers for n-type and p-type mos source-drain contacts	WIPO
US15/645720	iii-v layers for n-type and p-type mos source-drain contacts	United States of America
WO2013095650	Nanowire structures having non-discrete source and drain regions	WIPO
WO2013095645	Semiconductor devices having modulated nanowire counts	WIPO
WO2013095656	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition	WIPO
JP2017-010605	Stacked memory allowing variance in device interconnects	Japan
WO2013081633	Stacked memory allowing variance in device interconnects	WIPO
US15/483220	Stacked memory allowing variance in device interconnects	United States of America
JP2015507360	Semiconductor device and manufacturing method of semiconductor device	Japan
WO2013104712	Semiconductor devices	WIPO
US8765563	Trench confined epitaxially grown device layer(s)	United States of America
WO2014051762	Trench confined epitaxially grown device layer(s)	WIPO
WO2014116433	Deep gate-all-around semiconductor device having germanium or group iii-v active layer	WIPO
EP3053185	Internal spacers for nanowire transistors and method of fabrication thereof	EPO
WO2015050546	Internal spacers for nanowire transistors and method of fabrication thereof	WIPO
EP3084811	Non-planar semiconductor device having hybrid geometry-based active region	EPO
WO2015094301	Non-planar semiconductor device having hybrid geometry-based active region	WIPO
WO2016093808	Three dimensional structures within mold compound	WIPO
WO2006130207	Translation information retrieval	WIPO
CN101495964	Translation information retrieval	China
WO2006130208	Translation information retrieval	WIPO
US20180068939	Redistribution layer lines	United States of America

WO2017146848	Redistribution layer lines	WIPO
WO2018004907	Integrated circuit package stack	WIPO
US17/072,992	Nanowire structures having wrap-around contacts	United States of America
KR10-2020-7030687	Non-planar semiconductor device having hybrid geometry-based active region	Korea
EP2803086	Semiconductor devices	Ireland
EP2803086	Semiconductor devices	Austria
EP2803086	Semiconductor devices	Belgium
EP2803086	Semiconductor devices	Switzerland
EP2803086	Semiconductor devices	Czech Republic
EP2803086	Semiconductor devices	Finland
EP2803086	Semiconductor devices	Liechtenstein
EP2803086	Semiconductor devices	Luxembourg
EP2803086	Semiconductor devices	Monaco
EP2803086	Semiconductor devices	Sweden
EP2803086	Semiconductor devices	Slovakia
EP2803086	Semiconductor devices	Spain
EP2803086	Semiconductor devices	Portugal

PATENT
RECORDED: 12/22/2020 **REEL: 054721 FRAME: 0992**