

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6551140

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
SILANNA SEMICONDUCTOR NORTH AMERICA, INC.	04/13/2019
RECEIVING PARTY DATA	
Name:	SILANNA ASIA PTE LTD
Street Address:	10 COLLYER QUAY
Internal Address:	#10-01 OCEAN FINANCIAL CENTRE
City:	SINGAPORE
State/Country:	SINGAPORE
Postal Code:	049315
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	17248873
CORRESPONDENCE DATA	
Fax Number:	(858)408-3570
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	8584811883
Email:	jon@mlo-ip.com
Correspondent Name:	L. JON LINDSAY
Address Line 1:	MLO
Address Line 2:	12707 HIGH BLUFF DRIVE, SUITE 200
Address Line 4:	SAN DIEGO, CALIFORNIA 92130
ATTORNEY DOCKET NUMBER:	SILSP073C1
NAME OF SUBMITTER:	L. JON LINDSAY
SIGNATURE:	/L. Jon Lindsay/
DATE SIGNED:	02/12/2021
Total Attachments: 1	
source=20210212_SILSP073C1_Assignment_Silanna_Semi_NA_to_Silanna_Asia#page1.tif	

PATENT ASSIGNMENT

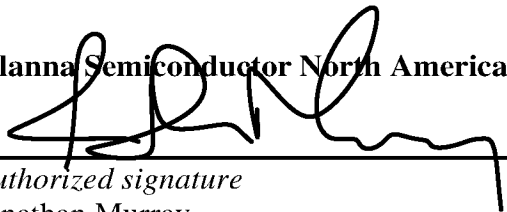
For good and valuable consideration, the receipt of which is hereby acknowledged, **Silanna Semiconductor North America, Inc.** ("Assignor"), having a registered office at 4795 Eastgate Mall, Suite 100, San Diego, CA 92121, USA, hereby assigns to **Silanna Asia Pte Ltd** ("Assignee"), having a registered office at 10 Collyer Quay, #10-01 Ocean Financial Centre, Singapore, 049315, all of its right, title and interest in and to the U.S. patent application listed below and the right to file non-provisionals, divisionals, continuations, continuations-in-part, substitute, continued prosecution, request for continued examination, renewals, reexaminations and reissues, and foreign filing of the patent application listed below, including but not limited to the right to file, prosecute and issue patent applications and patents claiming priority to the patent application listed below for the invention set forth in the patent application listed below and, including without limitation, any and all claims and potential claims of past, present and future infringement of such patent application and the right to sue and collect for past, present and future damages and any other causes of action under such patent application ("Assigned Patent Rights"):

Serial No.	Filing Date	Title	Inventors
Unassigned	Herewith	COMBINING VOLTAGE RAMPS TO CREATE LINEAR VOLTAGE RAMP	Joseph H. Colles; Steven E. Rosenbaum

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, letters patents, utility models or certificates of invention which may be granted upon the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

IN WITNESS WHEREOF Assignor has executed this Patent Assignment this 13th day of April, 2019.

Silanna Semiconductor North America, Inc.

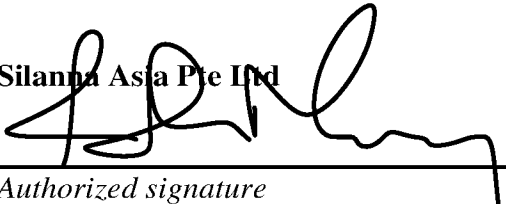


 Authorized signature
 Jonathan Murray

 Name (Printed)
 Treasurer

 Title

Silanna Asia Pte Ltd



 Authorized signature
 Jonathan Murray

 Name (Printed)
 Director

 Title

PATENT