PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	RESUBMISSION
NATURE OF CONVEYANCE:	ASSIGNMENT
RESUBMIT DOCUMENT ID:	506655393

CONVEYING PARTY DATA

Name	Execution Date
AURA SEMICONDUCTOR PRIVATE LIMITED	04/01/2021

RECEIVING PARTY DATA

Name:	NINGBO AURA SEMICONDUCTOR CO., LIMITED
Street Address:	203-2 OFFICE, #2 BUILDING, XINGEI ROAD
Internal Address:	HANG ZHOU BAY NEW DISTRICT
City:	NINGBO, ZHEJIANG
State/Country:	CHINA
Postal Code:	315336

PROPERTY NUMBERS Total: 13

Property Type	Number
Patent Number:	9319495
Patent Number:	9742414
Patent Number:	9438257
Patent Number:	9608801
Patent Number:	10312868
Patent Number:	10312872
Patent Number:	10389250
Patent Number:	10637402
Patent Number:	10700669
Patent Number:	10514720
Application Number:	15051675
Application Number:	62658625
Application Number:	62658626

CORRESPONDENCE DATA

Fax Number: (707)356-4172

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4435527281

Email:	general@iphorizons.com
Correspondent Name:	IPHORIZONS PLLC C/O MS. YASHNA THAPPETA
Address Line 1:	13495 BRIAR CT
Address Line 4:	SARATOGA, CALIFORNIA 95070

ATTORNEY DOCKET NUMBER:	AURA-1001-L
NAME OF SUBMITTER:	NARENDRA R. THAPPETA
SIGNATURE:	/Narendra R. Thappeta/
DATE SIGNED:	06/22/2021

Total Attachments: 8
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PATENT ASSIGNMENT CONFIRMATION AGREEMENT

This patent assignment agreement (the "**Agreement**"), is made and executed on this 01st day of April, 2021 ("**Effective Date**") by and between:

A. **Aura Semiconductor Private Limited,** a company established under the laws of India and having its registered office at Building 4C, 001, Ground Floor, RMZ Ecoworld SEZ, Devarabeesanahalli, Marathahalli, Sarjapur Outer Ring Road, Bangalore 560 103 (hereinafter referred to as the "**Assignor**");

AND

B. **Ningbo Aura Semiconductor Co., Limited,** a company established under the laws of People's Republic of China and having its registered office at 203-2 Office, #2 Building, Xingei Road, Hang Zhou Bay New District, Ningbo, Zhejiang – 315336 (hereinafter referred to as the "**Assignee**").

The Assignor and the Assignee shall individually be referred to as "**Party**" and collectively as "**Parties**".

WHEREAS:

A. The Assignor is a fabless semiconductor company that designs, builds (or have built on its behalf) and sells integrated circuits. The Assignor is an indirect wholly owned subsidiary of the Assignee.

B. Assignee is in the business of designing and manufacturing (or have made) of semiconductor products.

C. The Assignee desires to purchase or acquire all of Assignor's right, title, and interest in the Assigned Patents.

NOW THEREFORE, the Parties agree as follows:

1. Assigned Patents

Assigned Patents shall mean the issued U.S. and Indian patents and patent applications (including in pending, granted and abandoned status) listed on **Schedule** hereto, and, all know-how, trade secrets, whether patentable or not, invention, disclosures, developed or acquired before the date hereof related to the foregoing patents and patent applications.

2. Consideration and Assignment

2.1. In consideration of Assignee's payment obligations under this Clause 2, the Assignor hereby irrevocably and perpetually transfers, assigns, and delivers to Assignee all of Assignor's right, title, and interest of whatever kind in: (a) the Assigned Patents; (b) inventions disclosed in any patent or patent application listed on **Schedule**; (c) patents which may be issued on the patent applications and any of their continuations (including continuation-in-part), patents of addition, and divisionals, described on **Schedule**. Assignor agrees to execute all documents and agreements, and do all such acts, deeds, take such steps, as would be necessary to fully and effectively transfer and assign the Assigned Patents in favour of the Assignee.

2.2. In consideration of the above assignment, Assignor shall be entitled to receive from Assignee [Twenty percent (20%)] of the Net Revenues arising from development or commercialisation of the Assigned Patent during the two (2) year period following the date of this Agreement ("**Consideration**"). Consideration shall be calculated and reported in writing at the completion of the two (2) year commercialisation period mentioned hereinabove and shall be payable within sixty (60) days after the end of the said commercialisation period. "**Net Revenues**" shall mean

all monies received by the Assignee from sale, development or commercialization of the Assigned Patents, less taxes other than income taxes and any third party royalties if any paid.

2.3. In further consideration, Assignee hereby grants to Assignor a non-exclusive, fully paid, perpetual, irrevocable, worldwide licence, with the right to sublicense, to use the Assigned Patents for the purposes of development or manufacture of products incorporating the inventions disclosed in the Assigned Patents.

3. Successors

This Agreement shall inure to the benefit of and is binding upon the respective successors and assigns of Assignor and Assignee.

4. Miscellaneous

4.1. Entire Agreement, Amendment and Severability

This Agreement and Schedule constitute the entire agreement between the Parties and supersedes all prior oral or written agreements between the Parties with respect to the subject matter hereof. This Agreement may only be amended by writing signed by the Parties that refers explicitly to this Agreement. If a provision of this Agreement is unenforceable or invalid, the provision shall be revised so as to best accomplish the objectives of the Parties.

4.2. Notices

All notices under this Agreement shall be: (a) in writing; and (b) delivered by personal delivery or certified or registered mail, return receipt requested, or courier and deemed given upon personal delivery or upon receipt by the other Party. Notices shall be sent to the Parties at the addresses set forth in the introductory paragraph, or such other address as either Party may designate for itself in writing to the other Party.

4.3. Governing Law and Jurisdiction

This Agreement will be governed by and construed in accordance with the laws of India, and the courts of Bangalore, India shall have exclusive jurisdiction to determine any dispute or controversy arising from or relating to this Agreement.

IN WITNESS WHEREOF, Parties have executed this Agreement on the date and year first above mentioned.

For **Aura Semiconductor Private Limited**

Name: Srinath Sridharan
Designation: Director of Aura Semiconductor Private Limited

For **Ningbo Aura Semiconductor Co., Limited**

Name: Zhang Yi
Designation: Chairman of the board of directors of Ningbo Aura Semiconductor Co., Limited

SCHEDULE
DETAILS OF THE ASSIGNED PATENTS

Sl. No.	Application Type	Serial Number	Status	Title	Priority Date	Filed Date	Patent Number	Date Issued	Country
1.	Provisional	3527/CHE/2013	Pending	Power amplifier providing high efficiency.	June 08, 2013	June 08, 2013	-	-	India
2.	Utility	3527/CHE/2013	Abandoned	Power amplifier providing high efficiency.	June 08, 2013	June 08, 2013	-	-	India
3.	Provisional	2279/CHE/2015	Abandoned	Operating at origin without suffering delta sigma noise fold over.	May 05, 2015	May 05, 2015	-	-	India
4.	Provisional	2397/CHE/2015	Abandoned	Minimization of jitter noise power contributed by the low frequency forward path of a PLL.	May 11, 2015	May 11, 2015	-	-	India
5.	Provisional	3361/CHE/2015	Abandoned	Fractional-N feedback divider (DIVN) and integer-n feedforward divider (DIVO).	July 02, 2015	July 02, 2015	-	-	India
6.	Utility	3361/CHE/2015	Abandoned	Fractional-N feedback divider (DIVN) and integer-n feedforward divider (DIVO).	July 02, 2015	July 02, 2015	-	-	India

7.	Utility	201641018934	Abandoned	Reducing errors due to non-linearities caused by a phase frequency detector of a phase locked loop.	June 02, 2016	June 02, 2016	-	-	India
8.	Utility	201641018935	Abandoned	Phase locked loop with low phase-noise.	June 02, 2016	June 02, 2016	-	-	India
9.	Utility	201641019226	Abandoned	Programmable frequency divider providing a fifty-percent duty-cycle output over a range of divide factors.	July 02, 2015	June 03, 2016	-	-	India
10.	Provisional	201741012904	Abandoned	DCDC automatic transition.	April 11, 2017	April 11, 2017	-	-	India
11.	Provisional	201741012905	Abandoned	Circuit for generating the maximum of two voltages continuously.	April 11, 2017	April 11, 2017	-	-	India
12.	Utility	201741014020	Abandoned	Improved Linearity of Speaker Driver.	April 20, 2017	April 20, 2017	-	-	India
13.	Utility	201741014020	Abandoned	Correcting for non-linearity in an amplifier providing a differential output.	April 20, 2017	April 20, 2017	-	-	India
14.	Provisional	201741015165	Converted	Current shoot-through protecon in Class AB amplifier.	April 28, 2017	April 28, 2017	-	-	India

15.	Utility	201741015165	Pending	Managing a shoot-through condition in a component containing a push-pull output stage.	April 28, 2017	April 28, 2017	-	-	India
16.	Provisional	201741017431	Abandoned	Control scheme for peak inductor current control and zero inductor current detection to maximize efficiency of a DC-DC converter.	May 18, 2017	May 18, 2017	-	-	India
17.	Provisional	201841022836	Converted	Hitless switching when generating an output clock derived from multiple redundant input clocks.	June 19, 2018	June 19, 2018	-	-	India
18.	Provisional	201841022886	Converted	Clocking scheme for delta sigma modulator working with a fractional divider of variable length.	June 19, 2018	June 19, 2018	-	-	India
19.	Utility	201841023792	Pending	Operating mode for a DC-DC converter.	June 26, 2018	June 26, 2018	-	-	India
20.	Utility	201841023793	Pending	Charge pump for scaling the highest of multiple voltages when at least one of	June 26, 2018	June 26, 2018	-	-	India

				the multiple voltages varies.					
21.	Utility	201841022886	Pending	Avoiding very low duty cycles in a divided clock generated by a frequency divider.	June 19, 2018	May 21, 2019	-	-	India
22.	Utility	201841022836	Pending	Hitless switching when generating an output clock derived from multiple redundant input clocks.	June 19, 2018	May 27, 2019	-	-	India
23.	Utility	14449156	Issued	Audio power amplifier providing high efficiency.	August 06, 2013	August 01, 2014	9319495	April 19, 2016	United States of America
24.	Utility	14968930	Issued	Reducing errors due to non-linearities caused by a phase frequency detector of a phase locked loop.	May 05, 2015	December 15, 2015	9742414	August 22, 2017	United States of America
25.	Utility	15044115	Issued	Programmable frequency divider providing output with reduced duty-cycle variations over a range of divide ratios.	July 02, 2015	February 16, 2016	9438257	September 06, 2016	United States of America

26.	Utility	15046448	Issued	Programmable frequency divider providing a fifty-percent duty-cycle output over a range of divide factors.	July 02, 2015	February 18, 2016	9608801	March 28, 2017	United States of America
27.	Utility	15051675	Abandoned	Phase locked loop with low phase-noise.	May 11, 2015	February 24, 2016	-	-	United States of America
28.	Provisional	62658625	Converted	Operating mode for a DC-DC converter.	April 17, 2018	April 17, 2018	-	-	United States of America
29.	Provisional	62658626	Converted	Charge pump for scaling the highest of multiple voltages when at least one of the multiple voltages varies. A	April 17, 2018	April 17, 2018	-	-	United States of America
30.	Utility	15957927	Issued	Correcting for non-linearity in an amplifier providing a differential output.	April 20, 2017	April 20, 2018	10312868	June 04, 2019	United States of America
31.	Utility	15964102	Issued	Managing a shoot-through condition in a component containing a push-pull output stage.	April 28, 2017	April 27, 2018	10312872	June 04, 2019	United States of America

32.	Utility	16102739	Issued	Operating mode for a DC-DC converter.	April 17, 2018	August 14, 2018	10389250	August 20, 19	United States of America
33.	Utility	16102741	Issued	Charge pump for scaling the highest of multiple voltages when at least one of the multiple voltages varies.	April 17, 2018	August 14, 2018	10637402	April 28, 2020	United States of America
34.	Utility	16402257	Issued	Avoiding very low duty cycles in a divided clock generated by a frequency divider.	June 19, 2018	May 03, 2019	10700669	June 30, 2020	United States of America
35.	Utility	16419014	Issued	Hitless switching when generating an output clock derived from multiple redundant input clocks.	June 19, 2018	May 22, 2019	10514720	December 24, 2019	United States of America