PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6903705

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SPIN (ASSIGNMENT FOR BENEFIT OF CREDITORS), LLC	08/21/2021

RECEIVING PARTY DATA

Name:	INTEGRATED SILICON SOLUTION, (CAYMAN) INC.
Street Address:	P.O. BOX 309
Internal Address:	UGLAND HOUSE
City:	GRAND CAYMAN
State/Country:	CAYMAN ISLANDS
Postal Code:	KY1-1104

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14814036

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4086588094
Email: carmen@cookpatent.com
Correspondent Name: CARMEN COOK
Address Line 1: 1322 HAZLETT WAY
Address Line 4: SAN JOSE, CALIFORNIA 95131

ATTORNEY DOCKET NUMBER:	SP004US002
NAME OF SUBMITTER:	CARMEN C. COOK
SIGNATURE:	/Carmen C Cook/
DATE SIGNED:	09/07/2021

Total Attachments: 27
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EXHIBIT 9.1 (c)

INTELLECTUAL PROPERTY ASSIGNMENT AGREEMENT

This Intellectual Property Assignment Agreement (the "Assignment") is hereby entered into on August 21, 2021 (the "Effective Date"), by, between, and among Spin (assignment for the benefit of creditors), LLC, a California limited liability company, in its sole and limited capacity as assignee for the benefit of creditors of Spin Memory, Inc. ("Assignor"), and Integrated Silicon Solution (Cayman), Inc., a Cayman Islands corporation ("Assignee").

1. Assignor desires to transfer and assign to Assignee, and Assignee desires to accept the transfer and assignment of all of Assignor's right, title and interest in, to and under, all of the following (hereafter collectively referred to as "Intellectual Property"):

(i) the entire worldwide right, title and interest of Assignor in and to (A) each and all published patents and published patent applications in the United States and in all foreign countries including, without limitation, corresponding Patent Cooperation Treaty patents and patent applications and corresponding national patents and patent applications and all inventions, improvements and discoveries disclosed in said patents and applications, including but not limited to those set forth in **Schedule A** hereto, and (B) each patent application that is published after the Effective Date, having been unpublished as of the Effective Date, and (C) all substitutions, divisions, continuations, continuations-in-part, reexaminations, extensions, renewals and reissues (as applicable) of (A) and (B), including without limitation of generality, all rights of priority resulting from the filing of patent applications relating to any of the foregoing as well as any and all choices in action and any and all claims and demands, both at law and in equity, that Assignor has or may have for damages or profits accrued or to accrue on account of the infringement of any of said patents, patent applications, inventions, improvements and discoveries (or any provisional rights therein), the same to be held and enjoyed by Assignee, its successors and assigns, as fully and entirely as the same would have been held and enjoyed by Assignor if the assignment set forth in this Assignment had not been made;

(ii) the full and complete right to file patent applications in the name of the Assignor, at the Assignee's, or its designee's election, on the aforesaid inventions, improvements, discoveries and applications in all countries of the world;

(iii) the entire right, title and interest of Assignor in and to any patent which may issue thereon in the United States or in any country, and any renewals, revivals, reissues, reexaminations and extensions thereof, and any patents of confirmation, registration and importation of the same; and

(iv) any and all trademark, trade name, trade dress, and service mark rights throughout the world, including any and all applications, registrations, and common law marks, whether registered or not, together with the goodwill of the business associated with and symbolized by same, held by Assignor, including but not limited to those set forth on

Schedule B hereto, together with all common law rights therein, and the right of Assignor to sue for and recover damages or profits arising out of past, present, or future infringement of any and all of said rights as fully and entirely as the same would have been held and enjoyed by Assignor had this Assignment not been made.

2. Assignor, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, does hereby sell, convey, transfer and assign to Assignee, and Assignee hereby accepts the sale, conveyance, transfer and assignment of all right, title and interest of Assignor in, to and under the Intellectual Property, including all worldwide right, title and interest of Assignor in, to and under the Intellectual Property, together with the right of Assignor to claim priority in all countries in accordance with international law, any and all rights of Assignor corresponding to said Intellectual Property in countries throughout the world, and all of Assignor's rights to sue for past, present or future infringement of said Intellectual Property worldwide together with all claims for damages by reason of past, present or future infringement of said Intellectual Property, and the right to sue for and collect the same for Assignee's own use and enjoyment, all to be held and enjoyed by said Assignee, its successors and assigns, as fully and entirely as the same would have been held and enjoyed by Assignor had this Assignment not been made. Assignor hereby authorizes and requests the United States Patent and Trademarks Office to issue said Patents and Trademarks in accordance with this Assignment.

3. Schedule A may be updated by Assignee at any time after the Effective Date upon written notice to Assignor if it is found to be incomplete, incorrect, or otherwise did not accurately reflect the patents and patent applications owned by Assignee as of the Effective Date.

4. Assignor represents and warrants that Assignor has made no other agreements establishing any other encumbrances, liens, security interests, or third-party interests on or to the Intellectual Property, and that Assignor has full and complete authority to make this Assignment.

5. This Assignment may be executed in multiple counterparts, each of which shall be deemed an original hereof, and all of which shall constitute a single agreement effective as of the date hereof. Any delivery of an executed counterpart of this Assignment by facsimile or electronic mail shall be as effective as delivery of a manually executed counterpart of this Assignment.

6. This Assignment shall be binding upon and shall inure to the benefit of the parties and their respective successors and permitted assigns.

7. This Assignment shall be governed by and construed in accordance with federal law, to the extent applicable, and, where state law is implicated, the internal laws of the State of California, without giving effect to any principles of conflicts of law.

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IN WITNESS WHEREOF, Assignor and Assignee executed and delivered this Assignment by their duly authorized representatives as of the Effective Date.

ASSIGNOR:

Spin (assignment for the benefit of solely as assignee for the benefit of creditors of Spin Memory, Inc.

By: _____

Its: Manager

ASSIGNEE:

Integrated Silicon Solution creditors), LLC, (Cayman), Inc.

By: _____

Its: _____

IN WITNESS WHEREOF, Assignor and Assignee executed and delivered this Assignment by their duly authorized representatives as of the Effective Date.

ASSIGNOR:

Spin (assignment for the benefit of creditors), LLC, solely as assignee for the benefit of creditors of Spin Memory, Inc.

By:_____

Its:_____

ASSIGNEE:

Integrated Silicon Solution (Cayman), Inc.

By: Kongyen Han

Its: CEO

SCHEDULE A

Worldwide Patents and Patent Applications including but not limited to the following:

[TO ATTACH SCHEDULE OF PATENTS AND PATENT APPLICATIONS]

SCHEDULE B

Trademarks

TRADEMARKS: IN COUNTRIES INCLUDE UNITED STATES, CHINA, EUROPEAN UNION, JAPAN, SOUTH KOREA, AND TAIWAN

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	14/341,185	9,263,667	02/16/16	Issued	Magnetics	Original	Method for Manufacturing MTJ Memory Device
US	N/A	14/492,943	9,337,412	05/10/16	Issued	Magnetics	Original	Magnetic Tunnel Junction Structure for MRAM Device
US	N/A	14/814,036	9,853,206	12/26/17	Issued	Magnetics	Original based on PRO	Precessional Spin Current Structure for MRAM
US	N/A	14/866,359	9,728,712	08/08/17	Issued	Magnetics	Original based on PRO	Spin Transfer Torque Structure for MRAM Devices Having a Spin Current Injection Capping Layer
US	N/A	15/041,325	9,406,876	08/02/16	Issued	Magnetics	Continuation	Method for Manufacturing MTJ Memory Device
US	N/A	15/091,853	10,468,590	11/05/19	Issued	Magnetics	Original based on PRO	High Annealing Temperature Perpendicular Magnetic Anisotropy Structure For Magnetic Random Access Memory
US	N/A	15/097,576	9,773,974	09/26/17	Issued	Process	Original based on PRO	Polishing Stop Layer(s) For Processing Arrays of Semiconductor Elements
US	N/A	15/157,783	9,741,926	08/22/17	Issued	Magnetics	Original based on PRO	Memory Cell Having Magnetic Tunnel Junction and Thermal Stability Enhancement Layer
US	N/A	15/445,260	10,672,976	06/02/20	Issued	Magnetics	Original	Precessional Spin Current Structure With High In-Plane Magnetization For MRAM
US	N/A	15/445,362	10,665,777	05/26/20	Issued	Magnetics	Original	Precessional Spin Current Structure With Non-Magnetic Insertion For MRAM
US	N/A	15/634,629	10,032,978	07/24/18	Issued	Magnetics	Original	MRAM With Reduced Stray Magnetic Fields
US	N/A	15/656,398	10,381,553	08/13/19	Issued	Magnetics	Continuation	Memory Cell Having Magnetic Tunnel Junction And Thermal Stability Enhancement Layer (Child Application Of 58410-0025)
US	N/A	15/657,498	10,147,872	12/04/18	Issued	Magnetics	Continuation	Spin Transfer Torque Structure for MRAM Devices Having a Spin Current Injection Capping Layer
US	N/A	15/674,620	10,777,736	09/15/20	Issued	Process	Divisional	Polishing Stop Layer(s) For Processing Arrays of Semiconductor Elements

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/794,871	10,026,892	07/17/18	Issued	Magnetics	Divisional	Precessional Spin Current Structure for MRAM (continuation of 00014)
US	N/A	15/858,950	10,360,961	07/23/19	Issued	Design	Original	AC Current Pre-Charge Write-Assist in Orthogonal STT-MRAM
US	N/A	15/858,988	10,270,027	04/23/19	Issued	Design	Original	Self-Generating AC Current Assist in Orthogonal STT-MRAM
US	N/A	15/859,015	10,236,047	03/19/19	Issued	Magnetics	Original	Shared Oscillator (STNO) for MRAM Array Write-Assist in Orthogonal STT-MRAM
US	N/A	15/859,030	10,236,048	03/19/19	Issued	Design	Original	AC Current Write-Assist in Orthogonal STT-MRAM
US	N/A	15/859,047	10,199,083	02/05/19	Issued	Magnetics	Original	Three-Terminal MRAM With AC Write-Assist for Low Read Disturb
US	N/A	15/859,374	10,236,439	03/19/19	Issued	Magnetics	Original	Switching and Stability Control for Perpendicular Magnetic Tunnel Device
US	N/A	15/859,379	10,141,499	11/27/18	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Device With Offset Precessional Spin Current Layer
US	N/A	15/859,381	10,319,900	06/11/19	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Device With Precessional Spin Current Layer Having A Modulated Moment Density
US	N/A	15/859,384	10,339,993	07/02/19	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Device with Skyrmionic Assist Layers for Free Layer Switching
US	N/A	15/859,514	10,255,962	04/09/19	Issued	Magnetics	Original	Microwave Write-Assist in Orthogonal STT-MRAM
US	N/A	15/859,517	10,229,724	03/12/19	Issued	Magnetics	Original	Microwave Write-Assist in Series-Interconnected Orthogonal STT-MRAM devices
US	N/A	15/862,788	10,468,588	11/05/19	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Device With Skyrmionic Enhancement Layers For The Precessional Spin Current Magnetic Layer

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/027,739	10,553,787	02/04/20	Issued	Magnetics	Continuation	Precessional Spin Current Structure for MRAM
US	N/A	16/123,663	10,643,680	05/05/20	Issued	Magnetics	Continuation	Memory Cell Having Magnetic Tunnel Junction and Thermal Stability Enhancement Layer (continuation of 1058410-00025)
US	N/A	16/192,972	10,580,827	03/03/20	Issued	Magnetics	Original	Adjustable Stabilizer/Polarizer Method for MRAM with Enhanced Stability and Efficient Switching
US	N/A	16/197,622	10,615,335	04/07/20	Issued	Magnetics	Continuation	Spin Transfer Torque Structure for MRAM Devices Having a Spin Current Injection Capping Layer (continuation of 1058410-00049)
US	N/A	16/591,804	10,734,574	08/04/20	Issued	Magnetics	Divisional	Method of Manufacturing High Annealing Temperature Perpendicular Magnetic Anisotropy Structure for Magnetic Random Access Memory
CN	201580002433.3	N/A	CN 201580002433.3	07/31/18	Issued	Magnetics	National of PCT	Method for Manufacturing MTJ Memory Device
JP	2016-529428	N/A	6762231	09/10/20	Issued	Magnetics	National of PCT	Method for Manufacturing MTJ Memory Device
CN	201580009984.2	N/A	ZL201580009984.2	09/27/19	Issued	Magnetics	National of PCT	Magnetic Tunnel Junction Structure for MRAM Device
CN	201680035519.0	N/A	CN107750382A		Issued	Magnetics	National of PCT	Precessional Spin Current Structure for MRAM (continuation of 00014)

Schedula A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
JP	2017-564822	N/A	6770002	09/28/20	Issued	Magnetics	National of PCT	Precessional Spin Current Structure for MRAM (continuation of 00014)
US	N/A	15/857,574	10,541,268	01/21/20	Issued	Process	Original	Cylindrical Magnetic Memory Devices
US	N/A	15/858,765	10,797,233	10/06/20	Issued	Process	Original	Fabrication of Cylindrical Magnetic Memory Devices
US	N/A	15/858,808	10,326,073	06/18/19	Issued	Magnetics	Original	Spin Hall Effect (She) Assisted Three-Dimensional Spin Transfer Torque Magnetic Random Access Memory (Stt-Mram)
US	N/A	15/859,157	10,424,357	09/24/19	Issued	Process	Original	Magnetic Tunnel Junction (MTJ) Memory Device Having a Composite Free Magnetic Layer
US	N/A	15/859,250	10,403,343	09/03/19	Issued	Magnetics	Original	Systems and Methods Utilizing Serial Configurations of Magnetic Memory Devices
US	N/A	15/859,256	10,803,916	10/13/20	Issued	Design	Original	Methods and Systems for Writing to Magnetic Memory Devices Utilizing Alternating Current
US	N/A	15/859,259	10,347,308	07/09/19	Issued	Design	Original	Systems and Methods Utilizing Parallel Configurations of Magnetic Memory Devices
US	N/A	15/865,123	10,192,787	01/29/19	Issued	High density	Original	Methods of Fabricating Contacts for Cylindrical Devices
US	N/A	15/865,125	10,319,424	06/11/19	Issued	High density	Original	Adjustable Current Selectors
US	N/A	15/865,132	10,192,788	01/29/19	Issued	High density	Original	Methods of Fabricating Dual Threshold Voltage Device with Stacked Gates
US	N/A	15/865,135	10,770,510	09/08/20	Issued	High density	Original	Dual Threshold Voltage Devices

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of Filing	Patent Title
US	N/A	15/865,138	10,192,984	01/29/19	Issued	High density	Original	Dual Threshold Devices with Stacked Gates
US	N/A	15/865,140	10,192,789	01/29/19	Issued	High density	Original	Methods of Fabricating Dual Threshold Voltage Devices
US	N/A	15/865,144	10,497,415	12/03/19	Issued	High density	Original	Dual Gate Memory Devices
US	N/A	16/103,835	10,693,056	06/23/20	Issued	High density	Continuation-in-part	Buffer Layered Three-Dimensional Magnetic Memory (Tailoring the Interfacial Anisotropy in NanoCore MRAM)
US	N/A	16/147,257	10,692,556	06/23/20	Issued	High density	Original	Defect Injection Structure and Mechanism for Magnetic Memory
US	N/A	16/147,283	10,878,870	12/29/20	Issued	High density	Original	Defect Propagation Structure and Mechanism for Magnetic Memory
US	N/A	16/223,077	10,930,843	02/23/21	Issued	Magnetics	Original	Process for Manufacturing Scalable Spin-Orbit Torque (SOT) Magnetic Memory
US	N/A	16/223,080	10,600,465	03/24/20	Issued	Magnetics	Original	Spin-Orbit Torque (SOT) Magnetic Memory with Voltage or Current Assisted Switching
US	N/A	16/223,084	10,658,021	05/19/20	Issued	Magnetics	Original	Scalable Spin-Orbit Torque (SOT) Magnetic Memory
US	N/A	16/261,414	10,770,561	09/08/20	Issued	High density	Continuation	Methods of Fabricating Dual Threshold Voltage Devices
US	N/A	16/367,058	10,983,883	04/20/21	Issued	Other	Original	Error Recovery in Magnetic Random Access Memory After Reflow Soldering
US	N/A	16/434,724	10,854,260		Issued	High density	Continuation	Adjustable Current Selectors
US	N/A	16/506,878	10,937,478	03/02/21	Issued	Design	Continuation	Systems and Methods Utilizing Parallel Configurations of Magnetic Memory Devices

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/132,544	10,115,446	10/30/18	Issued	Engine	Original based on PRO	Spin Transfer Torque Mram Device With Error Buffer
US	N/A	15/174,483	10,163,479	12/25/18	Issued	Engine	Original based on PRO	Method and Apparatus for Bipolar Memory Write-Verify
US	N/A	15/277,799	10,366,774	07/30/19	Issued	Engine	Original	Device with Dynamic Redundancy Registers
US	N/A	15/691,577	10,347,314	07/09/19	Issued	Engine	Continuation	Method and Apparatus for Bipolar Memory Write-Verify
US	N/A	15/792,672	10,529,439	01/07/20	Issued	Design	Original	On-The-Fly- Bit Failure Detection And Bit Redundancy Remapping Techniques To Correct For Fixed Bit Defects
US	N/A	15/849,404	10,424,393	09/24/19	Issued	Engine	Divisional	Method Of Reading Data From A Memory Device Using Multiple Levels Of Dynamic Redundancy Registers (Title Changed)
US	N/A	15/849,457	10,366,775	07/30/19	Issued	Engine	Divisional	Memory Device Using Levels of Dynamic Redundancy Registers for Writing a Data Word That Failed a Write Operation
US	N/A	15/855,263	10,437,491	10/08/19	Issued	Engine	Continuation-in-part	Method Of Processing Incompleted Memory Operations In A Memory Device During A Power Up Sequence And A Power Down Sequence Using A Dynamic Redundancy Register
US	N/A	15/855,431	10,437,723	10/08/19	Issued	Engine	Continuation-in-part	Method to attempt Cleanup/Flush of E1 Before Power Down
US	N/A	15/855,589	10,360,964	07/23/19	Issued	Engine	Continuation-in-part	Method Of Writing Contents In Memory During A Power Up Sequence Using A Dynamic Redundancy Register In A Memory Device
US	N/A	15/855,660	10,679,685	06/09/20	Issued	Design	Original	Shared Bitline Array Architecture for MRAM

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/855,707	10,446,210	10/15/19	Issued	Engine	Continuation-in-part	Memory Instruction Pipeline With A Pre-Read Stage For A Write Operation For Reducing Power Consumption In A Memory Device That Uses
US	N/A	15/855,757	10,684,310	06/16/20	Issued	Other	Original	Magnetic Field Transducer Mounting Apparatus For MTJ Device Testers
US	N/A	15/855,799	10,962,590	03/30/21	Issued	Other	Original	Magnet Mounting Apparatus For Mtj Device Testers
US	N/A	15/855,811	10,192,601	01/29/19	Issued	Engine	Continuation-in-part	Memory Instruction Pipeline With an Additional Write Stage in a Memory Device That Uses Dynamic Redundancy Registers
US	N/A	15/855,855	10,192,602	01/29/19	Issued	Engine	Continuation-in-part	Smart Cache Design To Prevent Overflow For A Memory Device With A Dynamic Redundancy Register
US	N/A	15/855,866	10,481,976	11/19/19	Issued	Design	Continuation-in-part	Forcing Stuck Bits, Waterfall Bits, Shunt Bits And Low Tmr Bits To Short During Test And Using On-The-Fly Bit Failure Detection And Bit Redundancy Remapping
US	N/A	15/855,886	10,489,245	11/26/19	Issued	Design	Continuation-in-part	Forcing Stuck Bits, Waterfall Bits, Shunt Bits And Low Tmr Bits To Short During Testing And Using On-The-Fly Bit Failure Detection And Bit Redundancy Remapping Techniques To Correct Them
US	N/A	15/855,907	10,628,316	04/21/20	Issued	Engine	Continuation-in-part	Memory Device With A Plurality Of Memory Banks Where Each Memory Bank Is Associated With A Correspondence Memory Instruction Pipeline And A Dynamic Redundancy Register (N Plane Architecture)

Schedula A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/855,910	10,656,994	05/19/20	Issued	Design	Continuation-in-part	Over-Voltage Write Operation Of Tmr Memory Device And Correcting Failure Bits Therefrom By Using On-The-Fly Bit Failure Detection And Bit Redundancy Remapping Techniques Techniques
US	N/A	15/855,948	10,460,781	10/29/19	Issued	Engine	Continuation-in-part	Memory Device With A Dual Y-Multiplexer Structure For Performing Two Simultaneous Operations On The Same Row Of A Memory Bank
US	N/A	15/857,220	10,395,711	08/27/19	Issued	Design	Original	Perpendicular Source and Bit Lines for MRAM Array where Write Bias Voltage Goes from High to Low and Global Source Line Held at Zero Voltage
US	N/A	15/857,241	10,891,997	01/12/21	Issued	Design	Original	Grouped Bits with Horizontal Source Line and Virtual Source Line
US	N/A	15/857,264	10,395,712	08/27/19	Issued	Design	Original	Memory Array With Horizontal Source Line And Sacrificial Bitline Per Virtual Source
US	N/A	15/857,296	10,360,962	07/23/19	Issued	Design	Original	Memory Array With Individually Trimmable Sense Amplifiers
US	N/A	15/857,318	10,424,726	09/24/19	Issued	Process	Original	Process For Improving Photoresist Pillar Adhesion During MRAM Fabrication
US	N/A	15/857,351	10,811,594	10/20/20	Issued	Magnetics,Process	Original	Processing For Hard Mask Development For MRAM Pillar Formation Using Photolithography
US	N/A	15/857,382	10,516,094	12/24/19	Issued	Process	Original	Process For Creating Dense Pillars Using Multiple Exposures For MRAM Fabrication
US	N/A	15/858,398	10,546,624	01/28/20	Issued	Engine	Original	Multi-Port Random Access Memory
US	N/A	15/858,133	10,840,439	11/17/20	Issued	Magnetics	Original	Magnetic Tunnel Junction (MTJ) Fabrication Methods And Systems

Schedule A.1
Issued Patents

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/859,150	10,886,330	01/05/21	Issued	Magnetics	Original	Magnetic Tunnel Junction (MTJ) Structure Methods And Systems
US	N/A	15/859,195	10,840,436	11/17/20	Issued	Magnetics	Original	Perpendicular Magnetic Anisotropy Interface Tunnel Junction Devices And Methods Of Manufacture
US	N/A	15/859,230	10,367,139	07/30/19	Issued	Magnetics	Original	Methods Of Manufacturing Magnetic Tunnel Junction Devices
US	N/A	15/859,243	10,784,439	09/22/20	Issued	Magnetics	Original	Precessional Spin Current Magnetic Tunnel Junction Devices And Methods Of Manufacture
US	N/A	15/859,249	10,424,723	09/24/19	Issued	Magnetics	Original	Magnetic Tunnel Junction Devices Including An Optimization Layer
US	N/A	15/865,247	10,438,996	10/08/19	Issued	High density	Original	Methods Of Fabricating Magnetic Tunnel Junctions Integrated With Selectors (Method Of Integration Selector Device Using Two Single
US	N/A	15/865,249	10,438,995	10/08/19	Issued	High density	Original	Devices Including Magnetic Tunnel Junctions Integrated With Selectors (Selector Device Integrated With P-Mtj Memory Device Using Two Single Damascene Processes)
US	N/A	15/916,050	10,388,861	08/20/19	Issued	Other	Original	Magnetic Tunnel Junction Wafer Adaptor Used In Magnetic Annealing Furnace And Method Of Using The Same
US	N/A	15/916,078	10,446,744	10/15/19	Issued	Other	Original	Magnetic Tunnel Junction Wafer Adaptor Used In Magnetic Annealing Furnace And Method Of Using The Same
US	N/A	15/992,815	10,411,185	09/10/19	Issued	Process	Original	Test Platform of Lower Density For High Density 2D Magnetic Tunnel Junction (MTJ) Device Array

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/028,412	10,559,338	02/11/20	Issued	High density	Original	Multi-Bit Cell Read-Out Techniques
US	N/A	16/028,415	10,692,569	06/23/20	Issued	High density	Original	Read-Out Techniques for Multi-Bit Cell
US	N/A	16/059,012	10,734,573	08/04/20	Issued	High density	Original based on PRO	Magnetic Tunnel Junction Devices Including an Annular Discontinued Free Magnetic Layer and a Planar Reference Magnetic Layer
US	N/A	16/059,016	10,529,915	01/07/20	Issued	High density	Original based on PRO	Scalable Multi-stack With One Bit-Hole Process: 3D-NAND-Like Process
US	N/A	16/107,352	10,650,875	05/12/20	Issued	Other	Original	System For A Wide Temperature Range Nonvolatile Memory
US	N/A	16/118,137	10,546,625	01/28/20	Issued	Engine	Continuation-in-part	A Method Of Optimizing Write Voltage Based On Error Buffer Occupancy
US	N/A	16/121,480	10,784,437	09/22/20	Issued	High density	Continuation-in-part	Three-Dimensional Arrays with MTJ Devices Including a Free Magnetic Trench Layer and a Planar Reference Magnetic Layer
US	N/A	16/122,745	10,600,478	03/24/20	Issued	High density	Continuation-in-part	Multi-Bit Cell Read-Out Techniques For MRAM Cells With Mixed Pinned Magnetization Orientations (Split Of Spin-0044-01)
US	N/A	16/122,773	10,593,396	03/17/20	Issued	Design	Continuation-in-part	Multi-Bit Cell Read-Out Techniques For MRAM Cells With Mixed Pinned Magnetization Orientations
US	N/A	16/134,869	10,699,761	06/30/20	Issued	Design	Original	Word Line Decoder Memory Architecture
US	N/A	16/148,308	10,971,680	04/06/21	Issued	Magnetics	Original	Multi Terminal Device Stack Formation Methods

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/275,088	10,818,331	10/27/20	Issued	Design	Continuation-in-part	A Multi-Chip Module For MRAM Devices
US	N/A	16/294,920	10,803,949	10/13/20	Issued	Design	Original	Level Shifting Master Slave Latch Wordline Driver
US	N/A	16/388,774	10,615,337	04/07/20	Issued	Process	Divisional	A Process For Creating A High Density Magnetic Tunnel Junction Array Test Platform
US	N/A	16/520,162	10,930,332	02/23/21	Issued	Design	Continuation	Memory Array with Individually Trimmable Sense Amplifiers
US	N/A	16/584,731	10,879,457	12/29/20	Issued	Other	Continuation	Magnetic Tunnel Junction Wafer Adaptor Used In Magnetic Annealing Furnace and Method of Using the Same
US	N/A	16/598,568	10,991,410	04/27/21	Issued	Design	Continuation-in-part	Bipolar Write Scheme
US	N/A	16/598,599	11,010,294	05/18/21	Issued	Design	Continuation-in-part	MRAM Noise Mitigation For Write Operations With Simultaneous Background Operations
US	N/A	16/598,611	10,990,465	04/27/21	Issued	Design	Continuation-in-part	MRAM Noise Mitigation For Background By Delaying Write Timing To Avoid Being Aggressor To The Read Timing
US	N/A	15/851,593	10,236,075	03/19/19	Issued	Design	Original	Predicting Tunnel Barrier Endurance Using Redundant Memory Structures
US	N/A	15/866,381	10,431,628	10/01/19	Issued	High density	Original	Dual Channel/Gate Vertical Fieldeffect Transistor (Fet) For Use With A Perpendicular Magnetic Tunnel Junction (PMTJ)
US	N/A	16/051,272	10,614,867	04/07/20	Issued	High density	Original	Extreme Sub-litho Annular Patterning Technology
US	N/A	16/555,150	10,937,479	03/02/21	Issued	High density,Process	Original	Integrating Epi Grown Channel Selector with MRAM Device

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/685,873	10,957,370	03/23/21	Issued	High density,Process	Continuation	Integration Of Epitaxially Grown Channel Selector With Two Terminal Resistive Switching Memory Element.
US	N/A	15/865,066	10,333,063	06/25/19	Issued	Process	Original	Fabrication Of A Perpendicular Magnetic Tunnel Junction (PMTJ) Using Block Copolymers
US	N/A	15/859,114	10,355,045	07/16/19	Issued	High density	Original	Three-dimentional p-MTJ With Thin-Film Transistor
US	N/A	15/855,953	10,243,021	03/26/19	Issued	High density	Original	Steep Slope Field-Effect Transistor (Fet) For A Perpendicular Magnetic Tunnel Junction (PMTJ)
US	N/A	15/857,387	10,468,293	11/05/19	Issued	High density	Original	Methods of Forming Perpendicular Magnetic Tunnel Junction Memory Cells Having Vertical Channels
US	N/A	15/859,139	10,355,046	07/16/19	Issued	High density	Original	Steep Slope Field-Effect Transistor (Fet) For A Perpendicular Magnetic Tunnel Junction (Pmtj) (Split From Spimp017).
US	N/A	16/237,143	10,658,425	05/19/20	Issued	High density	Continuation-in-part	Methods Of Forming Perpendicular Magnetic Tunnel Junction Memory Cells Having Vertical Channels (Related To Spin025)
US	N/A	15/865,109	10,186,551	01/22/19	Issued	High density	Original	Buried Tap For A Vertical Transistor Used With A Perpendicular Magnetic Tunnel Junction (PMTJ)
US	N/A	15/859,040	10,460,778	10/29/19	Issued	Design	Original	Perpendicular Magnetic Tunnel Junction Memory Cells Having Shared Source Contacts
US	N/A	16/237,194	10,930,703	02/23/21	Issued	High density	Original based on PRO	High Density MRAM Integration
US	N/A	16/237,171	10,686,009	06/16/20	Issued	High density	Original based on PRO	High Density MRAM Integration

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/457,544	10,840,298	04/17/20	Issued	High density	Original	Vertical Selector STT MRAM Memory Architecture
US	N/A	16/691,448	10,854,255	12/01/20	Issued	High density	Continuation-in-part	Vertical Selector STT MRAM Memory Architecture
US	N/A	15/857,358	10,347,822	07/09/19	Issued	High density	Original	Fabrication Method of Forming Cylindrical Vertical Si Etched Channel 3D Switching Devices
US	N/A	15/859,222	10,355,047	07/16/19	Issued	High density	Original	Fabrication Methods Of Forming Annular Vertical Si Etched Channel Mos Devices
US	N/A	15/857,430	10,347,311	07/09/19	Issued	High density	Original	Cylindrical Vertical Si Etched Channel 3D Switching Devices
US	N/A	15/859,245	10,438,999	10/08/19	Issued	High density	Original	Annular Vertical Si Etched Channel Mos Devices
US	N/A	15/859,467	10,720,573	07/21/20	Issued	Process	Original	Method For Manufacturing Magnetic Tunnel Junction Pillars Using Photolithographicaly Directed Block Copolymer Self-Assembly And Organometallic Gas Infusion
US	N/A	16/362,329	10,847,199	11/24/20	Issued	Design	Original	Reinforcing Reference Structure For Magnetic Random-Access Memory
US	N/A	15/859,162	10,367,136	07/30/19	Issued	Magnetics	Original	Method For Manufacturing A Spin Current Structure In A Perpendicular Magnetic Tunnel Junction Using Mgo Radio Frequency Deposition
US	N/A	15/859,449	10,461,242	10/29/19	Issued	Magnetics	Original	Antiferromagnetic Exchange Coupling enhancement in pMTJ Stacks For MRAM Applications
US	N/A	15/862,495	10,186,308	01/22/19	Issued	Magnetics	Original	Magnetic Random Access Memory Having Improved Reliability Through Thermal Cladding
US	N/A	15/859,171	10,374,153	08/06/19	Issued	Process	Original	Method for Manufacturing a Magnetic Memory Device by Pre-Patterning a Bottom Electrode Prior to Patterning a Magnetic Material

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	15/859,453	10,916,582	02/09/21	Issued	High density	Original	Vertically-Strained Silicon Device For Use With A Perpendicular Magnetic Tunnel Junction (Pmtj)
US	N/A	15/858,070	10,629,649	04/21/20	Issued	High density	Original	Method of Making a 3D pMTJ With Thin-Film Transistor
US	N/A	16/178,105	10,847,198	11/24/20	Issued	Process	Original	Memory System Utilizing Heterogeneous MTJ Types in a Single Chip
US	N/A	16/211,167	10,971,681	04/06/21	Issued	Process	Original	Method For Manufacturing A Data Recording System Utilizing Heterogeneous Magnetic Tunnel Junction Types In A Single Chip (related to SPIN046)
US	N/A	15/859,074	10,790,333	09/29/20	Issued	Other	Original	Flexible Substrate For Use With A Perpendicular Magnetic Tunnel Junction (PMTJ)
US	N/A	15/859,460	10,374,147	08/06/19	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Having Improved Reference Layer Stability
US	N/A	16/147,242	10,608,047	03/31/20	Issued	Magnetics	Original	Magnetic Memory Element With Voltage Controlled Magnetic Anistropy
US	N/A	16/577,839	10,971,245	04/06/21	Issued	Design	Original	Measuring MTJ in The Compact Memory Array
US	N/A	15/859,224	10,651,370	05/12/20	Issued	Magnetics	Original	Perpendicular Magnetic Tunnel Junction Retention And Endurance Improvement
US	N/A	15/866,394	10,446,742	10/15/19	Issued	Process	Original	Method For Manufacturing A Magnetic Memory Element Array Using High Angle Side Etch To Open Top Electrical Contact
US	N/A	15/859,141	10,388,853	08/20/19	Issued	Magnetics	Original	Magnetic Memory Having a Pinning Synthetic Antiferromagnetic Structure (SAF) with Cobalt Over Platinum (Pt/Co) Bilayers

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/058,836	10,879,454	12/29/20	Issued	Magnetics	Original	Magnetic Tunnel Junction Memory Element With Improved Reference Layer Stability For Magnetic Random Access Memory Application
US	N/A	15/859,455	10,361,353	07/23/19	Issued	Magnetics	Original	Magnetic Random Access Memory With Reduced Internal Operating Temperature Range
US	N/A	15/859,459	10,388,860	08/20/19	Issued	Process	Original	Method For Manufacturing High Density Magnetic Random Access Memory Devices Using Diamond Like Carbon Hard Mask
US	N/A	15/866,362	10,305,031	05/28/19	Issued	High density	Original	Method For Manufacturing A Chemical Guidance Pattern For Block Copolymer Self Assembly From Photolithographically Defined Topographic Block Copolymer Guided Self Assembly
US	N/A	15/866,370	10,312,435	06/04/19	Issued	High density	Original	Method For Manufacturing High Density Magnetic Tunnel Junction Devices Using Photolithographic Vias And Chemically Guided Block Copolymer Self Assembly
US	N/A	15/859,465	10,607,902	03/20/20	Issued	Process	Original	Method For Measuring Proximity Effect On High Density Magnetic Tunnel Junction Devices In A Magnetic Random Access Memory Device
US	N/A	16/400,204	10,916,696		Issued	Process	Original	Method For Manufacturing Magnetic Memory Element With Post Pillar Formation Annealing
US	N/A	15/859,451	10,211,395	02/19/19	Issued	Process	Original	Method For Combining Nvm Class And SRAM Class MRAM Elements On The Same Chip
JP	2020-536182	N/A	6860748	03/30/21	Issued	Process	National of PCT	Method For Combining Nvm Class And SRAM Class MRAM Elements On The Same Chip
KR	10-2020-7022170	N/A	10-2198742	12/29/20	Issued	Process	National of PCT	Method For Combining NVM Class And SRAM Class MRAM Elements On The Same Chip

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Issue Date	Status	Category	Type of filing	Patent Title
US	N/A	16/397,759	10,903,002	01/26/21	Issued	Process	Original	Method For Manufacturing A Magnetic Memory Element Using Ru And Diamond Like Carbon Hard Masks
US	N/A	15/859,464	10,868,236	12/15/21	Issued	Process	Original	Method For Manufacturing Reduced Pitch Magnetic Random Access Memory Pillar
US	N/A	16/598,854	20200042451	06/29/21	Issued	Design	Continuation-in-part	Determining An Inactive Memory Bank During An Idle Memory Cycle To Prevent Error Cache Overflow

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Published Patent Applications

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Status	Published Date	Category	Type of filing	Patent Title
EP	16812075.6	N/A	EP3298638	Published	03/28/18	Magnetics	National of PCT	Precessional Spin Current Structure for MRAM (continuation of 00014)
EP	18761708.9	N/A	EP3583633	Published	12/25/19	Magnetics	National of PCT	Precessional Spin Current Structure With High In-Plane Magnetization For MRAM
EP	18761833.5	N/A	EP3583599	Published	12/25/19	Magnetics	National of PCT	Precessional Spin Current Structure For MRAM
CN	201680044692.7	N/A	CN107851712A	Published	03/27/18	Process	National of PCT	Polishing Stop Layer(s) for Processing Arrays of Semiconductor Elements
CN	201680080416.6	N/A	CN108604632A	Published	09/28/18	Magnetics	National of PCT	Memory Cell Having Magnetic Tunnel Junction and Thermal Stability Enhancement Layer
CN	201880021775.3	N/A	CN110462739	Published	11/15/19	Magnetics	National of PCT	Precessional Spin Current Structure For MRAM
KR	10-2017-7033059	N/A	KR20170139072	Published	12/18/17	Magnetics	National of PCT	High Annealing Temperature Perpendicular Magnetic Anisotropy Structure For Magnetic Random Access Memory
KR	10-2016-7013084	N/A	20170053258	Published	03/24/17	Magnetics	National of PCT	Method for Manufacturing MTJ Memory Device
KR	10-2016-7027094	N/A	KR20170063416	Published		Magnetics	National of PCT	Magnetic Tunnel Junction Structure for MRAM Device
KR	10-2018-7001466	N/A	KR20180018779	Published	02/21/18	Magnetics	National of PCT	Precessional Spin Current Structure for MRAM (continuation of 00014)
KR	10-2018-7005825	N/A	KR20180034613	Published	04/04/18	Process	National of PCT	Polishing Stop Layer(s) for Processing Arrays of Semiconductor Elements
KR	10-2018-7022992	N/A	KR20180100065	Published	09/06/18	Magnetics	National of PCT	Memory Cell Having Magnetic Tunnel Junction and Thermal Stability Enhancement Layer
KR	10-2019-7028383	N/A	KR20190115103	Published	10/10/19	Magnetics	National of PCT	Precessional Spin Current Structure For MRAM

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Status	Published Date	Category	Type of filing	Patent Title
KR	10-2019-7028584	N/A	KR20190115104	Published	10/10/19	Magnetics	National of PCT	Precessional Spin Current Structure For Mram
JP	2018-538876	N/A	2019-506745	Published	03/07/19	Magnetics	National of PCT	Memory Cell Having Magnetic Tunnel Junction and Thermal Stability Enhancement Layer
CN	201880021758.X	N/A	CN110476264A	Published	11/19/19	Magnetics	National of PCT	Precessional Spin Current Structure For Mram
JP	2019-0546792	N/A	2020-509590	Published	03/26/20	Magnetics	National of PCT	Precessional Spin Current Structure With High In-Plane Magnetization For MRAM
JP	2019-546791	N/A	2020511002	Published	04/09/20	Magnetics	National of PCT	Precessional Spin Current Structure For MRAM
US	N/A	16/818,472	20200220070	Published	07/09/20	Magnetics	Continuation	Precessional Spin Current Structure For MRAM
US	N/A	16/821,656	20200220074	Published	07/09/20	Magnetics	Divisional	Precessional Spin Current Structure with Non-Magnetic Insertion Layer for MRAM
US	N/A	16/452,302	20200409272	Published	12/31/20	Process	Original	Fabrication Method of a Sub-Lithographic Size Features and Reducing the Lithographic Pitch
US	N/A	16/452,197	20200409273	Published	12/31/20	Process	Original	Device, and methods for fabricating, reduced isolation
US	N/A	16/892,964	20200303631	Published	09/24/20	High density	Continuation	Three-Dimensional (3D) Magnetic Memory Device Comprising a Magnetic Tunnel Junction (MTJ) having a Metallic Buffer Layer
US	N/A	16/223,055	20200193282	Published	06/18/20	AI	Original	System and Method for Training Artificial Neural Networks
US	N/A	16/223,058	20200193283	Published	06/18/20	AI	Original	System and Method for Training Artificial Neural Networks
US	N/A	16/367,078	20200311555	Published	10/01/20	AI	Original	System and Method for Training Neural Networks with Errors
US	N/A	16/367,067	20200311522	Published	10/01/20	AI	Original	System and Method for Classifying Data Using a Neural Networks with Errors
US	N/A	16/121,453	20190296224	Published	09/26/19	High density	Continuation-in-part	Magnetic Tunnel Junction Devices Including a Free Magnetic Trench Layer and a Planar Reference Magnetic Layer

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Status	Published Date	Category	Type of filing	Patent Title
US	N/A	16/121,495	20190296230	Published	09/26/19	High density	Continuation-in-part	Methods of Manufacturing Three-Dimensional Arrays with MTJ Devices Including a Free Magnetic Trench Layer and a Planar Reference Magnetic Layer
US	N/A	16/148,223	20200105829	Published	04/02/20	Magnetics	Original	Multi Terminal Device Stack Systems And Methods
US	N/A	16/236,275	20200212296	Published	07/02/20	Process	Original	Patterned Silicide Structures and Methods of Manufacturing
US	N/A	16/443,345	20190303044	Published	10/03/19	Design	Continuation-in-part	MRAM Access Coordination Systems and Methods
US	N/A	16/598,596	20200042450	Published	02/06/20	Design	Continuation-in-part	Error Cache Segmentation For Power Reduction
US	N/A	16/598,634	20200117593	Published	04/16/20	Design	Continuation-in-part	Heuristics For Selecting Subsegments For Entry In And Entry Out Operations In An Error Cache System With Coarse And Fine Grain Segments
US	N/A	16/598,647	20200117610	Published	04/16/20	Design	Continuation-in-part	Error Cache System With Coarse And Fine Segments For Power Optimization
US	N/A	16/777,755	20200166544	Published	05/28/20	Other	Divisional	Magnetic Field Transducer Mounting Methods for MTJ Device Testers
US	N/A	16/831,592	20200227102	Filed	07/16/20	Design	Divisional	Word Line Decoder Memory Architecture
US	N/A	16/896,573	20200411752	Published	12/31/20	Magnetics	Divisional	Methods Of Manufacture Precessional Spin Current Magnetic Tunnel Junction Devices
US	N/A	17/111,207	20210089455	Published	03/25/21	Design	Continuation-in-part	Circuit Engine For Managing Memory META-Stability
CN	201780072273.90	N/A	CN109997189A	Published	07/09/19	Engine	National of PCT	A Method Of Writing Data Into A Memory Device Using Dynamic Redundancy Registers
EP	17857208.70	N/A	EP3520107	Published	08/07/19	Engine	National of PCT	A Method Of Writing Data Into A Memory Device Using Dynamic Redundancy Registers
CN	201780072274.30	N/A	CN1099977190A	Published	07/09/19	Engine	National of PCT	A Method Of Reading Data From A Memory Device Using Dynamic Redundancy Registers
EP	17857235.00	N/A	EP3520108	Published	08/07/19	Engine	National of PCT	A Method Of Reading Data From A Memory Device Using Dynamic Redundancy Registers

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Country	Foreign Application #	US Application #	Patent Pub or Patent #	Status	Published Date	Category	Type of filing	Patent Title
CN	201780072272.40	N/A	CN109997188A	Published	07/09/19	Engine	National of PCT	A Memory Device Using Dynamic Redundancy Registers
EP	17857252.50	N/A	EP3520109	Published	08/07/19	Engine	National of PCT	A Memory Device Using Dynamic Redundancy Registers
CN	201680053000.50	N/A	CN108140405A	Published	06/08/18	Engine	National of PCT	Method and Apparatus for Bipolar Memory Write-Verify
PCT	PCT/US2020/055346	N/A	WO/2021/071370	Published	04/15/21	Design	Original	Error Cache Segmentation For Power Reduction
US	N/A	16/719,790	20200127052	Published	04/23/20	High density	Continuation-in-part	Memory Cell Using Selective Epitaxial Vertical Channel MOS Select Transistor
US	N/A	15/859,116	20190207098	Published	07/04/19	High density	Original	Vertical Compound Semiconductor For Use With a Perpendicular Magnetic Tunnel Junction (PMTJ)
US	N/A	15/859,458	20190207091	Published	07/04/19	Magnetics	Original	High Retention Storage Layer Using Ultra-Low RA MgO Process in Perpendicular Magnetic Tunnel Junctions for MRAM Devices
PCT	PCT/US2020/039897	N/A	WO/2020/264349	Published	12/30/20	High density	Original	Vertical Selector STT MRAM Architecture
US	N/A	16/140,455	20200098980	Published	03/26/20	Process	Original	Method For Forming High Density Structures With Improved Resist Adhesion To Hard Mask
US	N/A	16/392,440	20200343298	Published	10/29/20	Process	Original	Magnetic Tunnel Junction Element With Ru Hard Mask For Use In Magnetic Random-Access Memory
PCT	PCT/US2020/029334	N/A	WO/2020/219555	Published	10/29/20	Process	Original	Magnetic Tunnel Junction Element With Ru Hard Mask For Use In Magnetic Random-Access Memory
US	N/A	16/019,429	20190392879	Published	12/26/19	Magnetics	Original	A Method Of Manufacturing MTJ device Isolation Layer For BEOL CMOS Annealing process
US	N/A	15/984,133	20190355896	Published	11/21/19	High density	Original	Three Dimensional Perpendicular Magnetic Tunnel Junction With Thin Film Transistor Array (Split Of Spinp015)
US	N/A	15/857,410	20190207024	Published	07/04/19	High density	Original	p-MTJ Memory Cells Having Vertical Channels
US	N/A	15/865,118	20190314552	Published	07/11/19	High density	Original	High Density 3D MRAM Cell Integration Using Wafer Cut and Transfer Method
US	N/A	16/124,655	20200083442	Published	03/12/20	Magnetics	Original	Precessional Spin Current Structure For Magnetic Random Access Memory With Novel Capping Materials
US	N/A	16/256,766	20200243124	Published	07/30/20	Design	Original	High Retention Multi-Level-Series Magnetic Random-Access Memory

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Published Patent Applications

Country	Foreign Application #	US Application #	Patent Pub or Patent #	Status	Published Date	Category	Type of filing	Patent Title
US	N/A	16/259,791	20200243757	Published	07/30/20	Process	Original	Method For Manufacturing A Magnetic Random-Access Memory Device Using Post Pillar Formation Annealing
PCT	PCT/US2020/030836	N/A	WO/2020/223549	Published	11/05/20	Process	Original	Method For Manufacturing Magnetic Memory Element With Post Pillar Formation Annealing
US	N/A	15/859,456	20190206929	Published	07/04/19	Process	Original	Magnetic Memory Chip Having Nvm Class And Sram Class Mram Elements On The Same Chip
CN	201880081072.X	N/A	CN111480242	Published	07/31/20	Process	National of PCT	Method For Combining Nvm Class And SRAM Class MRAM Elements On The Same Chip
PCT	PCT/US2020/030303	N/A	WO/2020/223254	Published	11/05/20	Process	Original	Method For Manufacturing A Magnetic Memory Element Using Ru And Diamond Like Carbon Hard Masks
US	N/A	16/397,987	20200343043	Published	10/29/20	Process	Original	Self Aligned Process For High Density Applications
PCT	PCT/US2020/030309	N/A	WO/2020/223258	Published	11/05/20	Process	Original	Self Aligned Process For High Density Applications