PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT6985249

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
CAVIUM, LLC	12/31/2019

RECEIVING PARTY DATA

Name:	CAVIUM INTERNATIONAL
Street Address:	C/O ESTERRA TRUST (CAYMAN) LIMITED, PO BOX 1350, CLIFTON HOUSE, 75 FORT STREET
City:	GRAND CAYMAN
State/Country:	CAYMAN ISLANDS
Postal Code:	KY1-1108

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16802357

CORRESPONDENCE DATA

Fax Number: (408)530-9797

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4085309700
Email: jowens@hollp.com
Correspondent Name: HAVERSTOCK & OWENS LLP
Address Line 1: 162 NORTH WOLFE ROAD
Address Line 4: SUNNYVALE, CALIFORNIA 94086

ATTORNEY DOCKET NUMBER:	XPL-02301
NAME OF SUBMITTER:	JONATHAN O. OWENS
SIGNATURE:	/Jonathan O. Owens/
DATE SIGNED:	10/24/2021

Total Attachments: 51
source=Assignment5_10_24_2021#page1.tif
source=Assignment5_10_24_2021#page2.tif
source=Assignment5_10_24_2021#page3.tif
source=Assignment5_10_24_2021#page4.tif
source=Assignment5_10_24_2021#page5.tif

source=Assignment5_10_24_2021#page6.tif
source=Assignment5_10_24_2021#page7.tif
source=Assignment5_10_24_2021#page8.tif
source=Assignment5_10_24_2021#page9.tif
source=Assignment5_10_24_2021#page10.tif
source=Assignment5_10_24_2021#page11.tif
source=Assignment5_10_24_2021#page12.tif
source=Assignment5_10_24_2021#page13.tif
source=Assignment5_10_24_2021#page14.tif
source=Assignment5_10_24_2021#page15.tif
source=Assignment5_10_24_2021#page16.tif
source=Assignment5_10_24_2021#page17.tif
source=Assignment5_10_24_2021#page18.tif
source=Assignment5_10_24_2021#page19.tif
source=Assignment5_10_24_2021#page20.tif
source=Assignment5_10_24_2021#page21.tif
source=Assignment5_10_24_2021#page22.tif
source=Assignment5_10_24_2021#page23.tif
source=Assignment5_10_24_2021#page24.tif
source=Assignment5_10_24_2021#page25.tif
source=Assignment5_10_24_2021#page26.tif
source=Assignment5_10_24_2021#page27.tif
source=Assignment5_10_24_2021#page28.tif
source=Assignment5_10_24_2021#page29.tif
source=Assignment5_10_24_2021#page30.tif
source=Assignment5_10_24_2021#page31.tif
source=Assignment5_10_24_2021#page32.tif
source=Assignment5_10_24_2021#page33.tif
source=Assignment5_10_24_2021#page34.tif
source=Assignment5_10_24_2021#page35.tif
source=Assignment5_10_24_2021#page36.tif
source=Assignment5_10_24_2021#page37.tif
source=Assignment5_10_24_2021#page38.tif
source=Assignment5_10_24_2021#page39.tif
source=Assignment5_10_24_2021#page40.tif
source=Assignment5_10_24_2021#page41.tif
source=Assignment5_10_24_2021#page42.tif
source=Assignment5_10_24_2021#page43.tif
source=Assignment5_10_24_2021#page44.tif
source=Assignment5_10_24_2021#page45.tif
source=Assignment5_10_24_2021#page46.tif
source=Assignment5_10_24_2021#page47.tif
source=Assignment5_10_24_2021#page48.tif
source=Assignment5_10_24_2021#page49.tif
source=Assignment5_10_24_2021#page50.tif
source=Assignment5_10_24_2021#page51.tif

ASSIGNMENT AND QUITCLAIM TRANSFER

WHEREAS, **Cavium, LLC**, a corporation organized under the laws of Delaware, and with offices at 5488 Marvell Lane, Santa Clara, California 95054 (hereinafter "**Assignor**") owns the patents and patent applications listed in Exhibit A attached hereto and incorporated herein by this reference (hereinafter "**Group A**") and may have an ownership interest in some or all of the patents and patent applications listed in Exhibit B attached hereto and incorporated herein by this reference (hereinafter "**Group B**");

WHEREAS, **Cavium International**, a corporation organized under the laws of Cayman Islands, and with offices at c/o Estera Trust (Cayman) Limited, PO Box 1350, Clifton House, 75 Fort Street, Grand Cayman KY1-1108 Cayman Islands, a limited liability corporation (hereinafter "Assignee"), desires to acquire the Assignor's ownership interest in, to and under the **Group A** and the **Group B**; and

WHEREAS, Assignor has executed on an effective date of December 31, 2019 (hereinafter "**Effective Date**") that certain Transfer and Assignment Agreement assigning, among other things, all interest in and to the **Group A** and transferring by quitclaim its ownership interest, if any, in and to the **Group B** to Assignee (the "Purchase Agreement").

NOW, THEREFORE, for consideration of one dollar ($1.00) and other good and valuable consideration paid by Assignee to Assignor, the receipt and sufficiency of which hereby is acknowledged, Assignor does hereby sell, assign and transfer to Assignee its entire interest in and to the **Group A**, including all divisions, continuations, reexaminations, reissues, and foreign counterparts of the applications and patent registrations for the **Group A** (and the right to claim priority and the right to apply for any of the foregoing); including assignment of any and all provisional applications that are relied upon for priority; all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the **Group A**.

FURTHER, for consideration of one dollar ($1.00) and other good and valuable consideration paid by Assignee to Assignor, the receipt and sufficiency of which hereby is acknowledged, Assignor does hereby **quitclaim** sell, assign and transfer to Assignee its ownership interest, if any, in and to the **Group B**, including all divisions, continuations, reexaminations, reissues, and foreign counterparts of the applications and patent registrations for the **Group B** (and the right to claim priority and the right to apply for any of the foregoing); including assignment of any and all provisional applications that are relied upon for priority; all rights to causes of action and remedies related thereto (including, without limitation, the right to sue for past, present or future infringement, misappropriation or violation of rights related to the foregoing); and any and all other rights and interests arising out of, in connection with or in relation to the **Group B**.

FURTHER, nothing contained herein shall be deemed to alter or amend the terms and provisions of the Purchase Agreement and in the event of any conflict between the terms and provisions of this Assignment and the Purchase Agreement, the terms and provisions of the Purchase Agreement shall be deemed to govern and be controlling in all circumstances. This Assignment is executed pursuant to the Purchase Agreement and is entitled to the benefits and subject to the

provisions thereof and shall bind and inure to the benefit of the parties thereto and their respective successors and assigns.

FURTHER, Assignor hereby covenants and agrees to execute and deliver, at the request of Assignee, such further instruments of transfer and assignment and to take any other action as such Assignee may reasonably request to more effectively consummate the assignments contemplated by this Assignment. Specifically, Assignor agrees to, at Assignee's expense, execute, acknowledge and deliver such further documents, instruments, conveyances and assurances and take such further actions as may be reasonably required to register in the name of Assignee the assignment of any of the Patents in **Group A** and/or the **Group B** in any appropriate governmental agency or registrar.

IN WITNESS WHEREOF, Assignor and Assignee have executed and delivered this Patent Assignment by their duly authorized representatives at 11:56 pm PST on the **Effective Date.**

ASSIGNOR:

Cavium, LLC,
a corporation organized under the laws of Delaware

By: _____

Jean Hu
President, Chief Financial Officer

ASSIGNEE:

Cavium International,
a corporation organized under the laws of Cayman Islands

By: _____

Philip Anderson
Director

provisions thereof and shall bind and inure to the benefit of the parties thereto and their respective successors and assigns.

FURTHER, Assignor hereby covenants and agrees to execute and deliver, at the request of Assignee, such further instruments of transfer and assignment and to take any other action as such Assignee may reasonably request to more effectively consummate the assignments contemplated by this Assignment. Specifically, Assignor agrees to, at Assignee's expense, execute, acknowledge and deliver such further documents, instruments, conveyances and assurances and take such further actions as may be reasonably required to register in the name of Assignee the assignment of any of the Patents in **Group A** and/or the **Group B** in any appropriate governmental agency or registrar.

IN WITNESS WHEREOF, Assignor and Assignee have executed and delivered this Patent Assignment by their duly authorized representatives at 11:56 pm PST on the **Effective Date.**

ASSIGNOR:

Cavium, LLC,
a corporation organized under the laws of Delaware

By: _____

Jean Hu
President, Chief Financial Officer

ASSIGNEE:

Cavium International,
a corporation organized under the laws of Cayman Islands

By: _____

Philip Anderson
Director

Exhibit A - 2C CAVIUM LLC TO CI Group A

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12007	MP12007	US	08/971,387	11/17/1997	6055285	4/25/2000	In Force	SYNCHRONIZATION CIRCUIT FOR TRANSFERRING POINTER BETWEEN TWO ASYNCHR
MP12008	MP12008	US	08/972,117	11/17/1997	6163550	12/19/2000	In Force	STATE DEPENDENT SYNCHRONIZATION CIRCUIT WHICH SYNCHRONIZES LEADING AN
MP12009	MP12009	US	09/030,865	2/26/1998	6151295	11/21/2000	In Force	OFDM RECEIVING SYSTEM
MP12010	MP12010	US	09/104,731	6/25/1998	6167321	12/26/2000	In Force	INTERFACE MODULE WITH PROTECTION CIRCUIT AND METHOD OF PROTECTING AN
MP12011	MP12011	US	09/386,109	8/30/1999	6597691	7/22/2003	In Force	HIGH PERFORMANCE SWITCHING
MP12013	MP12013	US	09/249,873	2/16/1999	6317842	11/13/2001	In Force	METHOD AND CIRCUIT FOR RECEIVING DUAL EDGE CLOCKED DATA
MP12014	MP12014	US	09/257,803	2/25/1999	6229845	5/8/2001	In Force	BUS DRIVER WITH DATA DEPENDENT DRIVE STRENGTH CONTROL LOGIC
MP12015	MP12015	US	09/280,506	3/30/1999	6470397	10/22/2002	In Force	SYSTEMS AND METHODS FOR NETWORK AND I/O DEVICE DRIVERS
MP12016	MP12016	US	09/281,369	3/30/1999	6327635	4/12/2001	In Force	ADD-ON CARD WITH AUTOMATIC BUS POWER LINE SELECTION CIRCUIT
MP12017	MP12017	US	09/282,341	3/31/1999	6434630	8/13/2002	In Force	HOST ADAPTER FOR COMBINING I/O COMPLETION REPORTS AND METHOD OF USIN
MP12018	MP12018	US	09/328,738	6/9/1999	6564271	5/13/2003	In Force	METHOD AND APPARATUS FOR AUTOMATICALLY TRANSFERRING I/O BLOCKS BETW
MP12019	MP12019	US	09/346,793	2/7/1999	6697359	2/24/2004	In Force	HIGH PERFORMANCE SWITCH FABRIC ELEMENT AND SWITCH SYSTEMS
MP12019	MP12019C1	US	10/752,390	1/6/2004	7408927	8/5/2008	In Force	HIGH PERFORMANCE SWITCH FABRIC ELEMENT AND SWITCH SYSTEMS
MP12022	MP12022WOU	US	10/166,570	6/10/2002	7443794	10/28/2008	In Force	FIBRE CHANNEL CREDIT EXTENDER AND REPEATER
MP12023	MP12023	US	09/587,689	6/5/2000	6708218	3/16/2004	In Force	IPSEC PERFORMANCE ENHANCEMENT USING A HARDWARE-BASED PARALLEL PROCE
MP12024	MP12024C1	US	11/765,724	6/20/2007	7684398	3/23/2010	In Force	HARDWARE-ENFORCED LOOP-LEVEL HARD ZONING FOR FIBRE CHANNEL SWITCH FA
MP12027	MP12027	US	09/755,642	1/4/2001	6883099	4/19/2005	In Force	SECURE VIRTUAL INTERFACE
MP12027	MP12027C1	US	11/070,858	3/1/2005	7389399	6/17/2008	In Force	SECURE VIRTUAL INTERFACE
MP12028	MP12028	US	09/792,428	2/21/2001	6976174	12/13/2005	In Force	SECURE MULTIPROTOCOL INTERFACE
MP12029	MP12029	US	10/025,512	12/19/2001	6789147	9/7/2004	In Force	INTERFACE FOR A SECURITY COPROCESSOR
MP12029	MP12029EP	EP	02016424.0	7/22/2002	1282025	7/4/2018	In Force	AN INTERFACE FOR A SECURITY COPROCESSOR
MP12029	MP12029EPDE	DE	02016424.0	7/22/2002	60249496.6	7/4/2018	In Force	AN INTERFACE FOR A SECURITY COPROCESSOR
MP12029	MP12029JP	JP	2002-215500	7/24/2002	4298971	7/22/2009	In Force	INTERFACE FOR SECURITY COPROCESSOR
MP12029	MP12029TW	TW	091116472	7/24/2002	576963	2/21/2004	In Force	AN INTERFACE FOR A SECURITY COPROCESSOR
MP12030	MP12030	US	09/938,166	8/23/2001	6954770	10/11/2005	In Force	RANDOM NUMBER GENERATOR
MP12031	MP12031	US	10/120,266	10/18/2001	7200144	4/3/2007	In Force	ROUTER AND METHODS USING NETWORK ADDRESSES FOR VIRTUALIZATION
MP12031	MP12031D1	US	10/284,273	10/29/2002	7362702	4/22/2008	In Force	ROUTER WITH ROUTING PROCESSORS AND METHODS FOR VIRTUALIZATION
MP12031	MP12031D3	US	10/285,226	10/31/2002	7292567	11/6/2007	In Force	ROUTER AND METHODS FOR DISTRIBUTED VIRTUALIZATION
MP12031	MP12031I1	US	11/098,831	4/4/2005	7447197	11/4/2008	In Force	SYSTEM AND METHOD OF PROVIDING NETWORK NODE SERVICES
MP12032	MP12032	US	09/992,637	11/6/2001	7376811	5/20/2008	In Force	METHOD AND APPARATUS FOR PERFORMING COMPUTATIONS AND OPERATIONS O
MP12034	MP12034	US	10/025,509	12/19/2001	7240203	7/3/2007	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSIONS
MP12034	MP12034DE	DE	02016423.2	7/22/2002	1292082	12/19/2018	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSION

PATENT
REEL: 057897 FRAME: 0507

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12034	MP12034EP	EP	02016423.2	7/22/2002	1292082	12/19/2018	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSION
MP12034	MP12034FR	FR	02016423.2	7/22/2002	1292082	12/19/2018	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSION
MP12034	MP12034GB	GB	02016423.2	7/22/2002	1292082	12/19/2018	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSION
MP12034	MP12034JP	JP	2002-215552	7/24/2002			Pending	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSIONS
MP12034	MP12034TW	TW	091116476	7/24/2002	I243566	11/11/2005	In Force	METHOD AND APPARATUS FOR ESTABLISHING SECURE SESSION
MP12035	MP12035	US	10/068,677	2/6/2002	7035889	4/25/2006	In Force	METHOD AND APPARATUS FOR MONTGOMERY MULTIPLICATION
MP12036	MP12036	US	10/052,054	1/17/2002	7076059	7/11/2006	In Force	METHOD AND APPARATUS TO IMPLEMENT THE DATA ENCRYPTION STANDARD ALG
MP12037	MP12037	US	10/086,665	2/28/2002	7096292	8/22/2006	In Force	On-Chip Inter-Subsystem Communication
MP12037	MP12037C1	US	11/422,373	6/6/2006	7243179	7/10/2007	In Force	On-Chip Inter-Subsystem Communication
MP12037	MP12037WO3	US	10/469,467	4/5/2004	7436954	10/14/2008	In Force	Security System With An Intelligent Dma Controller
MP12037	MP12037WOU	US	10/469,529	8/28/2003	7653763	1/26/2010	In Force	SUBSYSTEM BOOT AND PERIPHERAL DATA TRANSFER ARCHITECTURE FOR A SUBSYST
MP12038	MP12038	US	10/092,328	3/6/2002	7260217	8/21/2007	In Force	SPECULATIVE EXECUTION FOR DATA CIPHERING OPERATIONS
MP12039	MP12039	US	10/234,895	9/4/2002	7305567	12/4/2007	In Force	DECOUPLED ARCHITECTURE FOR DATA CIPHERING OPERATIONS
MP12040	MP12040	US	10/186,291	6/28/2002	6988150	1/17/2006	In Force	SYSTEM AND METHOD FOR EVENTLESS DETECTION OF NEWLY DELIVERED VARIABLE
MP12041	MP12041	US	10/600,779	6/20/2003	6864814	3/8/2005	In Force	SYSTEM AND METHOD FOR IMPROVING DYNAMIC RANGE OF ANALOG-TO DIGITAL C
MP12044	MP12044	US	10/200,393	7/22/2002	7230929	12/6/2007	In Force	METHOD AND SYSTEM FOR DYNAMICALLY ASSIGNING DOMAIN IDENTIFICATION IN
MP12044	MP12044-2	US	10/200,487	7/22/2002	7154886	12/26/2006	In Force	METHOD AND SYSTEM FOR PRIMARY BLADE SELECTION IN A MULTI-MODULE FIBRE
MP12044	MP12044-2C1	US	11/608,634	12/8/2006	7388861	6/17/2008	In Force	METHOD AND SYSTEM FOR PRIMARY BLADE SELECTION IN A MULTI-MODULE FIBRE
MP12045	MP12045	US	10/212,425	8/5/2002	7334046	2/19/2008	In Force	SYSTEM AND METHOD FOR OPTIMIZING FRAME ROUTING IN A NETWORK
MP12046	MP12046	US	10/213,237	8/6/2002	7263108	8/28/2007	In Force	DUAL-MODE NETWORK STORAGE SYSTEMS AND METHODS
MP12046	MP12046C1	US	11/845,688	8/27/2007	7688867	3/30/2010	In Force	DUAL-MODE NETWORK STORAGE SYSTEMS AND METHODS
MP12048	MP12048	US	10/241,153	11/9/2002	7397768	8/7/2008	In Force	ZONE MANAGEMENT IN A MULTI-MODULE FIBRE CHANNEL SWITCH
MP12048	MP12048C1	US	11/682,199	3/5/2007	7729288	6/1/2010	In Force	ZONE MANAGEMENT IN A MULTI-MODULE FIBRE CHANNEL SWITCH
MP12049	MP12049	US	10/263,858	3/10/2002	7362717	4/22/2008	In Force	METHOD AND SYSTEM FOR USING DISTRIBUTED NAME SERVERS IN MULTI-MODULE
MP12050	MP12050	US	10/295,976	11/15/2002	6769596	8/3/2004	In Force	METHOD AND SYSTEM FOR REWORKING BALL GRID ARRAYS
MP12053	MP12053	US	10/375,643	2/27/2003	6810440	10/26/2004	In Force	METHOD AND APPARATUS FOR AUTOMATICALLY TRANSFERRING I/O BLOCKS BETW
MP12054	MP12054	US	10/387,151	3/11/2003	6861865	3/1/2005	In Force	APPARATUS AND METHOD FOR REPAIRING LOGIC BLOCKS
MP12054	MP12054D1	US	11/040,266	1/20/2005	7205785	4/17/2007	In Force	APPARATUS AND METHOD FOR REPAIRING LOGIC BLOCKS
MP12055	MP12055	US	10/397,083	3/26/2003	7209531	4/24/2007	In Force	APPARATUS AND METHOD FOR DATA DESKEW
MP12056	MP12056	US	10/410,773	4/10/2003	6959345	10/25/2005	In Force	METHOD AND SYSTEM FOR CALIBRATING SCSI EXPANDERS
MP12057	MP12057	US	10/411,909	4/12/2003	7398386	7/8/2008	In Force	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO
MP12057	MP12057JPD1	JP	2010-131757	6/9/2010	5074558	11/14/2012	In Force	Network processing using IPSec
MP12057	MP12057WO	WO	PCT/US2004/00973	3/30/2004			Pending	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO
MP12057	MP12057WOEP	EP	04749529.6	3/30/2004	1614250	8/26/2015	In Force	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO

PATENT
REEL: 057897 FRAME: 0508

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12057	MP12057WOEP	DE	04749529.6	3/30/2004	6020040477	8/26/2015	In Force	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO
MP12057	MP12057WOEP	FR	04749529.6	3/30/2004	1614250	8/26/2015	In Force	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO
MP12057	MP12057WOJP	JP	2006-509485	3/30/2004			Pending	TRANSPARENT IPSEC PROCESSING INLINE BETWEEN A FRAMER AND A NETWORK CO
MP12058	MP12058	US	10/411,944	4/12/2003	7661130	2/9/2010	In Force	APPARATUS AND METHOD FOR ALLOCATING RESOURCES WITHIN A SECURITY PROC
MP12059	MP12059	US	10/411,967	4/12/2003	7814310	10/12/2010	In Force	IPSEC PERFORMANCE OPTIMIZATION
MP12059	MP12059WO	WO	PCT/US2004/00983	3/31/2004	DNA		Pending	IPSEC PERFORMANCE OPTIMIZATION
MP12060	MP12060	US	10/411,943	4/12/2003	7657933	2/2/2010	In Force	APPARATUS AND METHOD FOR ALLOCATING RESOURCES WITHIN A SECURITY PROC
MP12060	MP12060WO	WO	PCT/US2004/01091	4/8/2004	DNA		Pending	AN APPARATUS AND METHOD FOR ALLOCATING RESOURCES WITHIN A SECURITY PR
MP12061	MP12061	US	10/411,945	4/12/2003	7337314	2/26/2008	In Force	APPARATUS AND METHOD FOR ALLOCATING RESOURCES WITHIN A SECURITY PROC
MP12061	MP12061WO	WO	PCT/US2004/01078	4/7/2004	DNA		Pending	AN APPARATUS AND METHOD FOR ALLOCATING RESOURCES WITHIN A SECURITY PR
MP12062	MP12062	US	10/417,523	4/17/2003	6961784	11/1/2005	In Force	METHOD AND SYSTEM FOR PROCESSING NON-DATA FRAMES IN HOST BUS ADAPTER
MP12063	MP12063	US	10/423,499	4/25/2003	6996785	2/7/2006	In Force	ON-CHIP PACKET-BASED INTERCONNECTIONS USING REPEATERS/ROUTERS
MP12063	MP12063C1	US	11/283,210	11/18/2005	7543250	6/2/2009	In Force	ON-CHIP PACKET-BASED INTERCONNECTIONS USING REPEATERS/ROUTERS
MP12065	MP12065	US	10/445,695	5/27/2003	7424419	9/9/2008	In Force	METHOD AND SYSTEM FOR PROVIDING A VIRTUAL UNIVERSAL SERIAL PORT INTERFA
MP12066	MP12066	US	10/601,534	6/24/2003	7352778	4/1/2008	In Force	SYNCHRONIZING METHOD AND APPARATUS
MP12066	MP12066CA	CA	2433139	6/23/2003	2433139	3/27/2012	In Force	SYNCHRONIZING METHOD AND APPARATUS
MP12067	MP12067	US	10/619,719	7/15/2003	7515612	4/7/2009	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK DATA PACKETS
MP12067	MP12067C1	US	12/389,308	2/19/2009	7830919	11/9/2010	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK DATA PACKETS
MP12068	MP12068	US	10/620,040	7/15/2003	7403542	7/22/2008	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK DATA PACKETS
MP12070	MP12070	US	10/889,551	7/12/2004	7388843	6/17/2008	In Force	METHOD AND APPARATUS FOR TESTING LOOP PATHWAY INTEGRITY IN A FIBRE CHA
MP12071	MP12071	US	10/889,256	7/12/2004	7620059	11/17/2009	In Force	METHOD AND APPARATUS FOR ACCELERATING RECEIVE-MODIFY-SEND FRAMES IN A
MP12072	MP12072	US	10/889,259	7/12/2004	7453802	11/18/2008	In Force	METHOD AND APPARATUS FOR DETECTING AND REMOVING ORPHANED PRIMITIVES
MP12072	MP12072C1	US	12/198,644	8/26/2008	7542418	6/2/2009	In Force	METHOD AND APPARATUS FOR DETECTING AND REMOVING ORPHANED PRIMITIVES
MP12073	MP12073	US	10/889,337	7/12/2004	7355966	4/8/2008	In Force	METHOD AND SYSTEM FOR MINIMIZING DISRUPTION IN COMMON-ACCESS NETWO
MP12074	MP12074	US	10/889,635	7/12/2004	7525910	4/28/2009	In Force	METHOD AND SYSTEM FOR NON-DISRUPTIVE DATA CAPTURE IN NETWORKS
MP12075	MP12075	US	10/889,588	7/12/2004	7152132	12/19/2006	In Force	METHOD AND APPARATUS FOR IMPROVING BUFFER UTILIZATION IN COMMUNICATI
MP12076	MP12076	US	10/894,827	7/20/2004	7525983	4/28/2009	In Force	METHOD AND SYSTEM FOR SELECTING VIRTUAL LANES IN FIBRE CHANNEL SWITCHE
MP12076	MP12076D1	US	12/427,966	4/22/2009	8081650	12/20/2011	In Force	METHOD AND SYSTEM FOR SELECTING VIRTUAL LANES IN FIBRE CHANNEL SWITCHE
MP12077	MP12077	US	10/889,267	7/12/2004	7463646	12/9/2008	In Force	METHOD AND SYSTEM FOR FIBRE CHANNEL ARBITRATED LOOP ACCELERATION
MP12078	MP12078	US	10/889,255	7/12/2004	7471635	12/30/2008	In Force	METHOD AND APPARATUS FOR TEST PATTERN GENERATION
MP12080	MP12080	US	10/894,492	7/20/2004	7466700	12/16/2008	In Force	LUN BASED HARD ZONING IN FIBRE CHANNEL SWITCHES
MP12081	MP12081	US	10/895,175	7/20/2004	7522529	4/21/2009	In Force	METHOD AND SYSTEM FOR DETECTING CONGESTION AND OVER SUBSCRIPTION IN A
MP12082	MP12082	US	10/674,943	9/30/2003	7234101	6/19/2007	In Force	METHOD AND SYSTEM FOR PROVIDING DATA INTEGRITY IN STORAGE SYSTEMS
MP12083	MP12083	US	10/894,689	7/20/2004	7477655	1/13/2009	In Force	METHOD AND SYSTEM FOR POWER CONTROL OF FIBRE CHANNEL SWITCHES

PATENT
REEL: 057897 FRAME: 0509

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12083	MP12083C1	US	12/267,188	11/7/2008	7822061	10/26/2010	In Force	METHOD AND SYSTEM FOR POWER CONTROL OF FIBRE CHANNEL SWITCHES
MP12084	MP12084-1	US	10/894,491	7/20/2004	7420982	9/2/2008	In Force	METHOD AND SYSTEM FOR KEEPING A FIBRE CHANNEL ARBITRATED LOOP OPEN DU
MP12084	MP12084-1-C1	US	12/191,890	8/14/2008	7822057	10/26/2010	In Force	METHOD AND SYSTEM FOR KEEPING A FIBRE CHANNEL ARBITRATED LOOP OPEN DU
MP12084	MP12084-2	US	10/894,536	7/20/2004	7512067	3/31/2009	In Force	METHOD AND SYSTEM FOR CONGESTION CONTROL BASED ON OPTIMUM BANDWID
MP12084	MP12084-3	US	10/894,587	7/20/2004	7580354	8/25/2009	In Force	MULTI-SPEED CUT THROUGH OPERATION IN FIBRE CHANNEL SWITCHES
MP12084	MP12084-3-C1	US	12/502,973	7/14/2009	9118586	8/25/2015	In Force	MULTI-SPEED CUT THROUGH OPERATION IN FIBRE CHANNEL SWITCHES
MP12084	MP12084-4	US	10/894,629	7/20/2004	7447224	11/4/2008	In Force	METHOD AND SYSTEM FOR ROUTING FIBRE CHANNEL FRAMES
MP12084	MP12084-4-C1	US	12/189,502	8/11/2008	7936771	5/3/2011	In Force	METHOD AND SYSTEM FOR ROUTING FIBRE CHANNEL FRAMES
MP12084	MP12084-5	US	10/894,726	7/20/2004	7583597	9/1/2009	In Force	METHOD AND SYSTEM FOR IMPROVING BANDWIDTH AND REDUCING IDLES IN FIBR
MP12085	MP12085	US	10/664,548	9/19/2003	7352701	4/1/2008	In Force	BUFFER TO BUFFER CREDIT RECOVERY FOR IN-LINE FIBRE CHANNEL CREDIT EXTENSI
MP12086	MP12086	US	10/894,595	7/20/2004	7522522	4/21/2009	In Force	METHOD AND SYSTEM FOR REDUCING LATENCY AND CONGESTION IN FIBRE CHANN
MP12087	MP12087	US	10/894,627	7/20/2004	7573909	8/11/2009	In Force	METHOD AND SYSTEM FOR PROGRAMMABLE DATA DEPENDANT NETWORK ROUTIN
MP12088	MP12088	US	10/683,622	10/10/2003	7009413	3/7/2006	In Force	SYSTEM AND METHOD FOR TESTING BALL GRID ARRAYS
MP12089	MP12089	US	10/696,471	10/29/2003	7219263	5/15/2007	In Force	METHOD AND SYSTEM FOR MINIMIZING MEMORY CORRUPTION
MP12090	MP12090	US	10/719,077	11/21/2003	7103504	9/5/2006	In Force	METHOD AND SYSTEM FOR MONITORING EVENTS IN STORAGE AREA NETWORKS
MP12091	MP12091	US	10/723,004	11/26/2003	6949423	9/27/2005	In Force	MOSFET-FUSED NONVOLATILE READ-ONLY MEMORY CELL (MOFROM)
MP12092	MP12092	US	10/894,586	7/20/2004	7630384	12/8/2009	In Force	METHOD AND SYSTEM FOR DISTRIBUTING CREDIT IN FIBRE CHANNEL SYSTEMS
MP12092	MP12092C1	US	12/580,169	10/15/2009	8072988	12/6/2011	In Force	METHOD AND SYSTEM FOR BUFFER-TO-BUFFER CREDIT RECOVERY IN FIBRE CHANNE
MP12093	MP12093	US	10/894,547	7/20/2004	7684401	3/23/2010	In Force	METHOD AND SYSTEM FOR USING EXTENDED FABRIC FEATURES WITH FIBRE CHANN
MP12093	MP12093C1	US	12/697,994	2/1/2010	7990975	8/2/2011	In Force	METHOD AND SYSTEM FOR USING EXTENDED FABRIC FEATURES WITH FIBRE CHANN
MP12093	MP12093C1D1	US	13/177,314	7/6/2011	8644317	2/4/2014	In Force	METHOD AND SYSTEM FOR USING EXTENDED FABRIC FEATURES WITH FIBRE CHANN
MP12094	MP12094	US	10/894,597	7/20/2004	7406092	7/29/2008	In Force	PROGRAMMABLE PSEUDO VIRTUAL LANES FOR FIBRE CHANNEL SYSTEMS
MP12094	MP12094C1	US	12/141,519	6/18/2008	7760752	7/20/2010	In Force	PROGRAMMABLE PSEUDO VIRTUAL LANES FOR FIBRE CHANNEL SYSTEMS
MP12095	MP12095	US	10/894,579	7/20/2004	7430175	9/30/2008	In Force	METHOD AND SYSTEM FOR MANAGING TRAFFIC IN FIBRE CHANNEL SYSTEMS
MP12095	MP12095C1	US	12/189,497	8/11/2008	7649903	1/19/2010	In Force	METHOD AND SYSTEM FOR MANAGING TRAFFIC IN FIBRE CHANNEL SYSTEMS
MP12096	MP12096	US	10/894,546	7/20/2004	7792115	9/7/2010	In Force	METHOD AND SYSTEM FOR ROUTING AND FILTERING NETWORK DATA PACKETS IN FI
MP12097	MP12097	US	10/798,527	3/11/2004	7480293	1/20/2009	In Force	METHOD AND SYSTEM FOR PREVENTING DEADLOCK IN FIBRE CHANNEL FABRICS USI
MP12098	MP12098	US	10/798,468	3/11/2004	7564789	7/21/2009	In Force	METHOD AND SYSTEM FOR REDUCING DEADLOCK IN FIBRE CHANNEL FABRICS USIN
MP12100	MP12100	US	10/894,978	7/20/2004	7646767	1/12/2010	In Force	METHOD AND SYSTEM FOR PROGRAMMABLE DATA DEPENDANT NETWORK ROUTIN
MP12101	MP12101	US	10/797,977	3/10/2004	7231410	6/12/2007	In Force	REVISION CONTROL SYSTEM FOR LARGE-SCALE SYSTEMS MANAGEMENT
MP12101	MP12101C1	US	11/748,160	5/14/2007	7647363	1/12/2010	In Force	REVISION CONTROL SYSTEM FOR LARGE-SCALE SYSTEMS MANAGEMENT
MP12102	MP12102	US	10/806,691	3/23/2004	7424564	9/9/2008	In Force	PCI - EXPRESS SLOT FOR COUPLING PLURAL DEVICES TO A HOST SYSTEM
MP12107	MP12107	US	10/894,732	7/20/2004	7894348	2/22/2011	In Force	METHOD AND SYSTEM FOR CONGESTION CONTROL IN A FIBRE CHANNEL SWITCH
MP12108	MP12108	US	10/848,485	5/17/2004	7493481	2/17/2009	In Force	DIRECT HARDWARE PROCESSING OF INTERNAL DATA STRUCTURE FIELDS

PATENT
REEL: 057897 FRAME: 0510

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12109	MP12109	US	10/894,917	7/20/2004	7558281	7/7/2009	In Force	METHOD AND SYSTEM FOR CONFIGURING FIBRE CHANNEL PORTS
MP12109	MP12109C1	US	12/473,150	5/27/2009	8005105	8/23/2011	In Force	METHOD AND SYSTEM FOR CONFIGURING FIBRE CHANNEL PORTS
MP12110	MP12110	US	10/847,756	5/18/2004	7669190	2/23/2010	In Force	METHOD AND SYSTEM FOR EFFICIENTLY RECORDING PROCESSOR EVENTS IN HOST B
MP12112	MP12112	US	10/878,595	6/28/2004	7469267	12/23/2008	In Force	METHOD AND SYSTEM FOR HOST DEVICE EVENT SYNCHRONIZATION
MP12113	MP12113	US	29/209,313	7/14/2004	D520,863	5/16/2006	In Force	FIBER OPTIC CABLE RETENTION AND GUIDE CLIP
MP12114	MP12114	US	10/894,529	7/20/2004	7404020	7/22/2008	In Force	INTEGRATED FIBRE CHANNEL FABRIC CONTROLLER
MP12117	MP12117	US	10/927,170	8/25/2004	7308535	12/11/2007	In Force	SELF-TRIGGERING OUTGOING BUFFERS
MP12117	MP12117C1	US	11/933,860	11/1/2007	7500057	3/3/2009	In Force	SELF-TRIGERRING OUTGOING BUFFERS
MP12118	MP12118	US	10/931,851	1/9/2004	7522623	4/21/2009	In Force	METHOD AND SYSTEM FOR EFFICIENTLY USING BUFFER SPACE
MP12118	MP12118C1	US	12/407,153	3/19/2009	7924859	4/12/2011	In Force	METHOD AND SYSTEM FOR EFFICIENTLY USING BUFFER SPACE
MP12119	MP12119	US	10/931,850	1/9/2004	7761608	7/20/2010	In Force	METHOD AND SYSTEM FOR PROCESSING MARKERS, DATA INTEGRITY FIELDS AND DI
MP12120	MP12120	US	10/935,919	9/8/2004	7577772	8/18/2009	In Force	METHOD AND SYSTEM FOR OPTIMIZING DMA CHANNEL SELECTION
MP12122	MP12122	US	10/940,355	9/13/2004	7895390	2/22/2011	In Force	ENSURING BUFFER AVAILABILITY
MP12125	MP12125	US	10/956,955	10/1/2004	7676611	3/9/2010	In Force	METHOD AND SYSTEM FOR PROCESSING OUT OF ORDER FRAMES
MP12126	MP12126	US	10/956,501	10/1/2004	8295299	10/23/2012	In Force	HIGH SPEED FIBRE CHANNEL SWITCH ELEMENT
MP12126	MP12126C1	US	13/604,261	9/5/2012	8774206	7/8/2014	In Force	HIGH SPEED FIBRE CHANNEL SWITCH ELEMENT
MP12127	MP12127	US	10/956,502	10/1/2004	7593997	9/22/2009	In Force	METHOD AND SYSTEM FOR LUN REMAPPING IN FIBRE CHANNEL NETWORKS
MP12128	MP12128	US	10/957,465	10/1/2004	7930377	4/19/2011	In Force	METHOD AND SYSTEM FOR USING BOOT SERVERS IN NETWORKS
MP12129	MP12129	US	10/956,718	10/1/2004	7380030	5/27/2008	In Force	METHD AND SYSTEM FOR USING AN IN-LINE CREDIT EXTENDER WITH A HOST BUS A
MP12130	MP12130	US	10/956,717	1/10/2004	7411958	12/8/2008	In Force	METHOD AND SYSTEM FOR TRANSFERRING DATA DIRECTLY BETWEEN STORAGE DEV
MP12131	MP12131	US	10/961,463	8/10/2004	7340167	4/3/2008	In Force	FIBRE CHANNEL TRANSPARENT SWITCH FOR MIXED SWITCH FABRICS
MP12131	MP12131C1	US	12/031,585	2/14/2008	7542676	6/2/2009	In Force	FIBRE CHANNEL TRANSPARENT SWITCH FOR MIXED SWITCH FABRICS
MP12132	MP12132	US	10/963,287	10/11/2004	7512721	3/31/2009	In Force	METHOD AND APPARATUS FOR EFFICIENT DETERMINATION OF STATUS FROM DMA
MP12133	MP12133	US	10/994,829	11/22/2004	7398335	7/8/2008	In Force	METHOD AND SYSTEM FOR DMA OPTIMIZATION IN HOST BUS ADAPTERS
MP12134	MP12134	US	11/002,728	11/30/2004	7606998	10/20/2009	In Force	Store Instruction Ordering For Multi-Core Processor
MP12134	MP12134WO	WO	PCT/US2005/03171	9/1/2005	DNA		Pending	Store Instruction Ordering For Multi-Core Processor
MP12134	MP12134WOC	CN	2005800346066	9/1/2005	ZL20058003	8/26/2009	In Force	Store Instruction Ordering For Multi-Core Processor
MP12134	MP12134WOD	DE	05795368.9	9/1/2005	6020050529	10/25/2017	In Force	Store Instruction Ordering For Multi-Core Processor
MP12134	MP12134WOEP	EP	05795368.9	9/1/2005	1787194	10/25/2017	In Force	Store Instruction Ordering For Multi-Core Processor
MP12134	MP12134WOJP	JP	2007-531266	9/1/2005	JP5197010	2/15/2013	In Force	Store Instruction Ordering For Multi-Core Processor
MP12135	MP12135	US	11/005,490	12/6/2004	7895431	2/22/2011	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WO	WO	PCT/US2005/03121	9/1/2005	DNA		Pending	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOC	CN	2005800346009	9/1/2005	ZL20058003	2/8/2012	In Force	Data packet queuing, scheduling and ordering
MP12135	MP12135WOEP	EP	05796391.0	9/1/2005	1787212	2/13/2013	In Force	Packet Queuing, Scheduling And Ordering

PATENT
REEL: 057897 FRAME: 0511

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12135	MP12135WOEP	DE	05796391.0	9/1/2005	6020050381	2/13/2013	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOEP	FI	05796391.0	9/1/2005	1787212	2/13/2013	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOEP	FR	05796391.0	9/1/2005	1787212	2/13/2013	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOEP	GB	05796391.0	9/1/2005	1787212	2/13/2013	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOEP	SE	05796391.0	9/1/2005		2/13/2013	In Force	Packet Queuing, Scheduling And Ordering
MP12135	MP12135WOJP	JP	2007-531240	9/1/2005	JP4723586	4/15/2011	In Force	Packet Queuing, Scheduling And Ordering
MP12136	MP12136	US	11/015,343	12/17/2004	7941585	5/10/2011	In Force	Local Scratchpad And Data Caching System
MP12137	MP12137	US	11/018,055	12/21/2004	7164425	1/16/2007	In Force	METHOD AND SYSTEM FOR HIGH SPEED NETWORK APPLICATION
MP12138	MP12138	US	11/024,002	12/28/2004	7594081	9/22/2009	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WO	WO	PCT/US2005/03129	9/1/2005	DNA		Pending	Direct Access To Low-Latency Memory
MP12138	MP12138WOC	CN	2005800334834	9/1/2005	ZL20058003	12/8/2010	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	EP	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	CH	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	DE	05810485.2	9/1/2005	6020050454	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	FR	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	GB	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	IE	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12138	MP12138WOEP	SE	05810485.2	9/1/2005	1787193	12/10/2014	In Force	Direct Access To Low-Latency Memory
MP12139	MP12139C1	US	14/159,210	1/20/2014	9141548	9/22/2015	In Force	Method And Apparatus For Managing Write Back Cache
MP12140	MP12140	US	11/037,922	1/18/2005	7519058	4/14/2009	In Force	ADDRESS TRANSLATION IN FIBRE CHANNEL SWITCHES
MP12141	MP12141	US	11/039,189	1/20/2005	7392437	6/24/2008	In Force	METHOD AND SYSTEM FOR TESTING HOST BUS ADAPTERS
MP12143	MP12143WO	WO	PCT/US2005/03170	9/1/2005	DNA		Pending	Multiply Instructions For Modular Exponentiation
MP12147	MP12147	US	11/346,106	2/2/2006	7496745	2/24/2009	In Force	METHOD AND SYSTEM FOR MANAGING STORAGE AREA NETWORKS
MP12149	MP12149	US	11/355,622	2/16/2006	7694047	4/6/2010	In Force	METHOD AND SYSTEM FOR SHARING INPUT/OUTPUT DEVICES
MP12150	MP12150I1	US	11/097,024	4/1/2005	7420991	9/2/2008	In Force	TCP TIME STAMP PROCESSING IN HARDWARE BASED TCP OFFLOAD
MP12153	MP12153	US	11/100,063	6/4/2005	7231480	12/6/2007	In Force	METHOD AND SYSTEM FOR RECEIVER DETECTION IN PCI-EXPRESS DEVICES
MP12154	MP12154	US	11/220,899	9/7/2005	8301788	10/30/2012	In Force	Deterministic Finite Automata (DFA) Instruction
MP12155	MP12155	US	11/221,408	9/7/2005	8392590	3/5/2013	In Force	Deterministic Finite Automata (DFA) Processing
MP12155	MP12155WO	WO	PCT/US2005/03223	9/8/2005	DNA		Pending	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOC	CN	200580034214X	9/8/2005	ZL20058003	2/29/2012	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	EP	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	CH	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	DE	05810485.2	9/8/2005	6020050388	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	FI	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing

PATENT
REEL: 057897 FRAME: 0512

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12155	MP12155WOEP	FR	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	GB	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	IE	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12155	MP12155WOEP	SE	05812863.8	9/8/2005	1790148	3/27/2013	In Force	Deterministic finite Automata (DFA) Processing
MP12156	MP12156	US	11/224,728	9/12/2005	8560475	10/15/2013	In Force	Content Search Mechanism That Uses A Deterministic Finite Automata (DFA) Graph,
MP12156	MP12156-2	US	14/040,323	9/27/2013	8818921	8/26/2014	In Force	Content Search Mechanism That Uses A Deterministic Finite Automata (DFA) Graph
MP12156	MP12156C1	US	14/337,759	7/22/2014	9336328	5/10/2016	In Force	Content search mechanism that uses a deterministic finite automata (DFA) graph, a
MP12156	MP12156C1C1	US	15/134,919	4/21/2016	9652505	5/16/2017	In Force	Content Search Pattern Matching Using Deterministic Finite Automata (DFA) Graphs
MP12157	MP12157I1	US	11/335,189	1/18/2006	7558925	7/7/2009	In Force	Selective Replication Of Data Structures
MP12157	MP12157WO	WO	PCT/US2005/03223	9/9/2005	DNA		Pending	Selective Replication Of Data Structures
MP12157	MP12157WO2	WO	PCT/US2005/03180	9/9/2005	DNA		Pending	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2C	CH	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2C	CN	2005800304519	9/9/2005	ZL20058003	2/1/2012	In Force	Selective replication of data structure
MP12157	MP12157WO2	DE	05795143.6	9/9/2005	6020050517	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2	DK	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2E	EP	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2F	FI	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2F	FR	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2	GB	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2	NL	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12157	MP12157WO2S	SE	05795143.6	9/9/2005	1794979	4/12/2017	In Force	SELECTIVE REPLICATION OF DATA STRUCTURE
MP12158	MP12158	US	11/225,373	9/12/2005	7613813	11/3/2009	In Force	METHOD AND APPARATUS FOR REDUCING HOST OVERHEAD IN A SOCKET SERVER I
MP12158	MP12158C1	US	12/574,263	10/6/2009	7930349	4/19/2011	In Force	Method And Apparatus For Reducing Host Overhead In A Socket Server Implementati
MP12159	MP12159	US	11/218,727	9/2/2005	7535907	5/19/2009	In Force	TCP Engine
MP12162	MP12162	US	11/126,988	5/11/2005	7447618	11/4/2008	In Force	METHOD AND SYSTEM FOR ASIC SIMULATION
MP12163	MP12163	US	11/132,020	5/18/2005	7802031	9/21/2010	In Force	METHOD AND SYSTEM FOR HIGH SPEED NETWORK APPLICATION
MP12165	MP12165	US	11/140,891	5/31/2005	7168971	1/30/2007	In Force	GASKET RETAINER
MP12166	MP12166	US	11/201,036	8/10/2005	7565580	7/21/2009	In Force	METHOD AND SYSTEM FOR TESTING NETWORK DEVICE LOGIC
MP12167	MP12167	US	11/222,592	9/9/2005	7230549	12/6/2007	In Force	METHOD AND SYSTEM FOR SYNCHRONIZING BIT STREAMS FOR PCI EXPRESS DEVICE
MP12169	MP12169	US	11/223,693	9/9/2005	7639715	12/29/2009	In Force	DEDICATED APPLICATION INTERFACE FOR NETWORK SYSTEMS
MP12170	MP12170	US	11/222,936	9/9/2005	7577773	8/18/2009	In Force	METHOD AND SYSTEM FOR DMA OPTIMIZATION
MP12172	MP12172	US	11/252,524	10/18/2005	7447874	4/11/2008	In Force	METHOD AND SYSTEM FOR DESIGNING A FLEXIBLE HARDWARE STATE MACHINE
MP12173	MP12173	US	11/257,693	10/25/2005	7630876	12/8/2009	In Force	METHOD AND SYSTEM FOR FILTERING UNKNOWN VALUES IN ASIC DESIGN SIMULATI
MP12174	MP12174	US	11/291,430	12/1/2005	7920473	4/5/2011	In Force	METHOD AND SYSTEM FOR MANAGING TRANSMIT DESCRIPTORS IN A NETWORKING

PATENT
REEL: 057897 FRAME: 0513

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12175	MP12175	US	11/317,315	12/23/2005	7735099	6/8/2010	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK DATA
MP12176	MP12176	US	11/318,116	12/23/2005	8682799	3/25/2014	In Force	Method and system for port licensing in switches
MP12178	MP12178	US	11/328,358	9/1/2006	7594057	9/22/2009	In Force	METHOD AND SYSTEM FOR PROCESSING DMA REQUESTS
MP12180	MP12180	US	11/343,596	1/31/2006	8464238	6/11/2013	In Force	METHOD AND SYSTEM FOR MANAGING STORAGE AREA NETWORKS
MP12181	MP12181	US	11/357,515	2/17/2006	7668978	2/23/2010	In Force	METHOD AND SYSTEM FOR STORING FRAMES IN NETWORKS
MP12182	MP12182	US	11/362,690	2/27/2006	7518995	4/14/2009	In Force	METHOD AND SYSTEM FOR MANAGING FRAME FLOW IN FIBRE CHANNEL SYSTEMS
MP12183	MP12183	US	11/363,365	2/27/2006	7548560	6/16/2009	In Force	METHOD AND SYSTEM FOR CHECKING FRAME-LENGTH IN FIBRE CHANNEL FRAMES
MP12184	MP12184	US	11/376,703	3/14/2006	8009923	8/30/2011	In Force	METHOD AND SYSTEM FOR MOTION ESTIMATION WITH MULTIPLE VECTOR CANDID
MP12185	MP12185	US	11/376,955	3/16/2006	7525968	4/28/2009	In Force	METHOD AND SYSTEM FOR AUTO ROUTING FIBRE CHANNEL CLASS F FRAMES IN A F
MP12187	MP12187	US	11/378,838	3/17/2006	7461195	12/2/2008	In Force	METHOD AND SYSTEM FOR DYNAMICALLY ADJUSTING DATA TRANSFER RATES IN PCI
MP12188	MP12188	US	11/396,748	4/3/2006	7681102	3/16/2010	In Force	BYTE LEVEL PROTECTION IN PCI-EXPRESS DEVICES
MP12189	MP12189	US	11/430,704	5/9/2006	7447817	11/4/2008	In Force	METHOD AND SYSTEM FOR PROCESSING ARBITRATION REQUESTS
MP12190	MP12190	US	11/453,500	6/15/2006	7660302	2/9/2010	In Force	METHOD AND SYSTEM FOR INTER-FABRIC ROUTING
MP12192	MP12192	US	11/477,161	6/28/2006	7610482	10/27/2009	In Force	METHOD AND SYSTEM FOR MANAGING BOOT TRACE INFORMATION IN HOST BUS A
MP12193	MP12193	US	11/491,357	7/21/2006	7379837	5/27/2008	In Force	METHOD AND SYSTEM FOR TESTING INTEGRATED CIRCUITS
MP12194	MP12194	US	11/493,978	7/27/2006	8185960	5/22/2012	In Force	SYSTEM AND METHOD FOR MANAGING ACCESS TO ADAPTER FEATURES
MP12195	MP12195	US	11/461,387	7/31/2006	7764676	7/27/2010	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK INFORMATION
MP12196	MP12196	US	11/502,282	8/10/2006	7457887	11/25/2008	In Force	METHOD AND SYSTEM FOR PROCESSING ASYNCHRONOUS EVENT NOTIFICATIONS
MP12198	MP12198	US	11/469,377	8/31/2006	7669001	2/23/2010	In Force	METHOD AND SYSTEM FOR USING APPLICATION SPECIFIC INTEGRATED CIRCUITS
MP12199	MP12199	US	11/522,672	9/18/2006	7843846	11/30/2010	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK INFORMATION
MP12201	MP12201	US	11/533,873	9/21/2006	7773592	8/10/2010	In Force	METHOD AND SYSTEM FOR ROUTING NETWORK INFORMATION
MP12205	MP12205	US	11/555,180	10/31/2006	8055726	11/8/2011	In Force	METHOD AND SYSTEM FOR WRITING NETWORK DATA
MP12205	MP12205C1	US	13/241,012	9/22/2011	8676928	3/18/2014	In Force	METHOD AND SYSTEM FOR WRITING NETWORK DATA
MP12206	MP12206	US	11/555,123	10/31/2006	8601179	12/3/2013	In Force	METHOD AND SYSTEM FOR DATA TRANSFER
MP12208	MP12208	US	11/560,317	11/15/2006	7613816	11/3/2009	In Force	METHOD AND SYSTEM FOR ROUTING NETWORK INFORMATION
MP12210	MP12210	US	11/565,444	11/30/2006	7643505	1/5/2010	In Force	METHOD AND SYSTEM FOR REAL TIME COMPRESSION AND DECOMPRESSION
MP12212	MP12212	US	11/615,329	12/22/2006	7549005	6/16/2009	In Force	SYSTEM AND METHOD FOR MANAGING INTERRUPTS
MP12214	MP12214	US	11/669,573	1/31/2007	7668177	2/23/2010	In Force	METHOD AND SYSTEM FOR QUALITY OF SERVICE IN HOST BUS ADAPTERS
MP12217	MP12217	US	11/669,775	1/31/2007	7668162	2/23/2010	In Force	COMPRESSION AND DECOMPRESSION FOR NETWORK SYSTEMS
MP12217	MP12217C1	US	12/684,054	1/7/2010	7889730	2/15/2011	In Force	COMPRESSION AND DECOMPRESSION FOR NETWORK SYSTEMS
MP12219	MP12219WOB	BR	P10721380-8	2/28/2007			Pending	METHOD OF ALLOCATING COMMUNICATIONS RESOURCES AND SCHEDULER THEREF
MP12219	MP12219WOID	ID	WO0200902395	2/28/2007	P0032751	1/21/2013	In Force	METHOD OF ALLOCATING COMMUNICATIONS RESOURCES AND SCHEDULER THEREF
MP12219	MP12219WOIN	IN	1660/MUMNP/200	2/28/2007			Pending	METHOD OF ALLOCATING COMMUNICATIONS RESOURCES AND SCHEDULER THEREF
MP12220	MP12220WOIN	IN	1718/MUMNP/200	3/5/2007			Pending	CHANNEL PROFILER AND METHOD OF PROFILING AN INCOMING SIGNAL

PATENT
REEL: 057897 FRAME: 0514

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12220	MP12220WOJP	JP	2009-552286	3/5/2007			Pending	CHANNEL PROFILER AND METHOD OF PROFILING AN INCOMING SIGNAL
MP12221	MP12221CN	CN	200810081776.5	3/13/2008	ZL20081008	9/14/2011	In Force	Reliable Network Packet Dispatcher With Interleaving Multi-Port Circular Retry Queu
MP12222	MP12222	US	11/686,417	3/15/2007	7693070	4/6/2010	In Force	CONGESTION REDUCING RELIABLE TRANSPORT PACKET RETRY ENGINE
MP12223	MP12223	US	11/742,282	4/30/2007	8387073	2/26/2013	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK PACKETS
MP12224	MP12224	US	11/694,698	3/30/2007	8185715	5/22/2012	In Force	METHOD AND SYSTEM FOR MANAGING METADATA IN STORAGE VIRTUALIZATION E
MP12225	MP12225WOIN	IN	2098/MUMNP/200	5/2/2007			Pending	METHOD AND APPARATUS FOR CORRECTING LINEAR ERROR PHASE OF AN OFDM SI
MP12225	MP12225WOJP	JP	2010-504875	5/2/2007	JP5460579	4/2/2014	In Force	METHOD AND APPARATUS FOR CORRECTING LINEAR ERROR PHASE OF AN OFDM SI
MP12225	MP12225WOU	US	12/598,544	5/2/2007	8340205	12/25/2012	In Force	METHOD AND APPARATUS FOR CORRECTING LINEAR ERROR PHASE OF AN OFDM SI
MP12226	MP12226	US	11/752,212	5/22/2007	8250203	8/21/2012	In Force	METHOD AND SYSTEM FOR NETWORK TRAFFIC MONITORING
MP12227	MP12227	US	11/761,279	6/11/2007	8095978	1/10/2012	In Force	METHOD AND SYSTEM FOR MANAGING PORTS IN A HOST BUS ADAPTER
MP12228	MP12228	US	11/762,578	6/13/2007	8102769	1/24/2012	In Force	METHOD AND SYSTEM FOR NETWORK COMMUNICATION
MP12228	MP12228C1	US	13/330,085	12/19/2011	8792351	7/29/2014	In Force	METHOD AND SYSTEM FOR NETWORK COMMUNICATION
MP12229	MP12229	US	11/965,037	12/27/2007	8010809	8/30/2011	In Force	METHOD AND SYSTEM FOR SECURING NETWORK DATA
MP12229	MP12229C1	US	13/190,165	7/25/2011	8261099	9/4/2012	In Force	METHOD AND SYSTEM FOR SECURING NETWORK DATA
MP12230	MP12230	US	12/111,057	4/28/2008	8904077	12/2/2014	In Force	POWER MANAGEMENT FOR HOST BUS ADAPTERS
MP12232	MP12232	US	11/842,830	8/21/2007	8411677	4/2/2013	In Force	METHOD AND SYSTEM FOR PROCESSING LAYERED NETWORKING PROTOCOL PACKET
MP12234	MP12234	US	11/849,122	8/31/2007	7605658	10/20/2009	In Force	Resistively Loaded Single Stage Differential Amplifier Having Zero Volt Common Mod
MP12236	MP12236	US	11/864,651	9/28/2007	7903558	3/8/2011	In Force	METHOD AND SYSTEM FOR MONITORING A NETWORK LINK IN NETWORK SYSTEMS
MP12236	MP12236C1	US	13/026,007	2/11/2011	8441929	5/14/2013	In Force	METHOD AND SYSTEM FOR MONITORING A NETWORK LINK IN NETWORK SYSTEMS
MP12238	MP12238	US	11/982,391	11/1/2007	8086609	12/27/2011	In Force	Graph Caching
MP12238	MP12238C1	US	13/311,244	12/5/2011	9787693	10/10/2017	In Force	Graph Caching
MP12239	MP12239	US	11/982,433	11/1/2007	8819217	8/26/2014	In Force	Intelligent Graph Walking
MP12240	MP12240WOIN	IN	3312/CHENP/2010	11/6/2007			Pending	METHOD AND SYSTEM FOR DIGITALLY CORRECTING SAMPLING EFFECTS
MP12241	MP12241	US	12/052,130	3/20/2008	7908404	3/15/2011	In Force	METHOD AND SYSTEM FOR MANAGING NETWORK AND STORAGE DATA
MP12242	MP12242	US	11/986,975	11/27/2007	7949683	5/24/2011	In Force	Method And Apparatus For Traversing A Compressed Deterministic Finite Automata (
MP12242	MP12242WO	WO	PCT/US2008/01154	10/7/2008	DNA		Pending	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12242	MP12242WOEP	EP	08853776.6	10/7/2008	2215563	5/4/2016	In Force	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12242	MP12242WOEP	DE	08853776.6	10/7/2008	602008044C	5/4/2016	In Force	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12242	MP12242WOEP	FI	08853776.6	10/7/2008	2215563	5/4/2016	In Force	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12242	MP12242WOEP	FR	08853776.6	10/7/2008	2215563	5/4/2016	In Force	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12242	MP12242WOEP	SE	08853776.6	10/7/2008	2215563	5/4/2016	In Force	Method And Apparatus For Traversing A Deterministic Finite Automata (DFA) Graph
MP12243	MP12243	US	11/986,970	11/27/2007	8180803	5/15/2012	In Force	Deterministic Finite Automata (DFA) Graph Compression
MP12243	MP12243WO	WO	PCT/US2008/01154	10/7/2008	DNA		Pending	Deterministic Finite Automata (DFA) Graph Compression
MP12243	MP12243WOEP	EP	08854609.8	10/7/2008	2215565	5/4/2016	In Force	Deterministic Finite Automata (DFA) Graph Compression

PATENT
REEL: 057897 FRAME: 0515

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12243	MP12243WOEP	DE	08854609.8	10/7/2008	6020080441	5/4/2016	In Force	Deterministic Finite Automata (DFA) Graph Compression
MP12243	MP12243WOEP	FI	08854609.8	10/7/2008	2215565	5/4/2016	In Force	Deterministic Finite Automata (DFA) Graph Compression
MP12243	MP12243WOEP	FR	08854609.8	10/7/2008	2215565	5/4/2016	In Force	Deterministic Finite Automata (DFA) Graph Compression
MP12243	MP12243WOEP	SE	08854609.8	10/7/2008	2215565	5/4/2016	In Force	Deterministic Finite Automata (DFA) Graph Compression
MP12245	MP12245	US	11/963,566	12/21/2007	7720064	5/18/2010	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK AND STORAGE DATA
MP12245	MP12245C1	US	12/751,955	3/31/2010	8225004	7/17/2012	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK AND STORAGE DATA
MP12246	MP12246	US	11/966,857	12/28/2007	7719969	5/18/2010	In Force	SYSTEM AND METHOD FOR ASSIGNING NETWORK DEVICE PORT ADDRESS BASED ON
MP12248	MP12248	US	12/019,094	1/24/2008	7609710	10/27/2009	In Force	METHOD AND SYSTEM FOR CREDIT MANAGEMENT IN A NETWORKING SYSTEM
MP12251	MP12251	US	12/034,913	2/21/2008	7962675	6/14/2011	In Force	METHOD AND SYSTEM FOR COMMUNICATING WITH A HOST BUS ADAPTER
MP12252	MP12252	US	12/392,004	2/24/2009	8677144	3/18/2014	In Force	Secure Software And Hardware Association Technique
MP12253	MP12253	US	12/037,847	2/26/2008	8116206	2/14/2012	In Force	METHOD AND SYSTEM FOR ROUTING FRAMES IN A NETWORK
MP12254	MP12254	US	12/039,604	2/28/2008	7895300	2/22/2011	In Force	SYSTEMS AND METHODS FOR TESTING DEVICE PORTS IN A STORAGE AREA NETWOR
MP12255	MP12255	US	12/082,246	4/9/2008	8358699	1/22/2013	In Force	METHOD AND SYSTEM FOR SELECTION OF REFERENCE PICTURE AND MODE DECISIO
MP12256	MP12256C1	US	14/144,252	12/30/2013	8891706	11/18/2014	In Force	SYSTEM AND METHOD FOR OPTIMIZING USE OF CHANNEL STATE INFORMATION
MP12256	MP12256WOU	US	12/988,348	4/17/2008	8619923	12/31/2013	In Force	SYSTEM AND METHOD FOR OPTIMIZING USE OF CHANNEL STATE INFORMATION
MP12258	MP12258	US	12/135,973	6/9/2008	7773629	8/10/2010	In Force	METHOD AND SYSTEM FOR NETWORK PORT ADDRESSING
MP12259	MP12259	US	12/214,789	6/20/2008	8471601	6/25/2013	In Force	Single-Ended to Differential Converter
MP12260	MP12260	US	12/489,241	6/22/2009	8296386	10/23/2012	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK PACKETS
MP12260	MP12260C1	US	13/610,095	9/11/2012	8867537	10/21/2014	In Force	METHOD AND SYSTEM FOR PROCESSING NETWORK PACKETS
MP12261	MP12261	US	12/165,464	6/30/2008	7765317	7/27/2010	In Force	SYSTEM AND METHODS FOR LOCATING FPDU HEADERS WHEN MARKERS ARE DISABL
MP12262	MP12262	US	12/505,430	7/17/2009	8351442	1/8/2013	In Force	METHOD AND SYSTEM FOR NETWORK COMMUNICATION
MP12264	MP12264	US	12/536,336	8/5/2009	8793399	7/29/2014	In Force	METHOD AND SYSTEM FOR ACCELERATING NETWORK PACKET PROCESSING
MP12265	MP12265	US	12/539,156	8/11/2009	8391300	3/5/2013	In Force	CONFIGURABLE SWITCH ELEMENT AND METHODS THEREOF
MP12265	MP12265C1	US	13/758,543	2/4/2013	8976800	3/10/2015	In Force	CONFIGURABLE SWITCH ELEMENT AND METHODS THEREOF
MP12266	MP12266	US	12/229,617	8/25/2008	8176300	5/8/2012	In Force	Method And Apparatus For Content Based Searching
MP12267	MP12267	US	12/547,414	8/25/2009	8200473	6/12/2012	In Force	EMULATION OF MULTIPLE MDIO MANAGEABLE DEVICES
MP12268	MP12268	US	12/200,649	8/28/2008	7667985	2/23/2010	In Force	COMPUTER NETWORK DEVICE AND METHOD OF ASSEMBLY
MP12269	MP12269	US	12/201,304	8/29/2008	7646602	1/12/2010	In Force	APPARATUS AND METHODS FOR COOLING NETWORK SWITCHES
MP12270	MP12270	US	12/201,359	8/29/2008	7675750	3/9/2010	In Force	APPARATUS AND METHODS FOR COOLING NETWORK SWITCHES
MP12271	MP12271	US	12/586,169	9/17/2009	7961033	6/14/2011	In Force	DLL-Based Temperature Sensor
MP12273	MP12273	US	12/277,129	11/24/2008	8473523	6/25/2013	In Force	Deterministic Finite Automata Graph Traversal With Nodal Bit Mapping
MP12273	MP12273C1	US	13/905,711	5/30/2013	8886680	11/11/2014	In Force	Deterministic Finite Automata Graph Traversal With Nodal Bit Mapping
MP12273	MP12273C1C1	US	14/516,807	10/17/2014	9495479	11/15/2016	In Force	Traversal With Arc Configuration Information
MP12276	MP12276	US	12/410,294	3/24/2009	7907414	3/15/2011	In Force	NETWORK DEVICE HAVING LEVERS AND ASSOCIATED METHODS

PATENT
REEL: 057897 FRAME: 0516

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12278	MP12278	US	12/556,064	9/9/2009	8068482	11/29/2011	In Force	METHOD AND SYSTEM FOR NETWORK SWITCH ELEMENT
MP12278	MP12278C1	US	13/273,008	10/13/2011	8873546	10/28/2014	In Force	METHOD AND SYSTEM FOR NETWORK SWITCH ELEMENT
MP12279	MP12279	US	12/412,050	3/26/2009	9094343	7/28/2015	In Force	METHOD AND SYSTEM FOR TAKING A NETWORK PORT OFFLINE
MP12280	MP12280	US	12/411,176	3/25/2009	7907546	3/15/2011	In Force	METHOD AND SYSTEM FOR PORT NEGOTIATION
MP12281	MP12281	US	12/615,152	11/9/2009	8116311	2/14/2012	In Force	METHOD AND SYSTEM FOR TAG ARBITRATION IN SWITCHES
MP12282	MP12282	US	12/423,626	4/14/2009	8089971	1/3/2012	In Force	METHOD AND SYSTEM FOR TRANSMITTING FLOW CONTROL INFORMATION
MP12284	MP12284	US	12/415,873	3/31/2009	8060682	11/15/2011	In Force	METHOD AND SYSTEM FOR MULTI-LEVEL SWITCH CONFIGURATION
MP12288	MP12288	US	12/315,080	11/26/2008	8601139	12/3/2013	In Force	Multiple Core Session Initiation Protocol (SIP)
MP12290	MP12290	US	12/552,222	9/1/2009	8155022	4/10/2012	In Force	METHOD AND SYSTEM FOR CONTROLLING POWER CONSUMPTION IN NETWORK NO
MP12291	MP12291	US	12/731,065	3/24/2010	8351448	1/8/2013	In Force	METHOD AND SYSTEM FOR EXTENDED PORT ADDRESSING
MP12291	MP12291C1	US	13/711,380	12/11/2012	9071558	6/30/2015	In Force	METHOD AND SYSTEM FOR EXTENDED PORT ADDRESSING
MP12292	MP12292	US	12/410,277	3/24/2009	8068338	11/29/2011	In Force	NETWORK DEVICE WITH BAFFLE FOR REDIRECTING COOLING AIR AND ASSOCIATED
MP12293	MP12293	US	12/551,302	8/31/2009	8978052	3/10/2015	In Force	SYSTEM AND METHODS FOR INTER-DRIVER COMMUNICATION
MP12295	MP12295	US	12/774,574	5/5/2010	8705351	4/22/2014	In Force	METHOD AND SYSTEM FOR LOAD BALANCING IN NETWORKS
MP12296	MP12296	US	12/471,331	5/22/2009	8069293	11/29/2011	In Force	FLEXIBLE SERVER NETWORK CONNECTION UPGRADE SYSTEMS AND METHODS
MP12298	MP12298C1	US	13/447,652	4/16/2012	8996730	3/31/2015	In Force	SYSTEM AND METHOD TO RESTORE MAXIMUM PAYLOAD SIZE IN A NETWORK ADAP
MP12299	MP12299	US	12/572,835	10/2/2009	8504750	8/6/2013	In Force	SYSTEM AND METHOD TO PROCESS EVENT REPORTING IN AN ADAPTER
MP12299	MP12299C1	US	13/856,848	4/4/2013	9043519	5/26/2015	In Force	SYSTEM AND METHOD TO PROCESS EVENT REPORTING IN AN ADAPTER
MP12304	MP12304	US	12/544,658	8/20/2009	8065454	11/22/2011	In Force	SYSTEM AND METHOD FOR MAPPING FUNCTIONS TO AND FROM NETWORK DEVICE
MP12304	MP12304D1	US	13/221,737	8/30/2011	8225018	7/17/2012	In Force	SYSTEM AND METHOD FOR MAPPING FUNCTIONS TO AND FROM NETWORK DEVICE
MP12305	MP12305	US	12/859,690	8/19/2010	8706905	4/22/2014	In Force	METHOD AND SYSTEM FOR ROUTING INFORMATION IN A NETWORK
MP12306	MP12306	US	12/572,810	10/2/2009	8671228	3/11/2014	In Force	SYSTEM AND METHODS FOR MANAGING VIRTUAL ADAPTER INSTANCES
MP12307	MP12307	US	12/651,270	12/31/2009	7970927	6/28/2011	In Force	CONCURRENT TRANSMIT PROCESSING
MP12307	MP12307C1	US	13/111,475	5/19/2011	8275903	9/25/2012	In Force	CONCURRENT TRANSMIT PROCESSING
MP12309	MP12309	US	12/691,629	1/21/2010	9329794	5/3/2016	In Force	SYSTEM AND METHODS FOR DATA MIGRATION
MP12310	MP12310	US	12/695,648	1/28/2010	8356194	1/15/2013	In Force	METHOD AND APPARATUS FOR ESTIMATING OVERSHOOT POWER AFTER ESTIMATIN
MP12310	MP12310D1	US	13/713,650	12/13/2012	8868949	10/21/2014	In Force	Method And Apparatus For Power Control
MP12310	MP12310D1C1	US	14/488,724	9/17/2014	9703351	7/11/2017	In Force	Method And Apparatus For Power Control
MP12310	MP12310WO	WO	PCT/US2011/02221	1/24/2011	DNA		Pending	Method And Apparatus For Power Control
MP12310	MP12310WOEP	EP	11703077.5	1/24/2011	2529282	11/4/2015	In Force	Method And Apparatus For Power Control
MP12310	MP12310WOEP	DE	11703077.5	1/24/2011	602011021J	11/4/2015	In Force	Method And Apparatus For Power Control
MP12310	MP12310WOEP	SE	11703077.5	1/24/2011	2529282	11/4/2015	In Force	Method And Apparatus For Power Control
MP12310	MP12310WOJP	JP	2012-551212	1/24/2011	JP5827242	12/2/2015	In Force	METHOD AND APPARATUS FOR POWER CONTROL
MP12310	MP12310WOJP	JP	2015-074985	4/1/2015	JP6154843	6/9/2017	In Force	POWER CONTROL METHOD AND POWER CONTROL APPARATUS

PATENT
REEL: 057897 FRAME: 0517

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12313	MP12313	US	12/730,139	3/23/2010	8406152	3/26/2013	In Force	SYSTEM AND METHODS FOR PRESENTING STORAGE
MP12313	MP12313C1	US	13/770,828	2/19/2013	8873430	10/28/2014	In Force	SYSTEM AND METHODS FOR PRESENTING STORAGE
MP12314	MP12314	US	12/759,316	4/13/2010	8307111	11/6/2012	In Force	SYSTEMS AND METHODS FOR BANDWIDTH SCAVENGING AMONG A PLURALITY OF A
MP12314	MP12314C1	US	13/644,203	10/3/2012	9003038	4/7/2015	In Force	SYSTEMS AND METHODS FOR BANDWIDTH SCAVENGING AMONG A PLURALITY OF A
MP12315	MP12315	US	13/090,882	4/20/2011	8661266	2/25/2014	In Force	SYSTEM AND METHOD FOR SECURE DEVICE KEY STORAGE
MP12316	MP12316	US	12/769,463	4/28/2010	8826271	9/2/2014	In Force	Method And Apparatus For A Virtual System On Chip
MP12316	MP12316C1	US	14/452,873	8/6/2014	9378033	6/28/2016	In Force	Method And Apparatus For A Virtual System On Chip
MP12316	MP12316C1C1	US	15/192,214	6/24/2016	9665300	5/30/2017	In Force	Method And Apparatus For Virtualization
MP12316	MP12316C1C1C	US	15/499,177	4/27/2017	9823868	11/21/2017	In Force	Method And Apparatus For Virtualization
MP12316	MP12316C2	US	14/452,878	8/6/2014	10146463	12/4/2018	In Force	Method And Apparatus For A Virtual System On Chip
MP12320	MP12320	US	12/774,608	5/5/2010	9781477	10/3/2017	In Force	SYSTEM AND METHOD FOR LOW-LATENCY MULTIMEDIA STREAMING
MP12321	MP12321	US	12/795,563	6/7/2010	8315268	11/20/2012	In Force	METHOD AND SYSTEM FOR COMMUNICATION WITH AN ADAPTER
MP12325	MP12325	US	12/826,105	6/29/2010	8250252	8/21/2012	In Force	SYSTEM AND METHODS FOR USING A DMA MODULE FOR A PLURALITY OF VIRTUAL
MP12325	MP12325C1	US	13/489,016	6/5/2012	8392629	3/5/2013	In Force	SYSTEM AND METHODS FOR USING A DMA MODULE FOR A PLURALITY OF VIRTUAL
MP12326	MP12326	US	12/914,852	10/28/2010	8478909	7/2/2013	In Force	METHOD AND SYSTEM FOR COMMUNICATION ACROSS MULTIPLE CHANNELS
MP12327	MP12327	US	12/848,184	8/1/2010	8544106	9/24/2013	In Force	SYSTEM AND METHOD FOR ENABLING ACCESS TO A PROTECTED HARDWARE RESOU
MP12330	MP12330	US	13/216,598	8/24/2011	8441922	5/14/2013	In Force	METHOD AND SYSTEM FOR CONGESTION MANAGEMENT IN NETWORKS
MP12331	MP12331	US	12/901,409	10/8/2010	8510527	8/13/2013	In Force	SYSTEM AND METHODS FOR MIGRATING INFORMATION FROM SOURCE STORAGE T
MP12332	MP12332	US	12/902,020	10/11/2010	8301817	10/30/2012	In Force	RING BUS FOR SHARING RESOURCES AMONG MULTIPLE ENGINES
MP12333	MP12333	US	12/901,994	10/11/2010	8386644	2/26/2013	In Force	SYSTEMS AND METHODS FOR EFFICIENTLY PROCESSING LARGE DATA SEGMENTS
MP12335	MP12335	US	12/941,621	11/8/2010	8566573	10/22/2013	In Force	SELECTABLE INITIALIZATION FOR ADAPTERS
MP12337	MP12337	US	12/964,295	12/9/2010	9426097	8/23/2016	In Force	FACILITATING COMMUNICATION BETWEEN DEVICES IN A NETWORK
MP12338	MP12338	US	13/325,943	12/14/2011	8977944	3/10/2015	In Force	DRAM Address Protection
MP12338	MP12338C1	US	14/629,770	2/24/2015	9239753	1/19/2016	In Force	DRAM Address Protection
MP12339	MP12339	US	13/326,091	12/14/2011	9596193	3/14/2017	In Force	Messaging With Flexible Transmit Ordering
MP12339	MP12339D1	US	14/026,293	9/13/2013	9065781	6/23/2015	In Force	Messaging With Flexible Transmit Ordering
MP12339	MP12339D1C1	US	14/746,674	6/22/2015	9264385	2/16/2016	In Force	Messaging With Flexible Transmit Ordering
MP12343	MP12343	US	13/369,652	2/9/2012	8525572	9/3/2013	In Force	Level-Up Shifter Circuit
MP12343	MP12343I1	US	13/968,523	8/16/2013	8896360	11/25/2014	In Force	Level-Up Shifter Circuit For High Speed And Low Power Applications
MP12344	MP12344	US	13/369,562	2/9/2012	8519785	8/27/2013	In Force	Differential Amplifier With Duty Cycle Compensation
MP12345	MP12345	US	13/397,550	2/15/2012	8536944	9/17/2013	In Force	Differential Amplifier With De-Emphasis
MP12346	MP12346	US	13/397,303	2/15/2012	8634509	1/21/2014	In Force	Synchronized Clock Phase Interpolator
MP12347	MP12347	US	13/396,824	2/15/2012	9263151	2/16/2016	In Force	Memory Interface With Selectable Evaluation Modes
MP12348	MP12348	US	13/369,579	2/9/2012	8513994	8/20/2013	In Force	State Machine For Deskew Delay Locked Loop

PATENT
REEL: 057897 FRAME: 0518

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12349	MP12349	US	13/370,784	2/10/2012	9143140	9/22/2015	In Force	Multi-Function Delay Locked Loop
MP12349	MP12349C1	US	14/639,476	3/5/2015	9306584	4/5/2016	In Force	Multi-Function Delay Locked Loop
MP12350	MP12350	US	13/029,018	2/16/2011	8682632	3/25/2014	In Force	SIMULATION SYSTEM AND METHOD THEREOF
MP12352	MP12352	US	13/035,114	2/25/2011	8880732	11/4/2014	In Force	METHOD AND SYSTEM FOR APPLICATION ISOLATION
MP12353	MP12353	US	13/168,395	6/24/2011	9398033	7/19/2016	In Force	Regular Expression Processing Automaton
MP12354	MP12354	US	13/087,817	4/15/2011	8456331	6/4/2013	In Force	System And Method Of Compression And Decompression
MP12354	MP12354C1	US	13/888,851	5/7/2013	9054729	6/9/2015	In Force	System And Method Of Compression And Decompression
MP12355	MP12355	US	13/067,051	5/4/2011	8831108	9/9/2014	In Force	Low latency rate control system and method
MP12355	MP12355D1	US	14/480,469	9/8/2014	9445107	9/13/2016	In Force	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355HK	HK	14104540.1	5/4/2012	1191485B	11/24/2017	In Force	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355JPD1	JP	2016-029840	2/19/2016	JP6226490	11/8/2017	In Force	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355JPD2	JP	2017-143464	7/25/2017			Pending	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355WO	WO	PCT/US2012/03664	5/4/2012	DNA		Pending	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355WOC	CN	201280031677.0	5/4/2012	ZL20128003	2/1/2017	In Force	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355WOJP	JP	2014-509498	5/4/2012			Pending	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12355	MP12355WOKR	KR	10-2013-7032245	5/4/2012	101809306	12/14/2017	In Force	LOW LATENCY RATE CONTROL SYSTEM AND METHOD
MP12356	MP12356	US	13/067,050	5/4/2011	9025672	5/5/2015	In Force	ON-DEMAND INTRA-REFRESH FOR END-TO END CODED VIDEO TRANSMISSION SYSTE
MP12356	MP12356HK	HK	14106723.5	5/4/2012	1193292B	12/8/2017	In Force	ON-DEMAND INTRA-REFRESH FOR END-TO-END CODED VIDEO TRANSMISSION SYSTE
MP12356	MP12356WO	WO	PCT/US2012/03664	5/4/2012	DNA		Pending	ON-DEMAND INTRA-REFRESH FOR END-TO-END CODED VIDEO TRANSMISSION SYSTE
MP12356	MP12356WOC	CN	201280031662.4	5/4/2012	ZL20128003	2/15/2017	In Force	ON-DEMAND INTRA-REFRESH FOR END-TO-END CODED VIDEO TRANSMISSION SYSTE
MP12356	MP12356WOJP	JP	2014-509499	5/4/2012	JP5784823	9/24/2015	In Force	ON-DEMAND INTRA-REFRESH FOR END-TO-END CODED VIDEO TRANSMISSION SYSTE
MP12356	MP12356WOKR	KR	10-2013-7032246	5/4/2012		3/6/2019	In Force	ON-DEMAND INTRA-REFRESH FOR END-TO-END CODED VIDEO TRANSMISSION SYSTE
MP12359	MP12359	US	13/105,401	5/11/2011	8350732	1/8/2013	In Force	Compression With Adjustable Quality/Bandwidth Capability
MP12360	MP12360	US	13/168,450	6/24/2011	9858051	1/2/2018	In Force	Regex Compiler
MP12360	MP12360HK	HK	14106732.4	6/20/2012	1193278	3/9/2018	In Force	Compiler For Regular Expressions
MP12360	MP12360WO	WO	PCT/US2012/04330	6/20/2012	DNA		Pending	Compiler For Regular Expressions
MP12360	MP12360WOC	CN	2012800387992	6/20/2012	ZL20128003	5/3/2017	In Force	Compiler For Regular Expressions
MP12360	MP12360WOC	CN	2017102583709	6/20/2012	ZL20128003	5/3/2017	In Force	Compiler For Regular Expressions
MP12360	MP12360WOD	DE	112012002624.1	6/20/2012			Pending	Compiler For Regular Expressions
MP12360	MP12360WOKR	KR	1020167020582	6/20/2012		7/17/2018	In Force	Compiler For Regular Expressions
MP12361	MP12361	US	13/168,323	6/24/2011	8990259	3/24/2015	In Force	Anchored Patterns
MP12361	MP12361C1	US	14/632,448	2/26/2015	9514246	12/6/2016	In Force	Anchored Patterns
MP12361	MP12361WO	WO	PCT/US2012/04333	6/20/2012	DNA		Pending	Anchored Patterns
MP12361	MP12361WOKR	KR	1020147001978	6/20/2012		7/14/2015	In Force	Anchored Patterns

PATENT
REEL: 057897 FRAME: 0519

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12362	MP12362	US	13/067,880	7/1/2011	9025665	5/5/2015	In Force	Video encoder bit estimator for macroblock encoding
MP12362	MP12362D1	US	14/329,843	7/11/2014	9094669	7/28/2015	In Force	VIDEO ENCODER BIT ESTIMATOR FOR MACROBLOCK ENCODING
MP12363	MP12363	US	13/181,270	7/12/2011	8488601	7/16/2013	In Force	METHOD AND SYSTEM FOR LINK AGGREGATION
MP12364	MP12364	US	13/181,251	7/12/2011	8467395	6/18/2013	In Force	METHOD AND SYSTEM FOR LINK AGGREGATION
MP12365	MP12365	US	13/193,462	7/28/2011	9071544	6/30/2015	In Force	METHOD AND SYSTEM FOR MANAGING NETWORK ELEMENTS
MP12366	MP12366	US	13/565,271	8/2/2012	10277510	4/30/2019	In Force	System and Method for Storing Lookup Request Rules in Multiple Memories
MP12367	MP12367	US	13/565,784	8/2/2012	8937952	1/20/2015	In Force	Packet Classification
MP12367	MP12367C1	US	13/664,015	10/30/2012	8934488	1/13/2015	In Force	Identifying Duplication in Decision Trees
MP12367	MP12367C1I1	US	13/831,487	3/14/2013	9208438	12/8/2015	In Force	Duplication in Decision Trees
MP12367	MP12367C2	US	13/686,269	11/27/2012	8937954	1/20/2015	In Force	Decision Tree Level Merging
MP12367	MP12367C3	US	14/570,626	12/15/2014	9191321	11/17/2015	In Force	Packet Classification
MP12367	MP12367HK	HK	14107043.6	8/2/2012	1193686	6/1/2018	In Force	Packet Classification By An Optimised Decision Tree
MP12367	MP12367WO	WO	PCT/US2012/04940	8/2/2012	DNA		Pending	Packet Classification By An Optimised Decision Tree
MP12367	MP12367WOC	CN	201280048417.4	8/2/2012	ZL20128004	8/25/2017	In Force	Packet Classification By An Optimised Decision Tree
MP12368	MP12368	US	13/565,389	8/2/2012	9596222	3/14/2017	In Force	Method and apparatus encoding a rule for a lookup request in a processor
MP12369	MP12369	US	13/565,406	8/2/2012	9344366	5/17/2016	In Force	System and method for rule matching in a processor
MP12369	MP12369C1	US	15/145,052	5/3/2016	9866540	1/9/2018	In Force	System And Method For Rule Matching In A Processor
MP12370	MP12370	US	13/565,727	8/2/2012	8711861	4/29/2014	In Force	Lookup Front End Packet Input Processor
MP12370	MP12370C1	US	13/599,276	8/30/2012	9729527	8/8/2017	In Force	Lookup Front End Packet Input Processor
MP12370	MP12370C2	US	14/138,931	12/23/2013	9031075	5/12/2015	In Force	Lookup Front End Packet Input Processor
MP12370	MP12370WO	WO	PCT/US2012/04940	8/2/2012	DNA		Pending	LOOKUP FRONT END INPUT PROCESSOR
MP12370	MP12370WOKR	KR	1020147005800	8/2/2012		12/17/2014	In Force	LOOKUP FRONT END INPUT PROCESSOR
MP12371	MP12371	US	13/565,767	8/2/2012	8606959	12/10/2013	In Force	Lookup Front End Packet Output Processor
MP12371	MP12371C1	US	14/082,365	11/18/2013	9497117	11/15/2016	In Force	Lookup Front End Packet Output Processor
MP12371	MP12371WO	WO	PCT/US2012/04940	8/2/2012	DNA		Pending	Lookup Front End Output Processor
MP12371	MP12371WOJP	JP	2014-524092	8/2/2012	JP5657840	1/21/2015	In Force	LOOKUP FRONT END PACKET INPUT PROCESSOR
MP12372	MP12372	US	13/565,741	8/2/2012	9391892	7/12/2016	In Force	Method and apparatus for managing transport operations to a cluster within a proce
MP12372	MP12372-2	US	13/565,743	8/2/2012	9319316	4/19/2016	In Force	Method and apparatus for managing transfer of transport operations from a cluster i
MP12372	MP12372-3	US	13/565,746	8/2/2012	9525630	12/20/2016	In Force	Method and Apparatus for Assigning Resources Used To Manage Transport Operatio
MP12372	MP12372-4	US	13/565,749	8/2/2012	8954700	2/10/2015	In Force	Method and Apparatus for Managing Processing Thread Migration Between Clusters
MP12372	MP12372-4C1	US	14/592,384	1/8/2015	9531690	12/27/2016	In Force	Method and Apparatus for Managing Processing Thread Migration Between Clusters
MP12373	MP12373	US	13/565,775	8/2/2012	9137340	9/15/2015	In Force	Incremental Update
MP12373	MP12373CN	CN	2012800482910	8/2/2012	ZL20128004	12/14/2018	In Force	Incremental Update of Rules for Packet Classification
MP12373	MP12373DE	DE	102014 001 498.3	2/5/2014			Pending	Incremental Update Heuristics

PATENT
REEL: 057897 FRAME: 0520

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12373	MP12373HK	HK	14111478.2	2/8/2012			Pending	Incremental Update of Rules for Packet Classification
MP12373	MP12373I1	US	13/831,232	3/14/2013	9183244	11/10/2015	In Force	Rule Modification in Decision Trees
MP12373	MP12373I2	US	13/831,191	3/14/2013	10229139	3/12/2019	In Force	Incremental Update Heuristics
MP12373	MP12373WO	WO	PCT/US2012/04940	8/2/2012	DNA		Pending	Incremental Update of Rules for Packet Classification
MP12374	MP12374	US	13/565,735	8/2/2012	9065860	6/23/2015	In Force	Method And Apparatus For Multiple Access Of Plural Memory Banks
MP12374	MP12374-2	US	13/565,736	8/2/2012	8966152	2/24/2015	In Force	On-Chip Memory (OCM) Physical Bank Parallelism
MP12375	MP12375	US	13/565,459	8/2/2012	8719331	5/6/2014	In Force	Work Migration in A Processor
MP12375	MP12375C1	US	14/230,698	3/31/2014	9614762	4/4/2017	In Force	Work Migration in A Processor
MP12376	MP12376	US	13/565,422	8/2/2012	8472452	6/25/2013	In Force	Lookup Cluster Complex
MP12376	MP12376C1	US	13/901,220	5/23/2013	8995449	3/31/2015	In Force	Lookup Cluster Complex
MP12376	MP12376C1C1	US	14/660,132	3/17/2015	9225643	12/29/2015	In Force	Lookup Cluster Complex
MP12376	MP12376I1	US	13/843,353	3/15/2013	8923306	12/30/2014	In Force	Phased Bucket Pre-Fetch In A Network Processor
MP12376	MP12376I1C1	US	14/583,968	12/29/2014	9531723	12/27/2016	In Force	Phased Bucket Pre-Fetch In A Network Processor
MP12376	MP12376WO	WO	PCT/US2012/04938	8/2/2012	DNA		Pending	Lookup Cluster Complex
MP12376	MP12376WOKR	KR	1020147005633	8/2/2012		12/17/2014	In Force	Lookup Cluster Complex
MP12377	MP12377	US	13/220,249	8/29/2011	8798047	8/5/2014	In Force	METHODS AND SYSTEMS FOR PROCESSING NETWORK INFORMATION
MP12378	MP12378	US	13/238,485	9/21/2011	8572328	10/29/2013	In Force	METHOD AND SYSTEM FOR MEMORY MANAGEMENT
MP12378	MP12378C1	US	14/036,920	9/25/2013	8918593	12/23/2014	In Force	METHOD AND SYSTEM FOR MEMORY MANAGEMENT
MP12379	MP12379	US	13/433,146	3/28/2012	8953606	2/10/2015	In Force	FLEXIBLE EDGE ACCESS SWITCH AND ASSOCIATED METHODS THEREOF
MP12380	MP12380	US	13/397,002	2/15/2012	8873236	10/28/2014	In Force	ELECTRONIC DEVICES HAVING COOLING MODULE WITH DIRECTION-CONFIGURABLE
MP12381	MP12381	US	13/272,975	10/13/2011	9129060	9/8/2015	In Force	QoS Based Dynamic Execution Engine Selection
MP12381	MP12381C1	US	14/828,884	8/18/2015	9495161	11/15/2016	In Force	QoS Based Dynamic Execution Engine Selection
MP12382	MP12382	US	13/272,937	10/13/2011	9128769	9/8/2015	In Force	Processor With Dedicated Virtual Functions And Dynamic Assignment Of Functional
MP12383	MP12383	US	13/274,767	10/17/2011	9465662	10/11/2016	In Force	Processor With Efficient Work Queuing
MP12383	MP12383HK	HK	14109347.5	9/19/2012	1195959	6/15/2018	In Force	Processor With Efficient Work Queuing
MP12383	MP12383WO	WO	PCT/US2012/05605	9/19/2012	DNA		Pending	Processor With Efficient Work Queuing
MP12383	MP12383WOC	CN	2012800564728	9/19/2012	ZL20128005	9/29/2017	In Force	Processor With Efficient Work Queuing
MP12383	MP12383WOKR	KR	1020147013222	9/19/2012		7/17/2019	In Force	Processor With Efficient Work Queuing
MP12384	MP12384	US	13/277,613	10/20/2011	8885480	11/11/2014	In Force	Packet Priority In A Network Processor
MP12385	MP12385	US	13/281,059	10/25/2011	9065626	6/23/2015	In Force	Bit Error Rate Impact Reduction
MP12387	MP12387	US	13/280,756	10/25/2011	8850125	9/30/2014	In Force	System And Method To Provide Non-Coherent Access To A Coherent Memory Syste
MP12387	MP12387C1	US	14/466,384	8/22/2014	9569366	2/14/2017	In Force	System And Method To Provide Non-Coherent Access To A Coherent Memory Syste
MP12388	MP12388	US	13/280,738	10/25/2011	8560757	10/15/2013	In Force	System And Method To Reduce Memory Access Latencies Using Selective Replication
MP12388	MP12388C1	US	14/023,953	9/11/2013	8850101	9/30/2014	In Force	System And Method To Reduce Memory Access Latencies Using Selective Replication

PATENT
REEL: 057897 FRAME: 0521

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12388	MP12388HK	HK	14109348.4	9/16/2014	1195960	4/28/2017	In Force	System And Method To Reduce Memory Access Latencies Using Selective Replication
MP12388	MP12388WO	WO	PCT/US2012/05726	9/26/2012	DNA		Pending	System And Method To Reduce Memory Access Latencies Using Selective Replication
MP12388	MP12388WOC	CN	201280057867X	9/26/2012	ZL20128005	6/29/2016	In Force	System And Method To Reduce Memory Access Latencies Using Selective Replication
MP12388	MP12388WOKR	KR	1020147013564	5/20/2014		4/24/2019	In Force	System And Method To Reduce Memory Access Latencies Using Selective Replication
MP12389	MP12389	US	13/281,052	10/25/2011	8855248	10/7/2014	In Force	Word Boundary Lock
MP12389	MP12389C1	US	14/492,557	9/22/2014	9059836	6/16/2015	In Force	Word Boundary Lock
MP12390	MP12390	US	13/280,841	10/25/2011	9219560	12/22/2015	In Force	Multi-Protocol Serdes Phy Apparatus
MP12390	MP12390HK	HK	14107924.0	9/26/2012	1194544	12/8/2017	In Force	Multi-Protocol Serdes Phy Apparatus
MP12390	MP12390WO	WO	PCT/US2012/05727	9/26/2012	DNA		Pending	Multi-Protocol Serdes Phy Apparatus
MP12390	MP12390WOC	CN	201280052392.5	9/26/2012	ZL20128005	11/9/2016	In Force	Multi-protocol serdes phy apparatus
MP12390	MP12390WOD	DE	112012004 451.7	9/26/2012			Pending	Multi-Protocol Serdes Phy Apparatus
MP12390	MP12390WOKR	KR	1020147014165	9/26/2012		8/4/2016	In Force	MULTI-PROTOCOL SEREDS PHY APPARATUS
MP12391	MP12391	US	13/280,768	10/25/2011	8473658	6/25/2013	In Force	Input Output Bridging
MP12391	MP12391C1	US	13/905,750	5/30/2013	8595401	11/26/2013	In Force	Input Output Bridging
MP12392	MP12392	US	13/328,919	12/16/2011	9094333	7/28/2015	In Force	SYSTEMS AND METHODS FOR SENDING AND RECEIVING INFORMATION VIA A NETW
MP12392	MP12392C1	US	14/747,790	6/23/2015	9401879	7/26/2016	In Force	SYSTEMS AND METHODS FOR SENDING AND RECEIVING INFORMATION VIA A NETW
MP12393	MP12393	US	13/283,252	10/27/2011	9906468	2/27/2018	In Force	Packet Traffic Control In A Network Processor
MP12394	MP12394	US	13/284,289	10/28/2011	9612934	4/4/2017	In Force	Network Processor With Distributed Trace Buffers
MP12395	MP12395	US	13/285,773	10/31/2011	9059945	6/16/2015	In Force	Work Request Processor
MP12395	MP12395C1	US	14/670,934	3/27/2015	9529640	12/27/2016	In Force	Work Request Processor
MP12396	MP12396	US	13/403,697	2/23/2012	8893366	11/25/2014	In Force	TOOLS, SYSTEMS, AND METHODS FOR REMOVING CONNECTORS FROM PORTS IN A
MP12397	MP12397	US	13/285,629	10/31/2011	9330002	5/3/2016	In Force	Multi-Core Interconnect In A Network Processor
MP12397	MP12397HK	HK	14109343.9	10/29/2012			Pending	Multi-Core Interconnect In A Network Processor
MP12397	MP12397WO	WO	PCT/US2012/06237	10/29/2012	DNA		Pending	Multi-Core Interconnect In A Network Processor
MP12397	MP12397WOC	CN	2012800592395	10/29/2012	ZL20128005	6/21/2019	In Force	Multi-Core Interconnect In A Network Processor
MP12397	MP12397WOD	DE	112012004551.3	10/29/2012			Pending	Multi-Core Interconnect In A Network Processor
MP12397	MP12397WOJP	JP	2014-539104	10/29/2012			Pending	Multi-Core Interconnect In A Network Processor
MP12397	MP12397WOJP	JP	2017-213851	11/6/2017			Pending	MULTI-CORE INTERCONNECT IN NETWORK PROCESSOR
MP12397	MP12397WOKR	KR	1020147012490	10/29/2012			Pending	Multi-Core Interconnect In A Network Processor
MP12398	MP12398	US	13/303,885	11/23/2011	9203805	12/1/2015	In Force	Reverse NFA Generation And Processing
MP12398	MP12398C1	US	14/863,484	9/24/2015	9762544	9/12/2017	In Force	Reverse NFA Generation And Processing
MP12401	MP12401WO	WO	PCT/US2013/03309	3/20/2013	DNA		Pending	Hardware And Software Association And Authentication
MP12402	MP12402	US	13/447,521	4/16/2012	9164913	10/20/2015	In Force	METHOD AND SYSTEM FOR OFFLOADING COPY ON WRITE OPERATIONS
MP12403	MP12403	US	13/481,122	5/25/2012	8989220	3/24/2015	In Force	High Speed Variable Bandwidth Ring-Based System

PATENT
REEL: 057897 FRAME: 0522

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12404	MP12404-1	US	13/790,395	3/8/2013	9350807	5/24/2016	In Force	INTELLIGENT ADAPTER FOR PROVIDING STORAGE AREA NETWORK ACCESS AND ACC
MP12404	MP12404-2	US	13/790,471	3/8/2013	9330003	5/3/2016	In Force	INTELLIGENT ADAPTER FOR MAINTAINING CACHE COHERENCY
MP12404	MP12404-3	US	13/790,499	3/8/2013	9507524	11/29/2016	In Force	IN-BAND MANAGEMENT USING AN INTELLIGENT ADAPTER AND METHODS THEREOF
MP12404	MP12404-5	US	13/902,427	5/24/2013	9172586	10/27/2015	In Force	METHOD AND SYSTEM FOR WRITING TAG AND DATA
MP12404	MP12404-6	US	13/790,846	3/8/2013	9232005	1/5/2016	In Force	METHODS AND SYSTEMS FOR AN INTELLIGENT STORAGE ADAPTER USED FOR BOTH
MP12405	MP12405	US	13/594,343	8/24/2012	9229791	1/5/2016	In Force	SYSTEM AND METHOD FOR HIGH SPEED MULTIPLE BUFFER ALLOCATION
MP12406	MP12406	US	13/644,535	10/4/2012	9256562	2/9/2016	In Force	METHOD AND SYSTEM FOR COMMUNICATION BETWEEN A COMPUTING SYSTEM AN
MP12407	MP12407	US	13/649,391	10/11/2012	9727494	8/8/2017	In Force	METHOD AND SYSTEM FOR COMMUNICATION BETWEEN A COMPUTING DEVICE AN
MP12409	MP12409	US	13/654,308	10/17/2012	9069919	6/30/2015	In Force	METHOD AND SYSTEM FOR ARBITRATION VERIFICATION
MP12410	MP12410	US	14/062,418	10/24/2013	9424226	8/23/2016	In Force	METHOD AND SYSTEM FOR SIGNAL EQUALIZATION IN COMMUNICATION BETWEEN
MP12411	MP12411	US	13/660,928	10/25/2012	8677044	3/18/2014	In Force	METHOD AND SYSTEM FOR COMMUNICATION USING MULTIPLE DMA CHANNELS
MP12412	MP12412	US	14/058,887	10/21/2013	9311268	4/12/2016	In Force	METHOD AND SYSTEM FOR COMMUNICATION WITH PERIPHERAL DEVICES
MP12413	MP12413	US	13/924,107	6/21/2013	9338059	5/10/2016	In Force	SYSTEM AND METHODS FOR MANAGING NETWORKS
MP12414	MP12414	US	13/852,885	3/28/2013	9100334	8/4/2015	In Force	METHOD AND SYSTEM FOR VARIABLE LENGTH TAG PROCESSING
MP12415	MP12415	US	13/852,872	3/28/2013	9143415	9/22/2015	In Force	METHOD AND SYSTEM FOR DETECTING LOSS OF SYNCHRONIZATION IN PORTS
MP12416	MP12416	US	13/678,108	11/15/2012	8995455	3/31/2015	In Force	MEMORY DEVICES FOR NETWORK DEVICES AND ASSOCIATED METHODS
MP12417	MP12417	US	13/678,121	11/15/2012	9225808	12/29/2015	In Force	SYSTEMS AND METHODS FOR PROCESSING INFORMATION BY A NETWORK DEVICE
MP12418	MP12418	US	13/678,398	11/15/2012	9046941	6/2/2015	In Force	SYSTEM AND METHOD FOR SHARING LOGIC IN A NETWORK DEVICE
MP12419	MP12419	US	13/678,047	11/15/2012	8995425	3/31/2015	In Force	NETWORK DEVICE SCHEDULER AND METHODS THEREOF
MP12419	MP12419D1	US	14/658,544	3/16/2015	9590924	3/7/2017	In Force	NETWORK DEVICE SCHEDULER AND METHODS THEREOF
MP12420	MP12420	US	13/678,055	11/15/2012	8989191	3/24/2015	In Force	SYSTEMS AND METHODS FOR HARD ZONING IN NETWORKS
MP12421	MP12421	US	13/678,086	11/15/2012	9444713	9/13/2016	In Force	CUT-THROUGH ROUTING FOR NETWORK DEVICES
MP12422	MP12422	US	13/678,161	11/15/2012	8995457	3/31/2015	In Force	SYSTEMS AND METHODS FOR MODIFYING FRAMES IN A NETWORK DEVICE
MP12423	MP12423	US	13/678,135	11/15/2012	9172655	10/27/2015	In Force	SYSTEMS AND METHODS FOR QUALITY OF SERVICE IN NETWORKS
MP12424	MP12424	US	13/678,378	11/15/2012	9426063	8/23/2016	In Force	SYSTEMS AND METHODS FOR ROUTING BY NETWORK DEVICES
MP12425	MP12425	US	13/678,385	11/15/2012	9225672	12/29/2015	In Force	SYSTEMS AND METHODS FOR PACKET GROUPING IN NETWORKS
MP12426	MP12426	US	13/678,377	11/15/2012	8996798	3/31/2015	In Force	SYSTEMS AND METHODS FOR USING TCAMS IN NETWORK DEVICES
MP12427	MP12427	US	13/678,100	11/15/2012	8924764	12/30/2014	In Force	SYSTEMS AND METHODS FOR RATE MATCHING IN NETWORKS UTILIZING A STROBE C
MP12428	MP12428	US	13/678,367	11/15/2012	9071559	6/30/2015	In Force	NETWORK DEVICES HAVING CONFIGURABLE RECEIVE PACKET QUEUES AND RELATED
MP12428	MP12428D1	US	14/749,964	6/25/2015	9282000	3/8/2016	In Force	NETWORK DEVICES HAVING CONFIGURABLE RECEIVE PACKET QUEUES AND RELATED
MP12431	MP12431	US	13/678,145	11/15/2012	8976667	3/10/2015	In Force	METHOD AND SYSTEM FOR PROGRAMMABLE DELAY BEFORE TRANSMISSION PAUSI
MP12432	MP12432	US	13/830,717	3/14/2013	9282046	3/8/2016	In Force	SMOOTHING FIFO AND METHODS THEREOF
MP12433	MP12433	US	13/678,418	11/15/2012	9172602	10/27/2015	In Force	METHOD AND SYSTEM FOR AUTO-NEGOTIATION
MP12434	MP12434	US	13/678,397	11/15/2012	9049113	6/2/2015	In Force	SYSTEMS AND METHODS FOR PRIMITIVE SEQUENCE CAPTURE AND RETRANSMISSIO

PATENT
REEL: 057897 FRAME: 0523

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12435	MP12435	US	13/678,406	11/15/2012	9172661	10/27/2015	In Force	METHOD AND SYSTEM FOR USING LANE ALIGNMENT MARKERS
MP12436	MP12436	US	13/762,715	2/8/2013	9384113	7/5/2016	In Force	SYSTEMS AND METHODS FOR IDENTIFYING PORT PROTOCOLS USING LEDS
MP12438	MP12438	US	13/689,607	11/29/2012	9047151	6/2/2015	In Force	METHODS AND SYSTEMS FOR PROCESSING COMMANDS BY A DEVICE INTERFACING
MP12439	MP12439	US	13/782,673	3/1/2013	9164947	10/20/2015	In Force	METHOD AND SYSTEM FOR INSERTING COOKIES IN I/O COMMANDS
MP12441	MP12441	US	13/834,838	3/15/2013	8953608	2/10/2015	In Force	METHOD AND SYSTEM FOR FRAME AGGREGATION
MP12442	MP12442	US	14/100,856	12/9/2013	9047208	6/2/2015	In Force	METHOD AND SYSTEM OF CONFIGURING VIRTUAL FUNCTION IN PERIPHERAL DEVICE
MP12444	MP12444	US	13/755,770	1/31/2013	8948203	2/3/2015	In Force	METHOD AND SYSTEM FOR USING ASYMETRIC TRANSFER RATES IN RECEIVE AND TR
MP12446	MP12446	US	14/194,567	2/28/2014	9331942	5/3/2016	In Force	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST
MP12446	MP12446C1	US	15/140,424	4/27/2016	9729447	8/8/2017	In Force	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST
MP12446	MP12446CN	CN	201410090589.9	3/12/2014	6373021	12/7/2018	In Force	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST P
MP12446	MP12446HK	HK	15102553.8	3/12/2014	6190754		Pending	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST P
MP12446	MP12446JP	JP	2014-47788	3/11/2014	JP6373021	8/15/2018	In Force	Apparatus and method for processing longest prefix match table configured different
MP12446	MP12446KR	KR	10-2014-0028584	3/11/2014			Pending	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST P
MP12446	MP12446TW	TW	103108614	3/12/2014		12/21/2018	In Force	APPARATUS AND METHOD FOR PROCESSING ALTERNATELY CONFIGURED LONGEST P
MP12447	MP12447	US	14/142,612	12/27/2013	9256380	2/9/2016	In Force	APPARATUS AND METHOD FOR PACKET MEMORY DATAPATH PROCESSING IN HIGH
MP12448	MP12448	US	13/830,492	3/14/2013	9706564	7/11/2017	In Force	Apparatus and Method for Media Access Control Scheduling with a Priority Calculatio
MP12449	MP12449	US	13/831,415	3/14/2013	10083200	9/25/2018	In Force	Batch Incremental Update
MP1244W	MP1244WO	WO	PCT/US2007/01814	8/14/2007	DNA		Pending	A Multi-Thread Processor with Multiple Program Counters
MP12450	MP12450	US	13/830,395	3/14/2013	9237581	1/12/2016	In Force	APPARATUS AND METHOD FOR MEDIA ACCESS CONTROL SCHEDULING WITH A SORT
MP12450	MP12450CN	CN	201410145120.0	3/11/2014	ZL20141014	6/11/2019	In Force	APPARATUS AND METHOD FOR MEDIA ACCESS CONTROL SCHEDULING WITH A SORT
MP12450	MP12450KR	KR	10-2014-0030242	3/14/2014			Pending	APPARATUS AND METHOD FOR MEDIA ACCESS CONTROL SCHEDULING WITH A SORT
MP12451	MP12451-2	US	14/207,928	3/13/2014	9430511	8/30/2016	In Force	Merging Independent Writes, Separating Dependent And Independent Writes, And E
MP12451	MP12451-3	US	14/207,933	3/13/2014	10229144	3/12/2019	In Force	NSP Manager
MP12452	MP12452	US	13/841,743	3/15/2013	9531647	12/27/2016	In Force	Multi-Host Processing
MP12453	MP12453	US	13/896,798	5/17/2013	9595003	3/14/2017	In Force	Compiler With Mask Nodes
MP12455	MP12455	US	13/844,451	3/15/2013	9112767	8/18/2015	In Force	Method And An Accumulator Scoreboard For Out-Of-Order Rule Response Handling
MP12456	MP12456	US	13/840,867	3/15/2013	9195939	11/24/2015	In Force	Scope In Decision Trees
MP12456	MP12456C1	US	14/922,449	10/26/2015	10460250	10/29/2019	In force	Scope In Decision Trees
MP12457	MP12457	US	13/843,992	3/15/2013	9130819	9/8/2015	In Force	Method And Apparatus For Scheduling Rule Matching In A Processor
MP12457	MP12457CN	CN	201410097575X	3/14/2014	ZL20141009	4/12/2017	In Force	Scheduling Method And Apparatus For Scheduling Rule Matching In A Processor
MP12457	MP12457HK	HK	14110989.6	3/14/2014	1197478	3/9/2018	In Force	Scheduling Method And Apparatus For Scheduling Rule Matching In A Processor
MP12458	MP12458	US	13/843,308	3/15/2013	9276846	3/1/2016	In Force	Packet Extraction Optimization in A Network Processor
MP12459	MP12459	US	13/843,782	3/15/2013	9152494	10/6/2015	In Force	Method And Apparatus For Data Packet Integrity Checking In A Processor
MP12460	MP12460	US	14/201,692	3/7/2014	9264357	2/16/2016	In Force	APPARATUS AND METHOD FOR TABLE SEARCH WITH CENTRALIZED MEMORY POOL I

PATENT
REEL: 057897 FRAME: 0524

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12460	MP12460CN	CN	201410182691.1	4/30/2014	ZL20141018	4/10/2018	In Force	APPARATUS AND METHOD FOR TABLE SEARCH WITH CENTRALIZED MEMORY POOL I
MP12460	MP12460HK	HK	15104281.3	5/5/2015	1204166	7/12/2019	In Force	APPARATUS AND METHOD FOR TABLE SEARCH WITH CENTRALIZED MEMORY POOL I
MP12460	MP12460JP	JP	2014-92766	4/28/2014	JP6190754	8/30/2017	In Force	Apparatus and method for searching a table using a centralized memory pool in a net
MP12460	MP12460TW	TW	103115489	4/30/2014			Pending	APPARATUS AND METHOD FOR TABLE SEARCH WITH CENTRALIZED MEMORY POOL I
MP12462	MP12462	US	13/902,453	5/24/2013	9747227	8/29/2017	In Force	METHOD AND SYSTEM FOR TRANSMITTING INFORMATION FROM A NETWORK DEVI
MP12463	MP12463	US	13/906,207	5/30/2013	10019203	7/10/2018	In Force	METHOD AND SYSTEM FOR PROCESSING WRITE REQUESTS
MP12464	MP12464	US	13/921,090	6/18/2013			Pending	Apparatus and Method for Uniquely Enumerating Paths in a Parse Tree
MP12464	MP12464CN	CN	201410270176.9	6/17/2014	ZL20141027	5/5/2019	In Force	APPARATUS AND METHOD FOR UNIQUELY ENUMERATING PATHS IN A PARSE TREE
MP12464	MP12464JP	JP	2014-119339	6/10/2014	JP6383578	8/29/2018	In Force	APPARATUS AND METHOD FOR UNIQUELY ENUMERATING PATHS IN A PARSE TREE
MP12464	MP12464KR	KR	10-2014-0074391	6/18/2014			Pending	APPARATUS AND METHOD FOR UNIQUELY ENUMERATING PATHS IN A PARSE TREE
MP12464	MP12464TW	TW	103120983	6/18/2014			Pending	APPARATUS AND METHOD FOR UNIQUELY ENUMERATING PATHS IN A PARSE TREE
MP12465	MP12465	US	13/922,911	6/20/2013	8898346	11/25/2014	In Force	METHOD AND SYSTEM FOR CONFIGURING NETWORK DEVICES
MP12467	MP12467	US	13/949,095	7/23/2013	9411400	8/9/2016	In Force	METHODS AND SYSTEMS FOR ADVERTSING AVAILABLE CREDIT AT MEMORY OF NET
MP12468	MP12468CN	CN	201410452112.0	7/24/2014			Pending	NETWORK INTERFACE CARD WITH VIRTUAL SWITCH AND TRAFFIC FLOW POLICY ENF
MP12468	MP12468EP	EP	14177898.5	7/21/2014			Pending	NETWORK INTERFACE CARD WITH VIRTUAL SWITCH AND TRAFFIC FLOW POLICY ENF
MP12468	MP12468HK	HK	15107379.9	7/24/2014			Pending	NETWORK INTERFACE CARD WITH VIRTUAL SWITHCH AND TRAFFIC FLOW POLICY EN
MP12468	MP12468JP	JP	2014-151627	7/25/2014			Pending	NETWORK INTERFACE CARD WITH VIRTUAL SWITCH AND TRAFFIC FLOW POLICY ENF
MP12468	MP12468KR	KR	10-2014-0092692	7/22/2014			Pending	NETWORK INTERFACE CARD WITH VIRTUAL SWITCH AND TRAFFIC FLOW POLICY ENF
MP12469	MP12469	US	13/954,661	7/30/2013	8977786	3/10/2015	In Force	METHOD AND SYSTEM FOR PROCESSING INFORMATION AT PERIPHERAL DEVICES
MP12472	MP12472	US	14/200,939	3/7/2014	9264023	2/16/2016	In Force	Scannable Flop With A Single Storage Element
MP12473	MP12473	US	14/217,935	3/18/2014	9130549	9/8/2015	In Force	Multiplexer Flop
MP12474	MP12474	US	14/015,929	8/30/2013	9426166	8/23/2016	In Force	Method And Apparatus For Processing Finite Automata
MP12474	MP12474CN	CN	2014104321980	8/28/2014	ZL20141043	12/14/2018	In Force	Method And Apparatus For Processing Finite Automata
MP12474	MP12474HK	HK	15108607.1	8/28/2014			Pending	Method And Apparatus For Processing Finite Automata
MP12475	MP12475	US	14/014,803	8/30/2013	9154455	10/6/2015	In Force	METHOD AND SYSTEM FOR DETERMINING DROP ELIGIBILITY OF NETWORK INFORM
MP12476	MP12476	US	14/015,601	8/30/2013	8963601	2/24/2015	In Force	Clock Gated Delay Line Based On Setting Value
MP12477	MP12477	US	14/186,978	2/21/2014	9563399	2/7/2017	In Force	Generating A Non-Deterministic Finite Automata (NFA) Graph For Regular Expression
MP12477	MP12477CN	CN	2014104315551	8/28/2014	ZL20141043	1/4/2019	In Force	Generating a non-deterministic finite automata (NFA) graph for regular expression pa
MP12477	MP12477HK	HK	15108608.0	8/28/2014			Pending	Generating A Non-Deterministic Finite Automata (NFA) Graph For Regular Expression
MP12477	MP12477KR	KR	1020140114469	8/29/2014		4/21/2016	In Force	GENERATING A NFA (Non-Deterministic finite automata) GRAPH FOR REGULAR EXPR
MP12478	MP12478	US	14/186,913	2/21/2014	9507563	11/29/2016	In Force	System And Method To Traverse A Non-Deterministic Finite Automata (NFA) Graph G
MP12478	MP12478CN	CN	2014104332025	8/28/2014	ZL20141043	4/23/2019	In Force	System and method to traverse a non-deterministic finite automata (NFA) graph gen
MP12478	MP12478HK	HK	15112237.1	8/28/2014			Pending	SYSTEM AND METHOD TO TRAVERSE A NON-DETERMINISTIC FINITE AUTOMATA (NF
MP12479	MP12479	US	14/015,248	8/30/2013	9426165	8/23/2016	In Force	Method And Apparatus For Compilation Of Finite Automata

PATENT
REEL: 057897 FRAME: 0525

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12479	MP12479CN	CN	2014104333210	8/28/2014	ZL20141043	3/23/2018	In Force	Method And Apparatus For Compilation Of Finite Automata
MP12479	MP12479HK	HK	15108609.9	8/28/2014		7/5/2019	In Force	Method And Apparatus For Compilation Of Finite Automata
MP12480	MP12480	US	14/015,607	8/30/2013	9335784	5/10/2016	In Force	Clock Distribution Circuit With Distributed Delay Locked Loop
MP12480	MP12480CN	CN	201410438613.3	8/29/2014	ZL20141043	1/23/2018	In Force	Distributed Delay Locked Loop
MP12480	MP12480HK	HK	15107380.6	8/29/2014			Pending	Distributed Delay Locked Loop
MP12481	MP12481	US	14/142,623	12/27/2013	9509585	11/29/2016	In Force	APPARATUS AND METHOD FOR TIME STAMPING PACKETS ACROSS SEVERAL NODES
MP12482	MP12482	US	14/142,631	12/27/2013	9438539	9/6/2016	In Force	APPARATUS AND METHOD FOR OPTIMIZING THE NUMBER OF ACCESSES TO PAGE-R
MP12483	MP12483	US	14/142,643	12/27/2013	9009364	4/14/2015	In Force	APPARATUS AND METHOD FOR ACCELERATED PAGE LINK LIST PROCESSING IN A PA
MP12483	MP12483C1	US	14/676,791	4/1/2015	9262369	2/16/2016	In Force	APPARATUS AND METHOD FOR ACCELERATED PAGE LINK LIST PROCESSING IN A PA
MP12484	MP12484	US	14/142,653	12/27/2013	9736069	8/15/2017	In Force	Method for Storing and Retrieving Packets in High Bandwidth and Low Latency Packe
MP12485	MP12485	US	14/034,200	9/23/2013	9281953	3/8/2016	In Force	SYSTEMS AND METHODS FOR ROUTING MULTICAST PACKETS
MP12486	MP12486	US	14/034,006	9/23/2013	9256491	2/9/2016	In Force	METHOD AND SYSTEM FOR DATA INTEGRITY
MP12487	MP12487	US	14/036,709	9/25/2013	9568542	2/14/2017	In Force	Memory Interface With Integrated Tester
MP12488	MP12488TW	TW	103132756	9/23/2014			Pending	SEMICONDUCTOR WITH VIRTUALIZED COMPUTATION AND SWITCH RESOURCES
MP12488	MP12488WO	WO	PCT/US2014/05614	9/17/2014	DNA		Pending	SEMICONDUCTOR WITH VIRTUALIZED COMPUTATION AND SWITCH RESOURCES
MP12489	MP12489	US	14/038,156	9/26/2013	9639476	5/2/2017	In Force	Merged TLB Structure For Multiple Sequential Address Translations
MP12489	MP12489CN	CN	2014104984014	9/25/2014	ZL20141049	2/6/2018	In Force	Merged TLB Structure For Multiple Sequential Address Translations
MP12489	MP12489HK	HK	15107954.2	8/18/2015			Pending	Merged TLB Structure For Multiple Sequential Address Translations
MP12489	MP12489KR	KR	1020140129272	9/26/2014		1/14/2016	In Force	Merged TLB Structure For Multiple Sequential Address Translations
MP12490	MP12490	US	14/038,383	9/26/2013	9208103	12/8/2015	In Force	Translation Bypass In Multi-Stage Address Translation
MP12490	MP12490CN	CN	201410498013.6	9/25/2014	ZL20141049	6/8/2018	In Force	Translation Bypass In Multi-Stage Address Translation
MP12490	MP12490HK	HK	15109895.0	9/25/2014		8/2/2019	In Force	Translation Bypass In Multi-Stage Address Translation
MP12490	MP12490KR	KR	10-2014-0129264	9/26/2014		2/23/2016	In Force	Translation Bypass In Multi-Stage Address Translation
MP12491	MP12491	US	14/038,189	9/26/2013	9645941	5/9/2017	In Force	Collapsed Address Translation With Multiple Page Sizes
MP12491	MP12491C1	US	15/475,718	3/31/2017	10042778	8/7/2018	In Force	Collapsed Address Translation With Multiple Page Sizes
MP12491	MP12491DE	DE	102014014 076.8	9/25/2014			Pending	Collapsed Address Translation With Multiple Page Sizes
MP12492	MP12492	US	14/038,225	9/26/2013	9268694	2/23/2016	In Force	Maintenance Of Cache And Tags In A Translation Lookaside Buffer
MP12494	MP12494	US	14/040,431	9/27/2013	9507369	11/29/2016	In Force	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
MP12494	MP12494CN	CN	201410503442.8	9/26/2014			Pending	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
MP12494	MP12494CND1	CN	201810444294.5	9/26/2014			Pending	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
MP12494	MP12494DE	DE	102014014 494.1	9/25/2014			Pending	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
MP12494	MP12494HK	HK	15107953.3	9/26/2014			Pending	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
MP12494	MP12494JP	JP	2014-192983	9/22/2014	JP6002728	9/9/2016	In Force	DYNAMIC ADJUSTMENT OF SUPPLY VOLTAGE BASED ON MONITORED CHIP TEMPER
MP12495	MP12495	US	14/040,577	9/27/2013	9413568	8/9/2016	In Force	Method And Apparatus For Calibrating An Input Interface

PATENT
REEL: 057897 FRAME: 0526

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12496	MP12496	US	14/040,563	9/27/2013	9087567	7/21/2015	In Force	Method And Apparatus For Amplifier Offset Calibration
MP12497	MP12497	US	14/040,532	9/27/2013	9496012	11/15/2016	In Force	Method and Apparatus For Reference Voltage Calibration In A Single-Ended Receiver
MP12498	MP12498	US	14/039,846	9/27/2013	9490033	11/8/2016	In Force	Auto-Blow Memory Repair
MP12499	MP12499	US	14/041,961	9/30/2013	9041432	5/26/2015	In Force	Clock Multiplexing And Repeater Network
MP12500	MP12500	US	14/042,111	9/30/2013	9264383	2/16/2016	In Force	SYSTEMS AND METHODS FOR QUALITY OF SERVICE FOR LINK AGGREGATION GROUP
MP12501	MP12501	US	14/042,403	9/30/2013	10110393	10/23/2018	In Force	Protocol Switching over Multi-Network Interface
MP12502	MP12502	US	14/045,674	10/3/2013	9390023	7/12/2016	In Force	Method And Apparatus For Conditional Storing Of Data Using A Compare-And-Swap
MP12502	MP12502KR	KR	10-2014-0134480	10/6/2014	101587362	1/14/2016	In Force	Method And Apparatus For Conditional Storing Of Data Using A Compare-And-Swap
MP12503	MP12503	US	14/045,602	10/3/2013	9501243	11/22/2016	In Force	Method And Apparatus For Supporting Wide Operations Using Atomic Sequences
MP12503	MP12503CN	CN	201410521310.8	9/30/2014	ZL20141052	3/23/2018	In Force	Method And Apparatus For Supporting Wide Operations Using Atomic Sequences
MP12503	MP12503HK	HK	15107951.5	9/30/2014	1207437	7/5/2019	In Force	Method And Apparatus For Supporting Wide Operations Using Atomic Sequences
MP12503	MP12503TW	TW	103133879	9/30/2014	I670648	9/1/2019	In Force	Method And Apparatus For Supporting Wide Operations Using Atomic Sequences
MP12504	MP12504	US	14/045,644	10/3/2013	9281034	3/8/2016	In Force	Data Strobe Generation
MP12505	MP12505	US	14/046,879	10/4/2013	9721627	8/1/2017	In Force	Method and Apparatus for Aligning Signals
MP12506	MP12506	US	14/048,849	10/8/2013	9170880	10/27/2015	In Force	METHOD AND SYSTEM FOR DATA INTEGRITY IN TCAMS
MP12507	MP12507	US	14/051,290	10/10/2013	9253120	2/2/2016	In Force	SYSTEMS AND METHODS FOR HIGH SPEED DATA PROCESSING AT A NETWORK PORT
MP12508	MP12508	US	14/067,815	10/30/2013	9465406	10/11/2016	In Force	TIMERS AND METHODS THEREOF FOR COMPUTING DEVICES
MP12509	MP12509	US	14/080,389	11/14/2013	9323715	4/26/2016	In Force	Method And Apparatus To Represent A Processor Context With Fewer Bits
MP12509	MP12509CN	CN	2014106415662	11/13/2014	ZL20141064	5/4/2018	In Force	Method And Apparatus To Represent A Processor Context With Fewer Bits
MP12509	MP12509HK	HK	15107950.6	11/13/2014	1207436	7/12/2019	In Force	Method And Apparatus To Represent A Processor Context With Fewer Bits
MP12509	MP12509KR	KR	1020140157977	11/13/2014	101694591(	1/3/2017	In Force	Method And Apparatus To Represent A Processor Context With Fewer Bits
MP12509	MP12509TW	TW	103138879	11/10/2014	I541661	7/11/2016	In Force	Method And Apparatus To Represent A Processor Context With Fewer Bits
MP12510	MP12510	US	14/083,894	11/19/2013	9363193	6/7/2016	In Force	VIRTUALIZED NETWORK INTERFACE FOR TCP REASSEMBLY BUFFER ALLOCATION
MP12510	MP12510DE	DE	102014012618.8	8/22/2014			Pending	Virtualized network interface for TCP recomposition buffer allocation
MP12511	MP12511	US	14/088,082	11/22/2013	9223518	12/29/2015	In Force	METHOD AND SYSTEM FOR REMOTE CACHE DIRECT DATA PLACEMENT
MP12512	MP12512	US	14/151,748	1/9/2014	9058463	6/16/2015	In Force	SYSTEMS AND METHODS FOR SPECIFYING, MODELING, IMPLEMENTING AND VERIFYI
MP12512	MP12512TW	TW	103141564	12/1/2014	I634445	9/1/2018	In Force	Systems and methods for specifying, modeling, implementing and verifying IC design
MP12513	MP12513	US	14/106,841	12/15/2013	9313029	4/12/2016	In Force	VIRTUALIZED NETWORK INTERFACE FOR REMOTE DIRECT MEMORY ACCESS OVER C
MP12514	MP12514	US	14/106,827	12/15/2013			Pending	VIRTUALIZED NETWORK INTERFACE FOR LOCKDOWN AND OVERLAY OF DATA IN TRA
MP12515	MP12515	US	14/140,503	12/25/2013	9379992	6/28/2016	In Force	METHOD AND AN APPARATUS FOR VIRTUALIZATION OF A QUALITY-OF-SERVICE
MP12515	MP12515CN	CN	2014107420206	12/5/2014	ZL20141074	7/28/2017	In Force	Method and an apparatus for virtualization of quality-of-service
MP12515	MP12515HK	HK	15108376	12/5/2014	1207719B	4/20/2018	In Force	A METHOD AND AN APPARATUS FOR VIRTUALIZATION OF A QUALITY-OF-SERVICE
MP12515	MP12515KR	KR	1020140164241	11/24/2014	101698648(	1/16/2017	In Force	A METHOD AND AN APPARATUS FOR VIRTUALIZATION OF QUALITY-OF-SERVICE
MP12515	MP12515TW	TW	103137163	10/28/2014	I571076	2/11/2017	In Force	A METHOD AND AN APPARATUS FOR VIRTUALIZATION OF A QUALITY-OF-SERVICE

PATENT
REEL: 057897 FRAME: 0527

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12516	MP12516	US	14/140,488	12/25/2013	9306916	4/5/2016	In Force	SYSTEM AND A METHOD FOR A REMOTE DIRECT MEMORY ACCESS OVER CONVERGE
MP12517	MP12517	US	14/140,494	12/25/2013	9977737	5/22/2018	In Force	METHOD AND AN APPARATUS FOR MEMORY ADDRESS ALLIGNMENT
MP12517	MP12517CN	CN	201410756095X	12/10/2014	ZL20141075	8/2/2019	In Force	Method and apparatus for memory address allignment
MP12517	MP12517HK	HK	15109030.6	12/10/2014			Pending	A METHOD AND AN APPARATUS FOR MEMORY ADDRESS ALLIGNMENT
MP12517	MP12517TW	TW	103137161	10/28/2014	I627529	6/21/2018	In Force	A METHOD AND AN APPARATUS FOR MEMORY ADDRESS ALLIGNMENT
MP12518	MP12518	US	14/140,585	12/26/2013	9665508	5/30/2017	In Force	METHOD AND AN APPARATUS FOR CONVERTING INTERRUPTS INTO SCHEDULED EVE
MP12519	MP12519	US	14/141,076	12/26/2013	9390209	7/12/2016	In Force	SYSTEM FOR AND METHOD OF COMBINING CMOS INVERTERS OF MULTIPLE DRIVE S
MP12520	MP12520	US	14/141,096	12/26/2013	9443053	9/13/2016	In Force	SYSTEM FOR AND METHOD OF PLACING CLOCK STATIONS USING VARIABLE DRIVE-S
MP12521	MP12521	US	14/141,104	12/26/2013	9305129	4/5/2016	In Force	SYSTEM FOR AND METHOD OF TUNING CLOCK NETWORKS CONSTRUCTED USING VA
MP12521	MP12521HK	HK	15107952.4	8/18/2015			Pending	SYSTEM AND METHOD FOR TUNING CLOCK NETWORKS
MP12521	MP12521JP	JP	2014-263371	12/25/2014	JP6544923	6/28/2019	In Force	SYSTEM AND METHOD OF TUNING CLOCK NETWORKS CONSTRUCTED USING VARIAB
MP12521	MP12521KR	KR	1020140191072	12/26/2014			Pending	SYSTEM FOR AND METHOD OF TUNING CLOCK NETWORKS CONSTRUCTED USING VA
MP12521	MP12521TW	TW	103145439	12/25/2014	I661325	6/1/2019	In Force	SYSTEM FOR AND METHOD OF TUNING CLOCK NETWORKS CONSTRUCTED USING VA
MP12522	MP12522	US	14/142,511	12/27/2013	9620213	4/11/2017	In Force	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522CN	CN	201410838433.4	12/29/2014	ZL20141083	8/9/2019	In Force	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522D1	US	15/446,259	3/1/2017	9952799	4/24/2018	In Force	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522D2	US	15/446,297	3/1/2017	9952800	4/24/2018	In Force	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522D2C1	US	15/923,851	3/16/2018			Pending	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522HK	HK	15111512.9	12/29/2014			Pending	A MATRIX OF ON-CHIP ROUTERS INTERCONNECTING A PLURALITY OF PROCESSING E
MP12522	MP12522JP	JP	2014-263373	12/25/2014			Pending	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522KR	KR	1020140191978	12/29/2014			Pending	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12522	MP12522TW	TW	103145450	12/25/2014	I659303	5/11/2019	In Force	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12523	MP12523	US	14/142,497	12/27/2013	9548945	1/17/2017	In Force	MATRIX OF ON-CHIP ROUTERS INTERCONNECTING A PLURALITY OF PROCESSING EN
MP12523	MP12523CN	CN	201410838063.4	12/29/2014	ZL20140838	8/9/2019	In Force	Matrix of on-chip routers interconnecting a plurality of processing engines and a met
MP12523	MP12523HK	HK	15111519.2	12/29/2014			Pending	METHOD AND SYSTEM FOR RECONFIGURABLE PARALLEL LOOKUPS USING MULTIPLE
MP12523	MP12523JP	JP	2014-263372	12/25/2014	JP6556450	7/19/2019	In Force	A MATRIX OF ON-CHIP ROUTERS INTERCONNECTING A PLURALITY OF PROCESSING E
MP12523	MP12523KR	KR	1020140192064	12/29/2014			Pending	A MATRIX OF ON-CHIP ROUTERS INTERCONNECTING A PLURALITY OF PROCESSING E
MP12523	MP12523TW	TW	103145445	12/25/2014	I661702	6/1/2019	In Force	A MATRIX OF ON-CHIP ROUTERS INTERCONNECTING A PLURALITY OF PROCESSING E
MP12524	MP12524	US	14/141,987	12/27/2013	9491099	11/8/2016	In Force	LOOK-ASIDE PROCESSOR UNIT WITH INTERNAL AND EXTERNAL ACCESS FOR MULTIC
MP12524	MP12524CN	CN	2014107568006	12/10/2014	ZL20141075	11/23/2018	In Force	LOOK-ASIDE PROCESSOR UNIT WITH INTERNAL AND EXTERNAL ACCESS FOR MULTIC
MP12524	MP12524HK	HK	15108374.2	12/10/2014			Pending	A LOOK-ASIDE PROCESSOR UNIT WITH INTERNAL AND EXTERNAL ACCESS FOR MULTI
MP12524	MP12524KR	KR	1020140160344	11/17/2014			Pending	A LOOK-ASIDE PROCESSOR UNIT WITH INTERNAL AND EXTERNAL ACCESS FOR MULTI
MP12524	MP12524TW	TW	103137160	10/28/2014	I652623	3/1/2019	In Force	A LOOK-ASIDE PROCESSOR UNIT WITH INTERNAL AND EXTERNAL ACCESS FOR MULTI
MP12525	MP12525	US	14/141,681	12/27/2013	9460033	10/4/2016	In Force	Apparatus and Method for Interrupt Collecting and Reporting Status and Delivery Inf

PATENT
REEL: 057897 FRAME: 0528

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12526	MP12526	US	14/143,586	12/30/2013	9419943	8/16/2016	In Force	Method And Apparatus For Processing Of Finite Automata
MP12526	MP12526CN	CN	201410432859X	8/28/2014	ZL20141043	6/5/2018	In Force	Method And Apparatus For Processing Of Finite Automata
MP12526	MP12526HK	HK	15112773.1	8/28/2014	1212119	8/2/2019	In Force	Method And Apparatus For Processing Of Finite Automata
MP12527	MP12527	US	14/144,260	12/30/2013	9880844	1/30/2018	In Force	METHOD AND APPARATUS FOR PARALLEL AND CONDITIONAL DATA MANIPULATION
MP12527	MP12527CN	CN	2014108431994	12/30/2014	ZL20141084	5/28/2019	In Force	Method and apparatus for parallel and conditional data manipulation in software-def
MP12527	MP12527HK	HK	15109646.2	12/30/2014			Pending	METHOD AND APPARATUS FOR PARALLEL AND CONDITIONAL DATA MANIPULATION
MP12527	MP12527JP	JP	2014-267000	12/29/2014	6537823	6/14/2019	In Force	METHOD AND APPARATUS FOR PARALLEL AND CONDITIONAL DATA MANIPULATION
MP12527	MP12527KR	KR	1020140194027	12/30/2014			Pending	METHOD AND APPARATUS FOR PARALLEL AND CONDITIONAL DATA MANIPULATION
MP12528	MP12528	US	14/144,270	12/30/2013	9379963	6/28/2016	In Force	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528CN	CN	201410843934.1	12/30/2014			Pending	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528D1	US	15/167,704	5/27/2016	10009273	6/26/2018	In Force	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528D1D1	US	15/991,810	5/29/2018			Pending	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528HK	HK	15111520.9	12/30/2014			Pending	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528JP	JP	2014-267001	12/29/2014	6537824	6/14/2019	In Force	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528KR	KR	1020140194209	12/30/2014			Pending	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12528	MP12528TW	TW	103145662	12/26/2014	I661695	6/1/2019	In Force	APPARATUS AND METHOD OF GENERATING LOOKUPS AND MAKING DECISIONS FOR
MP12529	MP12529	US	14/145,374	12/31/2013	9275336	3/1/2016	In Force	METHOD AND SYSTEM FOR SKIPPING OVER GROUP(S) OF RULES BASED ON SKIP GR
MP12530	MP12530	US	14/145,918	12/31/2013	9544402	1/10/2017	In Force	MULTI-RULE APPROACH TO ENCODING A GROUP OF RULES
MP12534	MP12534	US	14/150,622	1/8/2014	10447823	10/15/2019	In Force	PACKET PARSING ENGINE
MP12534	MP12534WO	WO	PCT/US2015/10284	1/6/2015			Pending	PACKET PARSING ENGINE
MP12535	MP12535	US	14/150,650	1/8/2014	9307057	4/5/2016	In Force	METHODS AND SYSTEMS FOR RESOURCE MANAGEMENT IN A SINGLE INSTRUCTION
MP12536	MP12536	US	14/150,550	1/8/2014	9268855	2/23/2016	In Force	PROCESSING REQUEST KEYS BASED ON A KEY SIZE SUPPORTED BY UNDERLYING PRO
MP12537	MP12537	US	14/150,572	1/8/2014	9432284	8/30/2016	In Force	METHOD AND APPARATUS FOR COMPILING SEARCH TREES FOR PROCESSING REQUE
MP12538	MP12538	US	14/150,761	1/8/2014	9667446	5/30/2017	In Force	CONDITION CODE APPROACH FOR COMPARING RULE AND PACKET DATA THAT ARE
MP12539	MP12539TW	TW	104100216	1/6/2015	I593256	7/21/2017	In Force	METHODS AND SYSTEMS FOR FLEXIBLE PACKET CLASSIFICATION
MP12539	MP12539WO	WO	PCT/US2015/01027	1/6/2015			Pending	METHODS AND SYSTEMS FOR FLEXIBLE PACKET CLASSIFICATION
MP12540	MP12540	US	14/150,664	1/8/2014	9513926	12/6/2016	In Force	FLOATING MASK GENERATION FOR NETWORK PACKET FLOW
MP12541	MP12541	US	14/150,635	1/8/2014	10284690	5/7/2019	In Force	METHODS AND SYSTEMS FOR DISTRIBUTION OF PACKETS AMONG PARSING CLUSTER
MP12543	MP12543	US	14/152,817	1/10/2014	9647947	5/9/2017	In Force	BLOCK MASK REGISTER KEY PROCESSING BY COMPILING DATA STRUCTURES TO TRA
MP12544	MP12544	US	14/165,100	1/27/2014	9454305	9/27/2016	In Force	METHOD AND SYSTEM FOR MANAGING STORAGE RESERVATION
MP12545	MP12545	US	14/166,082	1/28/2014	9378036	6/28/2016	In Force	METHOD AND SYSTEM FOR COMMUNICATION IN A VIRTUAL MACHINE ENVIRONME
MP12546	MP12546	US	14/169,830	1/31/2014	9602532	3/21/2017	In Force	Method And Apparatus For Optimizing Finite Automata Processing
MP12546	MP12546KR	KR	10-2014-0113845	8/29/2014	101633649	6/21/2016	In Force	Method And Apparatus For Optimizing Finite Automata Processing
MP12547	MP12547	US	14/169,967	1/31/2014	9904630	2/27/2018	In Force	Finite Automata Processing Based On A Top Of Stack (TOS) Memory

PATENT
REEL: 057897 FRAME: 0529

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12547	MP12547CN	CN	2014104332877	8/28/2014	ZL20141043	9/25/2018	In Force	Finite Automata Processing Based On A Top Of Stack (TOS) Memory
MP12547	MP12547HK	HK	16101361.1	8/28/2014			Pending	Finite Automata Processing Based On A Top Of Stack (TOS) Memory
MP12548	MP12548	US	14/170,955	2/3/2014			Pending	METHOD AND AN APPARATUS FOR WORK PACKET QUEUING, SCHEDULING, AND OR
MP12548	MP12548WO	WO	PCT/US2015/14149	2/2/2015			Pending	METHOD AND AN APPARATUS FOR WORK PACKET QUEUING, SCHEDULING, AND OR
MP12549	MP12549	US	14/171,108	2/3/2014	9838471	12/5/2017	In Force	METHOD AND AN APPARATUS FOR WORK REQUEST ARBITRATION IN A NETWORK P
MP12549	MP12549WO	WO	PCT/US2015/01413	2/2/2015			Pending	METHOD AND AN APPARATUS FOR WORK REQUEST ARBITRATION IN A NETWORK P
MP12550	MP12550	US	14/171,290	2/3/2014	9811467	11/7/2017	In Force	METHOD AND AN APPARATUS FOR PRE-FETCHING AND PROCESSING WORK FOR PR
MP12550	MP12550WO	WO	PCT/US2015/01411	2/2/2015			Pending	A METHOD AND AN APPARATUS FOR PRE-FETCHING AND PROCESSING WORK FOR P
MP12550	MP12550WOC	CN	201580003167.6	2/2/2015			Pending	A method and an apparatus for pre-fetching and processing work for processor core
MP12551	MP12551	US	14/186,743	2/21/2014	9692715	6/27/2017	In Force	Multiple Ethernet Ports and Port Types Using a Shared Data Path
MP12551	MP12551C1	US	15/601,493	5/22/2017	10404623	9/3/2019	In Force	Multiple Ethernet Ports And Port Types Using A Shared Data Path
MP12551	MP12551CN	CN	201510072689.3	2/11/2015	104869176E	4/12/2019	In Force	Multiple Ethernet Ports and Port Types Using a Shared Data Path
MP12551	MP12551HK	HK	15109893.2	2/11/2015			Pending	Multiple Ethernet Ports and Port Types Using a Shared Data Path
MP12551	MP12551KR	KR	10-2015-0023450	2/16/2015	101664658	10/4/2016	In Force	Multiple Ethernet Ports and Port Types Using a Shared Data Path
MP12551	MP12551TW	TW	104103687	2/4/2015	I551101	9/21/2016	In Force	AN INTERFACE UNIT BASED ON MULTIPLE ETHERNET PORTS AND PORT TYPES USING
MP12552	MP12552	US	14/630,554	2/24/2015	9729320	8/8/2017	In Force	APPARATUS AND METHOD FOR SOFTWARE ENABLED ACCESS TO PROTECTED HARD
MP12552	MP12552CN	CN	201510172120.4	2/25/2015			Pending	APPARATUS AND METHOD FOR SOFTWARE ENABLED ACCESS TO PROTECTED HARD
MP12552	MP12552HK	HK	15111508.5	2/25/2015			Pending	APPARATUS AND METHOD FOR SOFTWARE ENABLED ACCESS TO PROTECTED HARD
MP12552	MP12552TW	TW	104105809	2/24/2015	I633458	8/21/2018	In Force	APPARATUS AND METHOD FOR SOFTWARE ENABLED ACCESS TO PROTECTED HARD
MP12553	MP12553	US	14/191,163	2/26/2014	9431105	8/30/2016	In Force	Method And Apparatus For Memory Access Management
MP12554	MP12554	US	14/192,100	2/27/2014	9490968	11/8/2016	In Force	CDR Voter With Improved Frequency Offset Tolerance
MP12555	MP12555	US	14/194,049	2/28/2014	9432288	8/30/2016	In Force	System On Chip Link Layer Protocol
MP12556	MP12556	US	14/193,793	2/28/2014	9471416	10/18/2016	In Force	Partitioned Error Code Computation
MP12557	MP12557	US	14/193,933	2/28/2014	9397938	7/19/2016	In Force	Packet Scheduling In A Network Processor
MP12557	MP12557TW	TW	104105253	2/16/2015	I559706	11/21/2016	In Force	Packet Scheduling In A Network Processor
MP12557	MP12557WO	WO	PCT/US2014/07282	12/30/2014			Pending	Packet Scheduling In A Network Processor
MP12557	MP12557WOC	CN	201480076494.X	12/30/2014	ZL20148007	4/20/2018	In Force	Packet Scheduling In A Network Processor
MP12558	MP12558	US	14/193,895	2/28/2014	9680742	6/13/2017	In Force	Packet Output Processing
MP12558	MP12558TW	TW	104104215	2/9/2015	I566551	1/11/2017	In Force	Packet Output Processing
MP12560	MP12560	US	14/193,899	2/28/2014	9483100	11/1/2016	In Force	Method And Apparatus For Power Gating Hardware Components In A Chip Device
MP12560	MP12560CN	CN	201510064815.0	2/6/2015	ZL20151006	5/4/2018	In Force	Method And Apparatus For Power Gating Hardware Components In A Chip Device
MP12560	MP12560HK	HK	15111507.6	6/2/2015	1210879	7/12/2019	In Force	Method And Apparatus For Power Gating Hardware Components In A Chip Device
MP12560	MP12560TW	TW	104105811	2/24/2015	I618355	3/11/2018	In Force	Method And Apparatus For Power Gating Hardware Components In A Chip Device
MP12561	MP12561	US	14/194,038	2/28/2014	9559982	1/31/2017	In Force	Packet Shaping In A Network Processor

PATENT
REEL: 057897 FRAME: 0530

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12561	MP12561TW	TW	104104959	2/13/2015	I668975	8/11/2019	In Force	Circuit and method for packet shaping in a network processor
MP12561	MP12561WO	WO	PCT/US2014/07283	12/30/2014			Pending	Packet Shaping In A Network Processor
MP12561	MP12561WOC	CN	201480076493.5	12/30/2014	ZL20148007	7/13/2018	In Force	Packet Shaping In A Network Processor
MP12562	MP12562	US	14/193,658	2/28/2014	9588920	3/7/2017	In Force	METHOD AND SYSTEM FOR PORT TRUNKING
MP12564	MP12564	US	14/201,594	3/7/2014	9529532	12/27/2016	In Force	Method And Apparatus For Memory Allocation In A Multi-Node System
MP12564	MP12564HK	HK	17104455.1	12/30/2014			Pending	Method And Apparatus For Memory Allocation In A Multi-Node System
MP12564	MP12564TW	TW	104104217	2/9/2015	I519958	2/1/2016	In Force	Method And Apparatus For Memory Allocation In A Multi-Node System
MP12564	MP12564WO	WO	PCT/US2014/07280	12/30/2014			Pending	Method And Apparatus For Memory Allocation In A Multi-Node System
MP12564	MP12564WOC	CN	201480076878.1	12/30/2014	ZL20148007	3/1/2019	In Force	Method and apparatus for memory allocation in multi-node system
MP12565	MP12565	US	14/201,513	3/7/2014	9372800	6/21/2016	In Force	Inter-Chip Interconnect Protocol For A Multi-Chip System
MP12565	MP12565TW	TW	104107158	3/6/2015	I541649	7/11/2016	In Force	System and method of inter-chip interconnect protocol for a multi-chip system
MP12566	MP12566	US	14/201,557	3/7/2014			Pending	Method And System For Ordering I/O Access In A Multi-Node Environment
MP12566	MP12566TW	TW	104105256	2/16/2015	I547870	9/1/2016	In Force	Method And System For Ordering I/O Access In A Multi-Node Environment
MP12567	MP12567	US	14/201,541	3/7/2014	9411644	8/9/2016	In Force	Method And System For Work Scheduling In A Multi-Chip System
MP12567	MP12567D1	US	15/200,587	7/1/2016	10169080	1/1/2019	In Force	Method For Work Scheduling In A Multi-Chip System
MP12567	MP12567TW	TW	104105255	2/16/2015	I543073	7/21/2016	In Force	Method And System For Work Scheduling In A Multi-Chip System
MP12569	MP12569	US	14/230,768	3/31/2014	9384008	7/5/2016	In Force	METHOD AND SYSTEM FOR OPERATING SYSTEM RECOVERY FROM A NETWORK DEVI
MP12571	MP12571	US	14/252,390	4/14/2014	9438561	9/6/2016	In Force	Processing Of Finite Automata Based On A Node Cache
MP12572	MP12572	US	14/252,299	4/14/2014	10110558	10/23/2018	In Force	Processing Of Finite Automata Based On Memory Hierarchy
MP12573	MP12573	US	14/252,354	4/14/2014	9823895	11/21/2017	In Force	Memory Management For Finite Automata Processing
MP12574	MP12574	US	14/252,293	4/14/2014	10002326	6/19/2018	In Force	Compilation Of Finite Automata Based On Memory Hierarchy
MP12574	MP12574CN	CN	2014104334020	8/28/2014	ZL20141043	11/13/2018	In Force	Compilation Of Finite Automata Based On Memory Hierarchy
MP12574	MP12574HK	HK	16102603.7	8/28/2014			Pending	Compilation Of Finite Automata Based On Memory Hierarchy
MP12575	MP12575	US	14/288,121	5/27/2014	9355206	5/31/2016	In Force	SYSTEM AND METHOD FOR AUTOMATED FUNCTIONAL COVERAGE GENERATION AN
MP12575	MP12575TW	TW	104108422	3/17/2015	I627547	6/21/2018	In Force	System and method for automated functional coverage generation and management
MP12576	MP12576	US	14/264,927	4/29/2014	9483290	11/1/2016	In Force	METHOD AND SYSTEM FOR VIRTUAL MACHINE COMMUNICATION
MP12577	MP12577	US	14/264,957	4/29/2014	9229893	1/5/2016	In Force	SYSTEMS AND METHODS FOR MANAGING DIRECT MEMORY ACCESS OPERATIONS
MP12578	MP12578	US	14/300,552	6/10/2014	9294567	3/22/2016	In Force	SYSTEMS AND METHODS FOR ENABLING ACCESS TO EXTENSIBLE STORAGE DEVICES
MP12578	MP12578-4	US	14/496,916	9/25/2014	9819739	11/14/2017	In Force	SYSTEMS AND METHODS FOR SUPPORTING HOT PLUGGING OF REMOTE STORAGE D
MP12578	MP12578-5	US	14/537,758	11/10/2014	9430268	8/30/2016	In Force	SYSTEMS AND METHODS FOR SUPPORTING MIGRATION OF VIRTUAL MACHINES ACC
MP12578	MP12578I1	US	15/041,892	2/11/2016	9529773	12/27/2016	In Force	SYSTEMS AND METHODS FOR ENABLING ACCESS TO EXTENSIBLE REMOTE STORAGE
MP12578	MP12578TW	TW	104106790	3/4/2015	I621023	4/11/2018	In Force	SYSTEMS AND METHODS FOR SUPPORTING HOT PLUGGING OF REMOTE STORAGE D
MP12578	MP12578TW-3	TW	104106793	3/4/2015	I637613	10/1/2018	In Force	SYSTEMS AND METHODS FOR ENABLING ACCESS TO EXTENSIBLE STORAGE DEVICES
MP12578	MP12578TW-5	TW	104111571	4/10/2015	I647573	1/11/2019	In Force	Systems and methods for supporting migration of virtual machines accessing remote

PATENT
REEL: 057897 FRAME: 0531

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12579	MP12579	US	14/289,533	5/28/2014			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN A NETWORK
MP12579	MP12579CN	CN	201510257702.2	5/19/2015			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN A NETWORK
MP12579	MP12579HK	HK	16108885.3	5/19/2015			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN A NETWORK
MP12579	MP12579IN	IN	835/DEL/2015	3/25/2015			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN A NETWORK
MP12579	MP12579JP	JP	2015-107430	5/27/2015			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN NETWORK S
MP12579	MP12579KR	KR	1020150073195	5/26/2015			Pending	METHOD AND APPARATUS FOR FLEXIBLE AND EFFICIENT ANALYTICS IN A NETWORK
MP12580	MP12580	US	14/289,548	5/28/2014	9773036	9/26/2017	In Force	METHOD AND APPARATUS FOR TABLE AGING IN A NETWORK SWITCH
MP12580	MP12580CN	CN	2015102546804	5/18/2015			Pending	METHOD AND APPARATUS FOR TABLE AGING IN A NETWORK SWITCH
MP12580	MP12580D1	US	15/675,336	8/11/2017	10216780	2/26/2019	In Force	METHOD AND APPARATUS FOR TABLE AGING IN A NETWORK SWITCH
MP12580	MP12580HK	HK	16108887.1	5/18/2015			Pending	METHOD AND APPARATUS FOR TABLE AGING IN A NETWORK SWITCH
MP12581	MP12581-4	US	14/723,858	5/28/2015	9571279	2/14/2017	In Force	SYSTEMS AND METHODS FOR SECURED BACKUP OF HARDWARE SECURITY MODULES
MP12581	MP12581TW-5	TW	104119522	6/17/2015	I632797	8/11/2018	In Force	SYSTEMS AND METHODS FOR SECURED BACKUP OF HARDWARE SECURITY MODULES
MP12582	MP12582	US	14/302,351	6/11/2014	9413357	8/9/2016	In Force	HIERARCHICAL STATISTICALLY MULTIPLEXED COUNTERS AND A METHOD THEROF
MP12582	MP12582CN	CN	2015103201878	6/11/2015			Pending	HIERARCHICAL STATISTICALLY MULTIPLEXED COUNTERS AND A METHOD THEREOF
MP12582	MP12582D1	US	15/202,428	7/5/2016	10038448	7/31/2018	In Force	HIERARCHICAL STATISICALLY MULTIPLEXED COUNTERS AND A METHOD THEREOF
MP12582	MP12582D2	US	16/019,780	6/27/2018			Pending	HIERARCHICAL STATISICALLY MULTIPLEXED COUNTERS AND A METHOD THEREOF
MP12582	MP12582HK	HK	16108891.5	6/11/2015			Pending	HIERARCHICAL STATISTICALLY MULTIPLEXED COUNTERS AND A METHOD THEREOF
MP12582	MP12582TW	TW	104112176	4/16/2015	I656476	4/11/2019	In Force	HIERARCHICAL STATISTICALLY MULTIPLEXED COUNTERS AND ARCHITECTURE, METH
MP12583	MP12583CN	CN	201510253417.3	5/18/2015			Pending	COUNTER WITH OVERFLOW FIFO AND A METHOD THEREOF
MP12583	MP12583HK	HK	16108886.2	5/18/2015			Pending	COUNTER WITH OVERFLOW FIFO AND A METHOD THEREOF
MP12584	MP12584	US	14/302,706	6/12/2014	9423980	8/23/2016	In Force	METHODS AND SYSTEMS FOR AUTOMATICALLY ADDING INTELLIGENT STORAGE ADA
MP12585	MP12585	US	14/309,659	6/19/2014	9635146	4/25/2017	In Force	METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEADER
MP12585	MP12585C1	US	15/457,970	3/13/2017			Pending	METHOD OF USING BIT VECTORS TO ALLOW EXPASION AND COLLAPSE OF HEADER L
MP12585	MP12585CN	CN	2015102724093	5/25/2015			Pending	A METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEAD
MP12585	MP12585EP	EP	15172929.0	6/19/2015	2958287	6/19/2019	In Force	A METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEAD
MP12585	MP12585EPDE	DE	15172929.0	6/19/2015	6020150302	6/19/2019	In Force	A METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEAD
MP12585	MP12585HK	HK	16108884.4	5/25/2015			Pending	A METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEAD
MP12585	MP12585KR	KR	1020150086042	6/17/2015			Pending	METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEADER
MP12585	MP12585TW	TW	104111755	4/13/2015	I664843	7/1/2019	In Force	A METHOD OF USING BIT VECTORS TO ALLOW EXPANSION AND COLLAPSE OF HEAD
MP12586	MP12586	US	14/309,726	6/19/2014	9516145	12/6/2016	In Force	METHOD OF EXTRACTING DATA FROM PACKETS AND AN APPARATUS THEREOF
MP12586	MP12586CN	CN	201510236939.2	5/11/2015			Pending	A METHOD OF EXTRACTING DATA FROM PACKETS AND AN APPARATUS THEREOF
MP12586	MP12586HK	HK	16108889.9	5/11/2015			Pending	A METHOD OF EXTRACTING DATA FROM PACKETS AND AN APPARATUS THEREOF
MP12586	MP12586JP	JP	2015-122563	6/18/2015			Pending	METHOD OF EXTRACTING DATA FROM PACKETS, AND APPARATUS THEREOF
MP12586	MP12586KR	KR	1020150087785	6/19/2015			Pending	A METHOD OF EXTRACTING DATA FROM PACKETS AND AN APPARATUS THEREOF

PATENT
REEL: 057897 FRAME: 0532

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12587	MP12587	US	14/309,802	6/19/2014	9628385	4/18/2017	In Force	METHOD OF IDENTIFYING INTERNAL DESTINATIONS OF NETWORK PACKETS AND AN
MP12587	MP12587C1	US	15/457,959	3/13/2017	10397113	8/27/2019	In Force	METHOD OF IDENTIFYING INTERNAL DESTINATIONS OF NETWORK PACKETS AND AN
MP12587	MP12587CN	CN	2015102296103	5/7/2015			Pending	METHOD OF IDENTIFYING INTERNAL DESTINATIONS OF NETWORK PACKETS AND AN
MP12587	MP12587HK	HK	16108883.5	5/7/2015			Pending	A METHOD OF IDENTIFYING INTERNAL DESTINATIONS OF NETWORK PACKETS AND A
MP12587	MP12587TW	TW	104110829	4/2/2015	I660609	5/21/2019	In Force	A method of identifying internal destinations of network packets and an apparatus th
MP12588	MP12588	US	14/309,789	6/19/2014	9742694	8/22/2017	In Force	METHOD OF DYNAMICALLY RENUMBERING PORTS AND AN APPARATUS THEREOF
MP12588	MP12588C1	US	15/653,021	7/18/2017			Pending	METHOD OF DYNAMICALLY RENUMBERING PORTS AND AN APPARATUS THEREOF
MP12589	MP12589	US	14/309,773	6/19/2014	10050833	8/14/2018	In Force	METHOD OF REDUCING LATENCY IN A FLEXIBLE PARSER AND AN APPARATUS THERE
MP12589	MP12589CN	CN	2015102297708	5/7/2015			Pending	METHOD OF REDUCING LATENCY IN A FLEXIBLE PARSER AND AN APPARATUS THERE
MP12589	MP12589HK	HK	16108892.4	5/7/2015			Pending	A METHOD OF REDUCING LATENCY IN A FLEXIBLE PARSER AND AN APPARATUS THER
MP12590	MP12590	US	14/309,763	6/19/2014			Pending	METHOD OF HANDLING LARGE PROTOCOL LAYERS FOR CONFIGURABLE EXTRACTION
MP12590	MP12590CN	CN	2015102297799	5/7/2015			Pending	METHOD OF HANDLING LARGE PROTOCOL LAYERS FOR CONFIGURABLE EXTRACTION
MP12590	MP12590HK	HK	16108890.6	5/7/2015			Pending	A METHOD OF HANDLING LARGE PROTOCOL LAYERS FOR CONFIGURABLE EXTRACTI
MP12591	MP12591	US	14/309,739	6/19/2014	9438703	9/6/2016	In Force	METHOD OF FORMING A HASH INPUT FROM PACKET CONTENTS AND AN APPARATU
MP12591	MP12591CN	CN	2015102367984	5/11/2015			Pending	A METHOD OF FORMING A HASH INPUT FROM PACKET CONTENTS AND AN APPARAT
MP12591	MP12591HK	HK	16108888.0	5/11/2015			Pending	A METHOD OF FORMING A HASH INPUT FROM PACKET CONTENTS AND AN APPARAT
MP12591	MP12591JP	JP	2015-122564	6/18/2015			Pending	METHOD OF FORMING HASH INPUT FROM PACKET CONTENTS, AND APPARATUS TH
MP12591	MP12591KR	KR	1020150087800	6/19/2015			Pending	METHOD OF FORMING A HASH INPUT FROM PACKET CONTENTS AND AN APPARATU
MP12592	MP12592	US	14/309,679	6/19/2014	9531849	12/27/2016	In Force	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592CN	CN	2015102764264	5/26/2015			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592EP	EP	15172935.7	6/19/2015			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592HK	HK	16108882.6	7/26/2016			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592IN	IN	841/DEL/2015	3/26/2015			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592JP	JP	2015-122562	6/18/2015			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12592	MP12592KR	KR	1020150086078	6/17/2015			Pending	METHOD OF SPLITTING A PACKET INTO INDIVIDUAL LAYERS FOR MODIFICATION AN
MP12593	MP12593	US	14/309,650	6/19/2014	9531848	12/27/2016	In Force	METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE M
MP12593	MP12593CN	CN	2015102726703	5/25/2015			Pending	A METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE
MP12593	MP12593EP	EP	15172917.5	6/19/2015	2958286	5/1/2019	In Force	A METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE
MP12593	MP12593EPDE	DE	15172917.5	6/19/2015	6020150291	5/1/2019	In Force	A METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE
MP12593	MP12593HK	HK	16108894.2	5/25/2015			Pending	A METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE
MP12593	MP12593IN	IN	847/DEL/2015	3/26/2015			Pending	A METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE
MP12593	MP12593JP	JP	2015-122561	6/18/2015			Pending	METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE M
MP12593	MP12593KR	KR	1020150084526	6/15/2015			Pending	METHOD OF USING GENERIC MODIFICATION INSTRUCTIONS TO ENABLE FLEXIBLE M
MP12594	MP12594	US	14/309,633	6/19/2014	9497294	11/15/2016	In Force	METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A PA

PATENT
REEL: 057897 FRAME: 0533

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12594	MP12594CN	CN	201510272163.X	5/25/2015			Pending	A METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A P
MP12594	MP12594EP	EP	15172911.8	6/19/2015	2958296	3/27/2019	In Force	A METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A P
MP12594	MP12594EPDE	DE	15172911.8	6/19/2015	602015027(	3/27/2019	In Force	A METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A P
MP12594	MP12594HK	HK	16104736.3	4/26/2016			Pending	A METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A P
MP12594	MP12594IN	IN	836/DEL/2015	3/25/2015			Pending	A METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A P
MP12594	MP12594JP	JP	2015-122560	6/18/2015			Pending	METHOD AND DEVICE FOR IDENTIFYING STRUCTURE OF PACKET BY USING UNIQUE I
MP12594	MP12594KR	KR	1020150083631	6/12/2015			Pending	METHOD OF USING A UNIQUE PACKET IDENTIFIER TO IDENTIFY STRUCTURE OF A PA
MP12595	MP12595	US	14/309,619	6/19/2014	9473601	10/18/2016	In Force	METHOD OF REPRESENTING A GENERIC FORMAT HEADER USING CONTINUOUS BYT
MP12595	MP12595CN	CN	2015102724360	5/25/2015			Pending	A METHOD OF REPRESENTING A GENERIC FORMAT HEADER USING CONTINUOUS BY
MP12595	MP12595HK	HK	16107161.0	5/25/2015			Pending	A METHOD OF REPRESENTING A GENERIC FORMAT HEADER USING CONTINUOUS BY
MP12596	MP12596	US	14/309,603	6/19/2014	9961167	5/1/2018	In Force	METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGRA
MP12596	MP12596CN	CN	2015102765888	5/26/2015			Pending	Method of modifying packets to a generic format for enabling programmable modific
MP12596	MP12596EP	EP	15172942.3	6/19/2015	2958288	5/1/2019	In Force	A METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGR
MP12596	MP12596EPDE	DE	15172942.3	6/19/2015	6020150291	5/1/2019	In Force	A METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGR
MP12596	MP12596HK	HK	16108893.3	5/26/2015			Pending	A METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGR
MP12596	MP12596IN	IN	834/DEL/2015	3/25/2015			Pending	A METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGR
MP12596	MP12596JP	JP	2015-122559	6/18/2015			Pending	Method of modifying packets to a generic format for enabling programmable modific
MP12596	MP12596KR	KR	1020150084520	6/15/2015			Pending	METHOD OF MODIFYING PACKETS TO A GENERIC FORMAT FOR ENABLING PROGRA
MP12598	MP12598	US	14/312,130	6/23/2014	9436654	9/6/2016	In Force	METHODS AND SYSTEMS FOR PROCESSING TASK MANAGEMENT FUNCTIONS IN A CL
MP12600	MP12600	US	14/325,841	7/8/2014	9785403	10/10/2017	In Force	Engine Architecture For Processing Finite Automata
MP12600	MP12600C1	US	15/703,638	9/13/2017	10466964	11/5/2019	In force	Engine Architecture For Processing Finite Automata
MP12600	MP12600CN	CN	2014104323187	8/28/2014	ZL20141043	3/1/2019	In Force	Engine Architecture For Processing Finite Automata
MP12600	MP12600HK	HK	15107653.6	8/28/2014			Pending	Engine Architecture For Processing Finite Automata
MP12601	MP12601	US	14/663,912	3/20/2015	9692560	6/27/2017	In Force	METHODS AND SYSTEMS FOR RELIABLE NETWORK COMMUNICATION
MP12602	MP12602	US	14/328,951	7/11/2014			Pending	MANAGING INSTRUCTION ORDER IN A PROCESSOR PIPELINE
MP12602	MP12602TW	TW	104114685	5/8/2015	I658407	5/1/2019	In Force	MANAGING INSTRUCTION ORDER IN A PROCESSOR PIPELINE
MP12603	MP12603	US	14/328,923	7/11/2014			Pending	MANAGING INSTRUCTION ORDER IN A PROCESSOR PIPELINE
MP12603	MP12603TW	TW	104110835	4/2/2015	I659357	5/11/2019	In Force	MANAGING INSTRUCTION ORDER IN A PROCESSOR PIPELINE
MP12603	MP12603TWD1	TW	108111505	4/2/2015			Pending	MANAGING INSTRUCTION ORDER IN A PROCESSOR PIPELINE
MP12604	MP12604	US	14/331,105	7/14/2014	10198389	2/5/2019	In Force	BASEBOARD INTERCONNECTION DEVICE, SYSTEM AND METHOD
MP12606	MP12606	US	14/339,086	7/23/2014	9477424	10/25/2016	In Force	METHODS AND SYSTEMS FOR USING AN INTELLIGENT STORAGE ADAPTER FOR REPU
MP12607	MP12607	US	14/724,273	5/28/2015	9819515	11/14/2017	In Force	INTEGRATED FABRIC ADAPTER AND ASSOCIATED METHODS THEREOF
MP12609	MP12609	US	14/447,732	7/31/2014	9678779	6/13/2017	In Force	METHOD AND AN APPARATUS FOR CO-PROCESSOR DATA PLANE VIRTUALIZATION
MP12610	MP12610	US	14/464,535	8/20/2014	9477414	10/25/2016	In Force	METHODS AND SYSTEMS FOR IMPROVED CACHING WITH DATA RECOVERY

PATENT
REEL: 057897 FRAME: 0534

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12611	MP12611	US	14/470,309	8/27/2014	9311021	4/12/2016	In Force	METHODS AND SYSTEMS FOR PERFORMING A READ AHEAD OPERATION USING AN I
MP12612	MP12612	US	14/470,337	8/27/2014	9330010	5/3/2016	In Force	METHODS AND SYSTEMS FOR IMPROVED DATA CACHING IN A VIRTUALIZED ENVIRO
MP12613	MP12613	US	14/473,524	8/29/2014	9936003	4/3/2018	In Force	METHOD AND SYSTEM FOR TRANSMITTING INFORMATION IN A NETWORK
MP12614	MP12614	US	14/038,549	9/26/2013	9671844	6/6/2017	In Force	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614C1	US	15/499,531	4/27/2017	10152102	12/11/2018	In Force	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614C1C1	US	16/210,987	12/5/2018			Pending	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614CN	CN	2014104983609	9/25/2014	ZL20141049	7/21/2017	In Force	Method and apparatus for managing global chip power on multicore system on chip
MP12614	MP12614CND1	CN	2017105321604	9/25/2014			Pending	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614DE	DE	10 2014 014 301.5	9/25/2014	10 2014 014	8/16/2018	In Force	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614HK	HK	15109894.1	9/25/2014	1209210B	5/4/2018	In Force	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12614	MP12614JP	JP	2014-192982	9/22/2014	6169547	7/7/2017	In Force	METHOD AND APPARATUS FOR MANAGING GLOBAL CHIP POWER ON MULTICORE S
MP12614	MP12614KR	KR	20140128554	9/25/2014	101701004C	1/23/2017	In Force	Method And Apparatus For Managing Global Chip Power On A Multicore System On
MP12615	MP12615	US	14/494,187	9/23/2014	9729338	8/8/2017	In Force	FAST HARDWARE SWITCHOVER IN A CONTROL PATH IN A NETWORK ASIC
MP12615	MP12615C1	US	15/642,141	7/5/2017	10341130	7/2/2019	In Force	FAST HARDWARE SWITCHOVER IN A CONTROL PATH IN A NETWORK ASIC
MP12616	MP12616	US	14/494,291	9/23/2014	9565136	2/7/2017	In Force	MULTICAST REPLICATION ENGINE OF A NETWORK ASIC AND METHODS THEREOF
MP12617	MP12617	US	14/494,168	9/23/2014	9813327	7/11/2017	In Force	HIERARCHICAL HARDWARE LINKED LIST APPROACH FOR MULTICAST REPLICATION E
MP12617	MP12617C1	US	15/725,643	10/5/2017	10205649	2/12/2019	In Force	HIERARCHICAL HARDWARE LINKED LIST APPROACH FOR MULTICAST REPLICATION E
MP12617	MP12617C1D1	US	16/232,882	12/26/2018			Pending	HIERARCHICAL HARDWARE LINKED LIST APPROACH FOR MULTICAST REPLICATION E
MP12618	MP12618	US	14/493,865	9/23/2014	9882678	1/30/2018	In Force	Method and Apparatus for Improving Data Integrity Using Compressed Soft Informati
MP12619	MP12619	US	14/494,229	9/23/2014	9760418	9/12/2017	In Force	SESSION BASED PACKET MIRRORING IN A NETWORK ASIC
MP12619	MP12619C1	US	15/672,082	8/8/2017	10417067	9/17/2019	In Force	SESSION BASED PACKET MIRRORING IN A NETWORK ASIC
MP12620	MP12620	US	14/493,897	9/23/2014	9503218	11/22/2016	In Force	Method and Apparatus for Quantizing Soft Information using Non-Linear LLR Quantiz
MP12620	MP12620-2	US	14/493,953	9/23/2014	9768912	9/19/2017	In Force	Method and Apparatus for Quantizing Soft Information using Linear Quantization
MP12621	MP12621	US	14/498,580	9/26/2014	9460017	10/4/2016	In Force	METHODS AND SYSTEMS FOR EFFICIENT CACHE MIRRORING
MP12622	MP12622	US	14/716,689	5/19/2015	10129162	11/13/2018	In Force	SYSTEMS AND METHODS FOR DEFINING STORAGE
MP12623	MP12623	US	14/870,675	9/30/2015			Pending	SYSTEMS AND METHODS FOR ALLOWING FLEXIBLE CHIP CONFIGURATION BY EXTER
MP12624	MP12624	US	14/514,708	10/15/2014	9690590	6/27/2017	In Force	FLEXIBLE INSTRUCTION EXECUTION IN A PROCESSOR PIPELINE
MP12624	MP12624TW	TW	103138148	11/4/2014	I613590	2/1/2018	In Force	FLEXIBLE INSTRUCTION EXECUTION IN A PROCESSOR PIPELINE
MP12625	MP12625	US	14/514,596	10/15/2014	9747109	8/29/2017	In Force	FLEXIBLE INSTRUCTION EXECUTION IN A PROCESSOR PIPELINE
MP12625	MP12625TW	TW	103138147	11/4/2014	I613589	2/1/2018	In Force	FLEXIBLE INSTRUCTION EXECUTION IN A PROCESSOR PIPELINE
MP12626	MP12626	US	14/521,333	10/22/2014			Pending	APPARATUS AND A METHOD OF DETECTING ERRORS ON REGISTERS
MP12627	MP12627	US	14/521,354	10/22/2014	9990324	6/5/2018	In Force	TWO MODES OF A CONFIGURATION INTERFACE OF A NETWORK ASIC
MP12627	MP12627D1	US	15/969,681	5/2/2018			Pending	METHOD OF IMPLEMENTING A NETWORK ASIC IN A NETWORK DEVICE
MP12628	MP12628	US	14/521,359	10/22/2014	9542342	1/10/2017	In Force	SMART HOLDING REGISTERS TO ENABLE MULTIPLE REGISTER ACCESSES

PATENT
REEL: 057897 FRAME: 0535

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12629	MP12629	US	14/521,367	10/22/2014	10078605	9/18/2018	In Force	MULTIPLE-INTERRUPT PROPAGATION SCHEME IN A NETWORK ASIC
MP12630	MP12630	US	14/530,388	10/31/2014	9936021	4/3/2018	In Force	METHODS AND SYSTEMS FOR A MULTI-FUNCTION ADAPTER
MP12631	MP12631	US	14/667,485	3/24/2015	9934177	4/3/2018	In Force	METHODS AND SYSTEMS FOR ACCESSING STORAGE USING A NETWORK INTERFACE C
MP12632	MP12632	US	14/536,937	11/10/2014	10116564	10/30/2018	In Force	HYBRID WILDCARD MATCH TABLE
MP12632	MP12632CN	CN	2015107573136	11/9/2015			Pending	HYBRID WILDCARD MATCH TABLE
MP12632	MP12632I1	US	14/932,791	11/4/2015			Pending	HYBRID WILDCARD MATCH TABLE
MP12632	MP12632TW	TW	104134823	10/23/2015	I667900	8/1/2019	In Force	HYBRID WILDCARD MATCH TABLE
MP12633	MP12633	US	14/538,484	11/11/2014	9645790	5/9/2017	In Force	Adder Decoder
MP12634	MP12634	US	14/540,414	11/13/2014	9858222	1/2/2018	In Force	Register Access Control Among Multiple Devices
MP12635	MP12635	US	14/540,175	11/13/2014	10013385	7/3/2018	In Force	Programmable Validation Of Transaction Requests
MP12636	MP12636	US	14/540,436	11/13/2014	10002099	6/19/2018	In Force	Arbitrated Access To Resources Among Multiple Devices
MP12637	MP12637	US	14/540,379	11/13/2014	9569362	2/14/2017	In Force	Programmable Ordering And Prefetch
MP12638	MP12638	US	14/540,656	11/13/2014			Pending	Independent Ordering of Independent Transactions
MP12639	MP12639	US	14/542,350	11/14/2014	10110515	10/23/2018	In Force	PACKET SCHEDULING USING HIERARCHICAL SCHEDULING PROCESS
MP12640	MP12640	US	14/542,039	11/14/2014	9417655	8/16/2016	In Force	FREQUENCY DIVISION CLOCK ALIGNMENT
MP12640	MP12640TW	TW	104112338	4/17/2015	I642277	11/21/2018	In Force	FREQUENCY DIVISION CLOCK ALIGNMENT
MP12641	MP12641	US	14/542,298	11/14/2014	10291540	5/14/2019	In Force	METHOD AND APPARATUS FOR PERFORMING A WEIGHTED QUEUE SCHEDULING USI
MP12642	MP12642	US	14/541,807	11/14/2014	9697137	7/4/2017	In Force	FILTERING TRANSLATION LOOKASIDE BUFFER INVALIDATIONS
MP12644	MP12644	US	14/541,902	11/14/2014	9665505	5/30/2017	In Force	MANAGING BUFFERED COMMUNICATION BETWEEN SOCKETS
MP12644	MP12644TW	TW	104110836	4/2/2015	I658362	5/1/2019	In Force	MANAGING BUFFERED COMMUNICATION BETWEEN SOCKETS
MP12645	MP12645	US	14/541,882	11/14/2014	10007524	6/26/2018	In Force	MANAGING HISTORY INFORMATION FOR BRANCH PREDICTION
MP12645	MP12645TW	TW	104112340	4/17/2015	I648624	1/21/2019	In Force	MANAGING HISTORY INFORMATION FOR BRANCH PREDICTION
MP12646	MP12646	US	14/541,977	11/14/2014	9470719	10/18/2016	In Force	TESTING SEMICONDUCTOR DEVICES
MP12647	MP12647	US	14/616,580	2/6/2015	9904511	2/27/2018	In Force	HIGH PERFORMANCE SHIFTER CIRCUIT
MP12648	MP12648	US	14/542,060	11/14/2014	9601181	3/21/2017	In Force	CONTROLLED MULTI-STEP DE-ALIGNMENT OF CLOCKS
MP12649	MP12649	US	14/542,136	11/14/2014	9910776	3/6/2018	In Force	INSTRUCTION ORDERING FOR IN-PROGRESS OPERATIONS
MP12649	MP12649C1	US	15/890,921	2/7/2018	10339054	7/2/2019	In Force	INSTRUCTION ORDERING FOR IN-PROGRESS OPERATIONS
MP12649	MP12649TW	TW	104110197	3/30/2015	I664571	7/1/2019	In Force	INSTRUCTION ORDERING FOR IN-PROGRESS OPERATIONS
MP12649	MP12649TWD1	TW	108117952	5/24/2019			Pending	INSTRUCTION ORDERING FOR IN-PROGRESS OPERATIONS
MP12650	MP12650	US	14/542,118	11/14/2014	9870328	1/16/2018	In Force	MANAGING BUFFERED COMMUNICATION BETWEEN CORES
MP12651	MP12651	US	14/542,188	11/14/2014	9613679	4/4/2017	In Force	CONTROLLED DYNAMIC DE-ALIGNMENT OF CLOCKS
MP12652	MP12652	US	14/542,202	11/14/2014	9502099	11/22/2016	In Force	MANAGING SKEW IN DATA SIGNALS WITH MULTIPLE MODES
MP12652	MP12652I1	US	14/672,787	3/30/2015	9607672	3/28/2017	In Force	MANAGING SKEW IN DATA SIGNALS WITH ADJUSTABLE STROBE
MP12653	MP12653	US	14/541,952	11/14/2014	9570128	2/14/2017	In Force	MANAGING SKEW IN DATA SIGNALS

PATENT
REEL: 057897 FRAME: 0536

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12654	MP12654	US	14/940,982	11/13/2015	10078601	9/18/2018	In Force	APPROACH FOR INTERFACING A PIPELINE WITH TWO OR MORE INTERFACES IN A PR
MP12655	MP12655	US	14/541,841	11/14/2014	9703669	7/11/2017	In Force	APPARATUS AND METHOD FOR DISTRIBUTED INSTRUCTION TRACE IN A PROCESSOR
MP12656	MP12656	US	14/542,485	11/14/2014	10116772	10/30/2018	In Force	NETWORK SWITCHING WITH CO-RESIDENT DATA-PLANE AND NETWORK INTERFACE
MP12656	MP12656D1	US	16/132,424	9/16/2018			Pending	NETWORK SWITCHING WITH CO-RESIDENT DATA-PLANE AND NETWORK INTERFACE
MP12657	MP12657	US	14/542,383	11/14/2014			Pending	APPARATUS AND METHOD FOR A MULTI-ENTITY SECURE SOFTWARE TRANSFER
MP12658	MP12658	US	14/541,726	11/14/2014	9684606	6/20/2017	In Force	TRANSLATION LOOKASIDE BUFFER INVALIDATION SUPPRESSION
MP12658	MP12658TW	TW	104113187	4/24/2015	I646421	1/1/2019	In Force	TRANSLATION LOOKASIDE BUFFER INVALIDATION SUPPRESSION
MP12659	MP12659	US	14/541,616	11/14/2014	9405702	8/2/2016	In Force	CACHING TLB TRANSLATIONS USING A UNIFIED PAGE TABLE WALKER CACHE
MP12659	MP12659TW	TW	104110648	4/1/2015	I641946	11/21/2018	In Force	CACHING TLB TRANSLATIONS USING A UNIFIED PAGE TABLE WALKER CACHE
MP12660	MP12660	US	14/541,498	11/14/2014	9501425	11/22/2016	In Force	TRANSLATION LOOKASIDE BUFFER MANAGEMENT
MP12660	MP12660TW	TW	104110402	3/31/2015			Pending	TRANSLATION LOOKASIDE BUFFER MANAGEMENT
MP12661	MP12661	US	14/541,685	11/14/2014	10394730	8/27/2019	In Force	DISTRIBUTED INTERRUPT SCHEME IN A MULTI-PROCESSOR SYSTEM
MP12662	MP12662	US	14/541,971	11/14/2014	9404970	8/2/2016	In Force	DEBUG INTERFACE FOR MULTIPLE CPU CORES
MP12663	MP12663	US	14/542,528	11/14/2014	9813342	11/7/2017	In Force	METHOD AND SYSTEM FOR IMPROVED LOAD BALANCING OF RECEIVED NETWORK T
MP12664	MP12664	US	14/941,182	11/13/2015	10303514	5/28/2019	In Force	SHARING RESOURCES IN A MULTI-CONTEXT COMPUTING SYSTEM
MP12665	MP12665	US	14/940,585	11/13/2015			Pending	IMPLEMENTING 128-BIT SIMD OPERATIONS ON A 64-BIT DATAPATH
MP12665	MP12665CN	CN	2015107789847.X	11/13/2015			Pending	IMPLEMENTING 128-BIT SIMD OPERATIONS ON A 64-BIT DATAPATH
MP12665	MP12665TW	TW	104137305	11/12/2015			Pending	IMPLEMENTING 128-BIT SIMD OPERATIONS ON A 64-BIT DATAPATH
MP12666	MP12666	US	14/542,509	11/14/2014	10050896	8/14/2018	In Force	MANAGEMENT OF AN OVER-SUBSCRIBED SHARED BUFFER
MP12667	MP12667	US	14/541,769	11/14/2014	9928193	3/27/2018	In Force	DISTRIBUTED TIMER SUBSYSTEM
MP12668	MP12668	US	14/940,981	11/13/2015	9933809	4/3/2018	In Force	Automatic Data Rate Matching
MP12669	MP12669	US	14/940,538	11/13/2015			Pending	CARRY CHAIN FOR SIMD OPERATIONS
MP12670	MP12670	US	14/541,917	11/14/2014	9824058	11/21/2017	In Force	Bypass FIFO For Multiple Virtual Channels
MP12671	MP12671	US	14/941,082	11/13/2015	9678717	6/13/2017	In Force	DISTRIBUTING RESOURCE REQUESTS IN A COMPUTING SYSTEM
MP12672	MP12672	US	14/542,216	11/14/2014	9411361	8/9/2016	In Force	FREQUENCY DIVISION CLOCK ALIGNMENT USING PATTERN SELECTION
MP12673	MP12673	US	14/542,065	11/14/2014	9568944	2/14/2017	In Force	DISTRIBUTED TIMER SUBSYSTEM ACROSS MULTIPLE DEVICES
MP12674	MP12674	US	14/940,679	11/13/2015	9703722	7/11/2017	In Force	METHOD AND SYSTEM FOR COMPRESSING DATA FOR A TRANSLATION LOOK ASIDE B
MP12674	MP12674C1	US	15/598,719	5/18/2017	9772952	9/26/2017	In Force	METHOD AND SYSTEM FOR COMPRESSING DATA FOR A TRANSLATION LOOK ASIDE B
MP12675	MP12675	US	14/609,164	1/29/2015	9740807	8/22/2017	In Force	METHOD TO MEASURE EDGE-RATE TIMING PENALTY OF DIGITAL INTEGRATED CIRCU
MP12676	MP12676	US	14/548,040	11/19/2014	9674303	6/6/2017	In Force	METHODS AND SYSTEMS FOR EFFICIENT DATA TRANSMISSION IN A DATA CENTER BY
MP12677	MP12677-1	US	14/681,978	4/8/2015	9571412	2/14/2017	In Force	SYSTEMS AND METHODS FOR HARDWARE ACCELERATED TIMER IMPLEMENTATION
MP12677	MP12677-2	US	14/939,982	11/12/2015	10084719	9/25/2018	In Force	SYSTEMS AND METHODS FOR HARDWARE ACCELERATED METERING FOR OPENFLO
MP12677	MP12677TW	TW	104118717	6/10/2015	I631841	8/1/2018	In Force	SYSTEMS AND METHODS FOR HARDWARE ACCELERATED TIMER IMPLEMENTATION
MP12678	MP12678	US	14/577,448	12/19/2014	9866657	1/9/2018	In Force	NETWORK SWITCHING WITH LAYER 2 SWITCH COUPLED CO-RESIDENT DATA-PLANE

PATENT
REEL: 057897 FRAME: 0537

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12679	MP12679	US	14/585,761	12/30/2014	9396023	7/19/2016	In Force	METHODS AND SYSTEMS FOR PARALLEL DISTRIBUTED COMPUTATION
MP12680	MP12680	US	14/593,898	1/9/2015	9483207	11/1/2016	In Force	METHODS AND SYSTEMS FOR EFFICIENT CACHING USING AN INTELLIGENT STORAGE
MP12681	MP12681	US	14/597,030	1/14/2015	9952979	4/24/2018	In Force	METHODS AND SYSTEMS FOR DIRECT MEMORY ACCESS OPERATIONS
MP12682	MP12682	US	14/609,945	1/30/2015	9426084	8/23/2016	In Force	METHODS AND SYSTEMS FOR CONTROLLING TRANSMISSION RATES IN NETWORKS
MP12683	MP12683	US	14/634,446	2/27/2015	9600614	3/21/2017	In Force	AUTOMATED FLIP-FLOP INSERTIONS IN PHYSICAL DESIGN WITHOUT PERTURBATION
MP12684	MP12684	US	14/617,699	2/9/2015	9778315	10/3/2017	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD HAVING AGENT LOOPBACK FU
MP12685	MP12685	US	14/617,610	2/9/2015	9330227	5/3/2016	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD INCLUDING A DISPATCHER
MP12686	MP12686	US	14/617,546	2/9/2015	10082538	9/25/2018	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD
MP12688	MP12688	US	14/617,645	2/9/2015	9506982	11/29/2016	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD INCLUDING A GENERIC MONIT
MP12689	MP12689	US	14/632,200	2/26/2015	9590897	3/7/2017	In Force	METHODS AND SYSTEMS FOR NETWORK DEVICES AND ASSOCIATED NETWORK TRAN
MP12691	MP12691	US	14/638,266	3/4/2015	9720773	8/1/2017	In Force	MANAGING REUSE INFORMATION IN CACHES
MP12691	MP12691TW	TW	104113188	4/24/2015	I641947	11/21/2018	In Force	MANAGING REUSE INFORMATION IN CACHES
MP12692	MP12692	US	14/638,194	3/4/2015	10013360	7/3/2018	In Force	MANAGING REUSE INFORMATION WITH MULTIPLE TRANSLATION STAGES
MP12694	MP12694	US	14/637,533	3/4/2015	9678159	6/13/2017	In Force	COMMUNICATION AND CONTROL TOPOLOGY FOR EFFICIENT TESTING OF SETS OF D
MP12694	MP12694TW	TW	104108042	3/13/2015	I631355	8/1/2018	In Force	COMMUNICATION AND CONTROL TOPOLOGY FOR EFFICIENT TESTING OF SETS OF D
MP12696	MP12696	US	15/065,799	3/9/2016	10002218	6/19/2018	In Force	DESIGN AND VERIFICATION OF A MULTICHIP COHERENCE PROTOCOL
MP12697	MP12697	US	14/662,405	3/19/2015	9471509	10/18/2016	In Force	MANAGING ADDRESS-INDEPENDENT PAGE ATTRIBUTES
MP12697	MP12697TW	TW	104113191	4/24/2015	I648625	1/21/2019	In Force	MANAGING ADDRESS-INDEPENDENT PAGE ATTRIBUTES
MP12698	MP12698	US	14/664,680	3/20/2015	9600620	3/21/2017	In Force	REPEATER INSERTIONS PROVIDING REDUCED ROUTING PERTURBATION CAUSED BY F
MP12699	MP12699	US	14/667,568	3/24/2015	9900253	2/20/2018	In Force	PHANTOM QUEUE LINK LEVEL LOAD BALANCING SYSTEM, METHOD AND DEVICE
MP12699	MP12699C1	US	15/862,509	1/4/2018	10103993	10/16/2018	In Force	PHANTOM QUEUE LINK LEVEL LOAD BALANCING SYSTEM, METHOD AND DEVICE
MP12699	MP12699C1C1	US	16/126,644	9/10/2018			Pending	PHANTOM QUEUE LINK LEVEL LOAD BALANCING SYSTEM, METHOD AND DEVICE
MP12699	MP12699C1C1C	US	16/694,481	11/25/2019			Pending	PHANTOM QUEUE LINK LEVEL LOAD BALANCING SYSTEM, METHOD AND DEVICE
MP12700	MP12700	US	14/667,488	3/24/2015	10419571	9/17/2019	In Force	PACKET PROCESSOR FORWARDING DATABASE CACHE
MP12700	MP12700CN	CN	201610176470.2	3/24/2016			Pending	PACKET PROCESSOR FORWARDING DATABASE CACHE
MP12700	MP12700HK	HK	17106372.6	3/24/2016			Pending	PACKET PROCESSOR FORWARDING DATABASE CACHE
MP12700	MP12700TW	TW	105108783	3/22/2016			Pending	PACKET PROCESSOR FORWARDING DATABASE CACHE
MP12701	MP12701	US	14/672,025	3/27/2015	9817067	11/14/2017	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD INCLUDING LATENCY DETECTI
MP12702	MP12702	US	14/672,006	3/27/2015	10282315	5/7/2019	In Force	SOFTWARE ASSISTED HARDWARE CONFIGURATION FOR SOFTWARE DEFINED NETW
MP12703	MP12703	US	14/671,900	3/27/2015			Pending	METHOD AND APPARATUS FOR BYPASS ROUTING OF MULTICAST DATA PACKETS AN
MP12704	MP12704	US	14/671,983	3/27/2015	9547041	1/17/2017	In Force	TESTBENCH BUILDER, SYSTEM, DEVICE AND METHOD WITH PHASE SYNCHRONIZATI
MP12705	MP12705	US	14/671,993	3/27/2015	9372772	6/21/2016	In Force	CO-VERIFICATION - OF HARDWARE AND SOFTWARE, A UNIFIED APPROACH IN VERIFI
MP12706	MP12706	US	14/672,016	3/27/2015	10006963	6/26/2018	In Force	PACKET TRACKING IN A VERIFICATION ENVIRONMENT
MP12707	MP12707	US	14/673,835	3/30/2015	9582215	2/28/2017	In Force	PACKET PROCESSING SYSTEM, METHOD AND DEVICE UTILIZING MEMORY SHARING

PATENT
REEL: 057897 FRAME: 0538

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12707	MP12707-2	US	14/673,836	3/30/2015	9612950	4/4/2017	In Force	CONTROL PATH SUBSYSTEM, METHOD AND DEVICE UTILIZING MEMORY SHARING
MP12707	MP12707-3	US	14/673,840	3/30/2015	9652171	5/16/2017	In Force	DATAPATH SUBSYSTEM, METHOD AND DEVICE UTILIZING MEMORY SHARING
MP12707	MP12707-3C1	US	15/483,946	4/10/2017	10061513	8/28/2018	In Force	PACKET PROCESSING SYSTEM, METHOD AND DEVICE UTILIZING MEMORY SHARING
MP12708	MP12708	US	14/673,807	3/30/2015	10003551	6/19/2018	In Force	PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12708	MP12708CN	CN	2016101932888	3/30/2016			Pending	PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12708	MP12708DE	DE	10 2016 003 679.6	3/24/2016			Pending	A PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12708	MP12708HK	HK	17103793.4	3/30/2016			Pending	A PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12708	MP12708KR	KR	2016-0036000	3/25/2016			Pending	A PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12708	MP12708TW	TW	105109655	3/28/2016			Pending	PACKET MEMORY SYSTEM, METHOD AND DEVICE FOR PREVENTING UNDERRUN
MP12709	MP12709	US	14/673,813	3/30/2015	9747226	8/29/2017	In Force	PACKET PROCESSING SYSTEM, METHOD AND DEVICE TO OPTIMIZE PACKET BUFFER S
MP12709	MP12709CN	CN	201610188963.8	3/29/2016			Pending	PACKET PROCESSING SYSTEM, METHOD AND DEVICE TO OPTIMIZE PACKET BUFFER S
MP12709	MP12709HK	HK	17103792.5	3/29/2016			Pending	A PACKET PROCESSING SYSTEM, METHOD AND DEVICE TO OPTIMIZE PACKET BUFFE
MP12709	MP12709TW	TW	105109656	3/28/2016			Pending	A PACKET PROCESSING SYSTEM, METHOD AND DEVICE TO OPTIMIZE PACKET BUFFE
MP12710	MP12710	US	14/673,819	3/30/2015			Pending	PACKET PROCESSING SYSTEM, METHOD AND DEVICE HAVING REDUCED STATIC POW
MP12711	MP12711	US	14/672,874	3/30/2015	9349434	5/24/2016	In Force	VARIABLE STROBE FOR ALIGNMENT OF PARTIALLY INVISIBLE DATA SIGNALS
MP12713	MP12713	US	14/675,356	3/31/2015	9792400	10/17/2017	In Force	DETERMINATION OF FLIP-FLOP COUNT IN PHYSICAL DESIGN
MP12714	MP12714	US	14/675,710	3/31/2015	9836283	12/5/2017	In Force	COMPILER ARCHITECTURE FOR PROGRAMMABLE APPLICATION SPECIFIC INTEGRATE
MP12714	MP12714C1	US	15/804,835	11/6/2017	10466976	11/5/2019	In force	COMPILER ARCHITECTURE FOR PROGRAMMABLE APPLICATION SPECIFIC INTEGRATE
MP12715	MP12715	US	14/675,702	3/31/2015	9864584	1/9/2018	In Force	CODE GENERATOR FOR PROGRAMMABLE NETWORK DEVICES
MP12716	MP12716	US	14/675,696	3/31/2015	9870204	1/16/2018	In Force	ALGORITHM TO ACHIEVE OPTIMAL LAYOUT OF INSTRUCTION TABLES FOR PROGRA
MP12717	MP12717	US	14/675,692	3/31/2015	9864583	1/9/2018	In Force	ALGORITHM TO DERIVE LOGIC EXPRESSION TO SELECT EXECUTION BLOCKS FOR PRO
MP12718	MP12718	US	14/675,307	3/31/2015	9547733	1/17/2017	In Force	IDENTIFYING INVERSION ERROR IN LOGIC EQUIVALENCE CHECK
MP12719	MP12719	US	14/675,682	3/31/2015	9582251	2/28/2017	In Force	ALGORITHM TO ACHIEVE OPTIMAL LAYOUT OF DECISION LOGIC ELEMENTS FOR PRO
MP12720	MP12720	US	14/675,450	3/31/2015			In Force	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS
MP12720	MP12720C1	US	16/594,962	10/7/2019			Pending	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS
MP12720	MP12720CN	CN	2015102909668	5/29/2015			Pending	Method and apparatus for using multiple linked memory lists
MP12720	MP12720HK	HK	17101140.8	5/29/2015			Pending	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS
MP12720	MP12720IN	IN	1284/DEL/2015	5/7/2015			Pending	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS FOR STORI
MP12720	MP12720JP	JP	2015-170003	8/31/2015	6535253	6/7/2019	In Force	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS
MP12720	MP12720KR	KR	1020150067244	5/14/2015			Pending	METHOD AND APPARATUS FOR USING MULTIPLE LINKED MEMORY LISTS
MP12720	MP12720TW	TW	104124865.0	7/31/2015			Pending	Method and apparatus for using multiple linked memory lists
MP12721	MP12721	US	14/675,403	3/31/2015			Pending	APPROACH FOR LOGIC SIGNAL GROUPING AND RTL GENERATION USING XML
MP12722	MP12722	US	14/675,342	3/31/2015	10303626	5/28/2019	In Force	APPROACH FOR CHIP-LEVEL FLOP INSERTION AND VERIFICATION BASED ON LOGIC I
MP12723	MP12723	US	14/675,667	3/31/2015	9606781	3/28/2017	In Force	PARSER ENGINE PROGRAMMING TOOL FOR PROGRAMMABLE NETWORK DEVICES

PATENT
REEL: 057897 FRAME: 0539

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12724	MP12724	US	14/675,674	3/31/2015	9864582	1/9/2018	In Force	CODE PROCESSOR TO BUILD ORTHOGONAL EXECUTION BLOCKS FOR PROGRAMMAB
MP12725	MP12725	US	14/675,728	3/31/2015	9954551	4/24/2018	In Force	BARREL COMPACTOR SYSTEM, METHOD AND DEVICE
MP12725	MP12725C1	US	15/917,284	3/9/2018			Pending	BARREL COMPACTOR SYSTEM, METHOD AND DEVICE
MP12726	MP12726	US	14/675,734	3/31/2015	9584635	2/28/2017	In Force	BARREL COMPACTOR SYSTEM, METHOD AND DEVICE HAVING CELL COMBINATION L
MP12727	MP12727	US	14/676,679	4/1/2015	9871733	1/16/2018	In Force	POLICER ARCHITECTURE
MP12728	MP12728	US	14/673,828	3/30/2015	9606942	3/28/2017	In Force	PACKET PROCESSING SYSTEM, METHOD AND DEVICE UTILIZING A PORT CLIENT CHA
MP12728	MP12728C1	US	15/434,917	2/16/2017	10289575	5/14/2019	In Force	PACKET PROCESSING SYSTEM, METHOD AND DEVICE UTILIZING A PORT CLIENT CHA
MP12728	MP12728C1C1	US	16/370,746	3/29/2019			Pending	PACKET PROCESSING SYSTEM, METHOD AND DEVICE UTILIZING A PORT CLIENT CHA
MP12729	MP12729	US	14/678,789	4/3/2015	9509362	11/29/2016	In Force	Method and Apparatus for Handling Modified Constellation Mapping Using a Soft D
MP12730	MP12730	US	14/678,836	4/3/2015	9825799	11/21/2017	In Force	METHOD AND APPARATUS FOR DISCARDING UNUSED POINTS FROM CONSTELLATIO
MP12731	MP12731	US	14/698,581	4/28/2015	9720733	8/1/2017	In Force	METHODS AND SYSTEMS FOR CONTROL BLOCK ROUTING
MP12732	MP12732	US	15/152,164	5/11/2016	10095558	10/9/2018	In Force	SYSTEMS AND METHODS FOR OFFLOADING INLINE SSL PROCESSING TO AN EMBEDD
MP12733	MP12733	US	14/805,161	7/21/2015	9588839	3/7/2017	In Force	METHODS AND SYSTEMS FOR USING SHARED LOGIC AT NETWORK DEVICES
MP12734	MP12734	US	14/830,045	8/19/2015	10216666	2/26/2019	In Force	CACHING METHODS AND SYSTEMS USING A NETWORK INTERFACE CARD
MP12735	MP12735	US	15/246,440	8/24/2016	10250571	4/2/2019	In Force	SYSTEMS AND METHODS FOR OFFLOADING IPSEC PROCESSING TO AN EMBEDDED N
MP12736	MP12736	US	14/838,056	8/27/2015	9985887	5/29/2018	In Force	METHOD AND APPARATUS FOR PROVIDING A LOW LATENCY TRANSMISSION SYSTE
MP12736	MP12736-2	US	14/838,088	8/27/2015			Pending	Method and Apparatus For Providing A Low Latency Transmission System Using Adju
MP12736	MP127362C1	US	16/699,520	11/29/2019			Pending	Method and Apparatus For Providing A Low Latency Transmission System Using Adju
MP12736	MP12736DIV	US	15/957,566	4/19/2018			Pending	Method and Apparatus for Providing A Low Latency Transmission System Using Adap
MP12737	MP12737	US	15/248,876	8/26/2016	10425234	9/24/2019	In Force	SYSTEMS AND METHODS FOR PERFECT FORWARD SECRECY (PFS) TRAFFIC MONITORI
MP12738	MP12738	US	14/840,323	8/31/2015	10216430	2/26/2019	In Force	LOCAL ORDERING OF INSTRUCTIONS IN A COMPUTING SYSTEM
MP12738	MP12738C1	US	16/240,104	1/4/2019			Pending	LOCAL INSTRUCTION ORDERING BASED ON MEMORY DOMAINS
MP12739	MP12739	US	15/265,252	9/14/2016	10025740	7/17/2018	In Force	SYSTEMS AND METHODS FOR OFFLOADING LINK AGGREGATION TO A HOST BUS AD
MP12741	MP12741	US	14/864,323	9/24/2015	9800524	10/24/2017	In Force	SWITCHING METHODS AND SYSTEMS FOR A NETWORK INTERFACE CARD
MP12742	MP12742	US	14/874,460	10/4/2015	9753859	9/5/2017	In Force	INPUT OUTPUT VALUE PREDICTION WITH PHYSICAL OR VIRTUAL ADDRESSING FOR V
MP12743	MP12743	US	14/919,508	10/21/2015	9753852	9/5/2017	In Force	METHODS AND SYSTEMS FOR MANAGING ADDRESS LIST CONTROL BLOCKS
MP12744	MP12744	US	15/291,475	10/12/2016	10002216	6/19/2018	In Force	SYSTEMS AND METHODS FOR DYNAMIC REGRESSION TEST GENERATION USING COV
MP12745	MP12745	US	14/969,950	12/15/2015	9946671	4/17/2018	In Force	METHODS AND SYSTEMS FOR PROCESSING READ AND WRITE REQUESTS
MP12746	MP12746	US	15/000,840	1/19/2016	9673753	6/6/2017	In Force	Voltage-Controlled Oscillator With Improved Tuning Curve Linearization
MP12753	MP12753	US	15/013,139	2/2/2016	10007614	6/26/2018	In Force	METHOD AND APPARATUS FOR DETERMINING METRIC FOR SELECTIVE CACHING
MP12754	MP12754	US	15/067,139	3/10/2016	9825884	11/21/2017	In Force	PROTOCOL INDEPENDENT PROGRAMMABLE SWITCH (PIPS) SOFTWARE DEFINED DA
MP12754	MP12754C1	US	15/786,900	10/18/2017			Pending	PROTOCOL INDEPENDENT PROGRAMMABLE SWITCH (PIPS) FOR SOFTWARE DEFINE
MP12754	MP12754CN	CN	201680015083.9	9/11/2017			Pending	Protocol independent programmable switch (PIPS) for software defined data center
MP12754	MP12754DE	DE	11 2016 001 193.8	3/11/2016			Pending	Protocol-independent, programmable switch for software-defined data center netw

PATENT
REEL: 057897 FRAME: 0540

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12754	MP12754TW	TW	105107740	3/14/2016			Pending	Protocol independent programmable switch (PIPS) for software defined data center
MP12757	MP12757	US	15/088,302	4/1/2016	9779028	10/3/2017	In Force	MANAGING TRANSLATION INVALIDATION
MP12758	MP12758	US	15/088,354	4/1/2016	9772943	9/26/2017	In Force	MANAGING SYNONYMS IN VIRTUAL-ADDRESS CACHES
MP12759	MP12759	US	15/099,552	4/14/2016			Pending	METHOD AND APPARATUS FOR SHARED MULTI-PORT MEMORY ACCESS
MP12760	MP12760	US	15/136,330	4/22/2016	10235211	3/19/2019	In Force	Method And Apparatus For Dynamic Virtual System On Chip
MP12760	MP12760CN	CN	201710266560.5	4/21/2017			Pending	DISPLAY CONTROL FOR CELLULAR PHONE
MP12760	MP12760DE	DE	102017206710.1	4/20/2017			Pending	Method And Apparatus For Dynamic Virtual System On Chip
MP12760	MP12760JP	JP	2017-083643	4/20/2017			Pending	METHOD AND DEVICE FOR KINETIC VIRTUAL SYSTEM ON CHIP
MP12760	MP12760KR	KR	10-2017-0044516	4/6/2017			Pending	Method And Apparatus For Dynamic Virtual System On Chip
MP12760	MP12760TW	TW	106113271	4/20/2017			Pending	Method And Apparatus For Dynamic Virtual System On Chip
MP12761	MP12761	US	15/143,302	4/29/2016	9904305	2/27/2018	In Force	Voltage Regulator With Adaptive Bias Network
MP12762	MP12762	US	15/143,282	4/29/2016	9590797	3/7/2017	In Force	Edge Rate Control Calibration
MP12763	MP12763	US	15/582,408	4/28/2017	10409911	9/10/2019	In Force	SYSTEMS AND METHODS FOR TEXT ANALYTICS PROCESSOR
MP12766	MP12766	US	15/582,420	4/28/2017			Pending	SYSTEMS AND METHODS FOR DEEP LEARNING PROCESSOR
MP12767	MP12767	US	15/590,519	5/9/2017			Pending	SYSTEMS AND METHODS FOR VIRTIO BASED OPTIMIZATION OF DATA PACKET PATHS
MP12768	MP12768	US	15/154,994	5/14/2016			Pending	METHOD AND APPARATUS FOR EFFICIENT AND FLEXIBLE DIRECT MEMORY ACCESS
MP12769	MP12769	US	15/420,343	1/31/2017	10050624	8/14/2018	In Force	Process-Compensated Level-Up Shifter Circuit
MP12770	MP12770	US	15/159,729	5/19/2016	10027457	7/17/2018	In Force	METHODS AND APPARATUS FOR PROVIDING SOFT AND BLIND COMBINING FOR PUS
MP12770	MP12770-2	US	15/378,750	12/14/2016	10469233	11/5/2019	In force	Methods and Apparatus for Providing Soft and Blind Combining for PUSCH Acknowle
MP12770	MP12770-2C1	US	16/583,243	9/25/2019			Pending	Methods and Apparatus for Providing Soft and Blind Combining for PUSCH Acknowle
MP12771	MP12771	US	15/593,235	5/11/2017			Pending	SYSTEMS AND METHODS FOR VECTORIZED FFT FOR MULTI-DIMENSIONAL CONVOLU
MP12772	MP12772	US	15/169,466	5/31/2016	10129219	11/13/2018	In Force	METHODS AND SYSTEMS FOR SECURING DATA STORED AT A STORAGE AREA NETWO
MP12774	MP12774	US	15/193,535	6/27/2016	10223279	3/5/2019	In Force	MANAGING VIRTUAL-ADDRESS CACHES FOR MULTIPLE MEMORY PAGE SIZES
MP12775	MP12775	US	15/222,184	7/28/2016			Pending	ADMISSION CONTROL FOR MEMORY ACCESS REQUESTS
MP12776	MP12776	US	15/269,072	9/19/2016	10013357	7/3/2018	In Force	MANAGING MEMORY ACCESS REQUESTS WITH PREFETCH FOR STREAMS
MP12776	MP12776C1	US	16/011,173	6/18/2018			Pending	MANAGING MEMORY ACCESS REQUESTS WITH PREFETCH FOR STREAMS
MP12777	MP12777	US	15/272,332	9/21/2016	10210135	2/19/2019	In Force	Methods and Apparatus for Providing a Programmable Mixed-Radix DFT/IDFT Proces
MP12777	MP12777I1	US	15/292,015	10/12/2016	10311018	6/4/2019	In Force	METHODS AND APPARATUS FOR A VECTOR MEMORY SUBSYSTEM FOR USE WITH A
MP12777	MP12777I1C1	US	16/272,470	2/11/2019			Pending	Method and Apparatus for A Vector Memory Subsystem for Use with A Programmabl
MP12777	MP12777I1I1	US	15/347,663	11/9/2016	10349251	7/9/2019	In Force	Methods and Apparatus for Twiddle Factor Generation for Use with a Programmable
MP12777	MP12777I1I1C1	US	16/506,820	7/9/2019			Pending	Methods and Apparatus for Twiddle Factor Generation for Use with a Programmable
MP12779	MP12779	US	15/335,816	10/27/2016	9698808	7/4/2017	In Force	Phase Measurement And Correction Circuitry
MP12780	MP12780	US	15/363,995	11/29/2016	10275261	4/30/2019	In Force	METHODS AND SYSTEMS FOR MESSAGE LOGGING AND RETRIEVAL IN COMPUTER SY
MP12781	MP12781	US	15/379,207	12/14/2016	10140250	11/27/2018	In Force	Methods and Apparatus for Providing an FFT Engine Using a Reconfigurable Single De

PATENT
REEL: 057897 FRAME: 0541

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12783	MP12783	US	15/398,617	1/4/2017			Pending	Methods and Apparatus for Configuring a Front End to Process Multiple Sectors with
MP12786	MP12786	US	15/496,294	4/25/2017	10158353	12/18/2018	In Force	Duty Cycle Correction Method
MP12787	MP12787	US	15/498,373	4/26/2017	10171207	1/1/2019	In Force	Methods and Apparatus for Control Bit Detection
MP12788	MP12788	US	15/497,356	4/26/2017	10263759	4/16/2019	In Force	Signal Presence Detection Circuit And Method
MP12788	MP12788C1	US	16/281,822	2/21/2019			Pending	Signal Presence Detection Circuit And Method
MP12788	MP12788DE	DE	102018206379.6	4/25/2018			Pending	Signal Presence Detection Circuit And Method
MP12789	MP12789	US	15/586,867	5/4/2017	10230381	3/12/2019	In Force	Frequency Divider
MP12790	MP12790	US	15/588,015	5/5/2017	10459770	10/29/2019	In Force	METHOD AND APPARATUS FOR PORT ACCESS MANAGEMENT AT A DISTRIBUTED JOI
MP12791	MP12791	US	15/592,087	5/10/2017	10171278	1/1/2019	In Force	Methods and Apparatus for Frequency Offset Estimation
MP12791	MP12791C1	US	16/237,635	12/31/2018			Pending	Methods and Apparatus for Frequency Offset Estimation
MP12792	MP12792	US	15/594,497	6/2/2017			Pending	Methods And Apparatus For A Unified Baseband Architecture
MP12793	MP12793	US	15/595,667	5/15/2017	10423215	9/24/2019	In Force	Methods and Apparatus for Adaptive Power Profiling in a Baseband Processing Syste
MP12793	MP12793C1	US	16/546,153	8/20/2019			Pending	Methods and Apparatus for Adaptive Power Profiling in A baseband Processing Syste
MP12796	MP12796	US	15/596,860	5/16/2017	10419481	9/17/2019	In Force	METHODS AND SYSTEMS FOR OVERLAPPING PROTECTION DOMAIN IN NETWORK DE
MP12797	MP12797	US	15/600,706	5/20/2017			Pending	METHOD AND APPARATUS FOR LOAD BALANCING OF JOBS SCHEDULED FOR PROCES
MP12798	MP12798	US	15/602,774	5/23/2017	9966964	5/8/2018	In Force	Multi-Phase Divider
MP12799	MP12799	US	15/608,852	5/30/2017			Pending	FLOWLET SCHEDULER FOR MULTICORE NETWORK PROCESSORS
MP12800	MP12800	US	15/609,225	5/31/2017			Pending	MANAGING LOCK AND UNLOCK OPERATIONS USING OPERATION PREDICTION
MP12801	MP12801	US	15/609,217	5/31/2017	10445096	10/15/2019	In Force	MANAGING LOCK AND UNLOCK OPERATIONS USING TRAFFIC PRIORITIZATION
MP12801	MP12801I1	US	15/697,736	9/7/2017	10331500	6/25/2019	In Force	MANAGING FAIRNESS FOR LOCK AND UNLOCK OPERATIONS USING OPERATION PRIO
MP12802	MP12802	US	15/609,211	5/31/2017	10248420	4/2/2019	In Force	MANAGING LOCK AND UNLOCK OPERATIONS USING ACTIVE SPINNING
MP12805	MP12805	US	15/894,732	2/12/2018			Pending	TIMESTAMP-BASED PACKET SWITCHING USING A TRIE DATA STRUCTURE
MP12806	MP12806	US	15/631,085	6/23/2017	10282299	5/7/2019	In Force	MANAGING CACHE PARTITIONS BASED ON CACHE USAGE INFORMATION
MP12807	MP12807	US	15/670,841	8/7/2017	10020929	7/10/2018	In Force	METHODS AND SYSTEMS FOR DATA ALIGNMENT IN NETWORK DEVICES
MP12808	MP12808	US	15/683,376	8/22/2017			Pending	Method and Apparatus for Uplink Control Channel Detection
MP12809	MP12809	US	15/693,020	8/31/2017	10362498	7/23/2019	In Force	Method and Apparatus for Coordinated Multipoint Receiver Processing Acceleration
MP12811	MP12811	US	15/721,236	9/29/2017	10222817	3/5/2019	In Force	Method And Circuit For Low Voltage Current-Mode Bandgap
MP12811	MP12811CN	CN					Pending	Method And Circuit For Low Voltage Current-Mode Bandgap
MP12811	MP12811TW	TW	107131736	9/10/2018			Pending	Method And Circuit For Low Voltage Current-Mode Bandgap
MP12812	MP12812	US	15/716,082	9/26/2017	10389481	8/20/2019	In Force	Methods and Apparatus for Calculating Transport Block (TB) Cyclic Redundancy Chec
MP12813	MP12813	US	15/719,171	9/28/2017	10448377	10/15/2019	In Force	Methods and Apparatus for Control Channel Detection in an Uplink Shared Channel
MP12813	MP12813C1	US	16/571,164	9/15/2019			Pending	Methods and Apparatus for Control Channel Detection in an Uplink Shared Channel
MP12814	MP12814	US	15/719,973	9/29/2017	10312920	6/4/2019	In Force	Baseline Wander Compensation
MP12815	MP12815	US	15/721,334	9/29/2017	10291386	5/14/2019	In Force	Serializer/Deserializer (Serdes) Lanes with Lane-by-Lane Datarate Independence

PATENT
REEL: 057897 FRAME: 0542

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12815	MP12815C1	US	16/352,180	3/13/2019	10461917	10/29/2019	In force	Serializer/Deserializer (SerDes) Lanes with Lane-by-Lane Datarate Independence
MP12815	MP12815C1C1	US	16/569,445	9/12/2019			Pending	Serializer/Deserializer (SerDes) Lanes with Lane-by-Lane Datarate Independence
MP12815	MP12815WO	WO	PCT/US2018/05028	9/10/2018			Pending	Serializer/Deserializer (Serdes) Lanes with Lane-by-Lane Datarate Independence
MP12816	MP12816	US	15/789,420	10/20/2017			Pending	Multi-Termination Scheme Interface
MP12816	MP12816DE	DE	10 2018 217 929.8	10/19/2018			Pending	Multi-Termination Scheme Interface
MP12817	MP12817	US	15/796,645	10/27/2017			Pending	Self-Biased Current Trimmer With Digital Scaling Input
MP12818	MP12818	US	15/805,631	11/7/2017	10141949	11/27/2018	In Force	Modular Serializer And Deserializer
MP12818	MP12818DE	DE	10 2018 218 151.9	10/24/2018			Pending	Modular Serializer And Deserializer
MP12819	MP12819	US	15/825,942	11/29/2017			Pending	Method And Apparatus For Multi-Band Voltage-Controlled Oscillator (VCO) Band Se
MP12822	MP12822	US	15/875,611	1/19/2018			Pending	ISSUING INSTRUCTIONS BASED ON RESOURCE CONFLICT CONSTRAINTS IN MICROPO
MP12824	MP12824DE	DE	102019200599.3	1/17/2019			Pending	MANAGING BRANCH PREDICTION INFORMATION FOR DIFFERENT CONTEXTS
MP12826	MP12826	US	15/934,804	3/23/2018			Pending	EXTERNAL DQS BI-DIRECTIONAL LOOPBACK WITH USE OF FEED FORWARD EQUALIZA
MP12840	MP12840	US	16/009,826	6/15/2018			Pending	Combined Conditional Branch and Indirect Branch Target Predictor
MP12842	MP12842	US	16/209,739	12/4/2018			Pending	Complex I/O Value Prediction for Multiple Values with Physical or Virtual Addresses
MP12843	MP12843	US	16/029,031	7/6/2018			Pending	Limiting Backpressure With Bad Actors
MP12844	MP12844	US	16/029,184	7/6/2018			Pending	Method To Limit Packet Fetching With Uncertain Packet Sizes To Control Line Rate
MP12845	MP12845KR	KR	10-2019-0145935	11/14/2019			Pending	Transmitter Tuning Using Receiver Gradient
MP12847	MP12847	US	16/696,789	11/26/2019			Pending	System and Method For Performing a Failure Assessment of an Integrated Circuit
MP12847	MP12847PR	US	62/771,466	11/26/2018			Pending	System and Method For Performing a Failure Assessment of an Integrated Circuit
MP12848	MP12848PR	US	62/778,386	12/12/2018			Pending	Traversing A Variable Delay Line In A Deterministic Number Of Clock Cycles
MP12851	MP12851PR	US	62/778,375	12/12/2018			Pending	Droop Detection and Mitigation
MP12853	MP12853	US	16/039,922	7/19/2018	10418125	9/17/2019	In Force	WRITE AND READ COMMON LEVELING FOR 4-BIT WIDE DRAMS
MP12853	MP12853C1	US	16/536,183	8/8/2019			Pending	WRITE AND READ COMMON LEVELING FOR 4-BIT WIDE DRAMS
MP12854	MP12854CN	CN	201910691268.7	7/29/2019			Pending	Preventing Information Leakage In Out-Of-Order Machines Due To Misspeculation
MP12855	MP12855	US	16/589,527	10/1/2019			Pending	MERGE EXECUTION UNIT FOR MICROINSTRUCTIONS
MP12857	MP12857	US	16/264,458	1/31/2019			Pending	PAIR MERGE EXECUTION UNITS FOR MICROINSTRUCTIONS
MP12858	MP12858	US	16/054,627	8/3/2018			Pending	VOQ-BASED NETWORK SWITCH ARCHITECTURE USING MULTI-STAGE ARBITRATION F
MP12862	MP12862	US	16/115,117	8/28/2018			Pending	COMPRESSING LIKE MAGNITUDE PARTIAL PRODUCTS IN MULTIPLY ACCUMULATION
MP12863	MP12863	US	16/568,698	9/12/2019			Pending	METHOD OF IMPROVING L1 ICACHE PERFORMANCE WITH LARGE PROGRAMS
MP12864	MP12864	US	16/128,369	9/11/2018			Pending	METHODS AND SYSTEMS FOR DISTRIBUTING MEMORY REQUESTS
MP12866	MP12866	US	16/129,107	9/12/2018			Pending	Low Latency Interconnect Protocol for Coherent Multi-Chip Communication
MP12867	MP12867	US	16/189,119	11/13/2018			Pending	FLEXIBLE RESOURCE ASSIGNMENT TO PHYSICAL AND VIRTUAL FUNCTIONS IN A VIRT
MP12868	MP12868	US	16/199,852	11/26/2018			Pending	PREFETCHING DATA TO REDUCE CACHE MISSES
MP12869	MP12869	US	16/199,936	11/26/2018			Pending	INCREASING THE LOOKAHEAD AMOUNT FOR PREFETCHING

PATENT
REEL: 057897 FRAME: 0543

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	Status	Title
MP12872	MP12872	US	16/142,698	9/26/2018			Pending	Secure Low-latency Chip-to-Chip Communication
MP12873	MP12873CN	CN	201910913261.5	9/25/2019			Pending	Secure In-line Received Network Packet Processing
MP12874	MP12874CN	CN	201910913894.6	9/25/2019			Pending	Secure In-line Network Packet Transmittal
MP12876	MP12876	US	15/419,942	1/30/2017	10218643	2/26/2019	In Force	APPARATUS AND METHOD FOR SCALABLE AND FLEXIBLE ACCESS CONTROL LIST LOO
MP12877	MP12877	US	14/540,868	11/13/2014	9485179	11/1/2016	In Force	APPARATUS AND METHOD FOR SCALABLE AND FLEXIBLE TABLE SEARCH IN A NETWO
MP12877	MP12877TW	TW	104104344	2/10/2015			Pending	APPARATUS AND METHOD FOR SCALABLE AND FLEXIBLE TABLE SEARCH IN A NETWO
MP12878	MP12878	US	14/540,927	11/13/2014	9553829	1/24/2017	In Force	APPARATUS AND METHOD FOR FAST SEARCH TABLE UPDATE IN A NETWORK SWITC
MP12878	MP12878TW	TW	104104960	2/10/2015	I632792	8/11/2018	In Force	APPARATUS AND METHOD FOR FAST SEARCH TABLE UPDATE IN A NETWORK SWITC
MP12879	MP12879	US	14/617,644	2/9/2015	9571395	2/14/2017	In Force	RECONFIGURABLE INTERCONNECT ELEMENT WITH LOCAL LOOKUP TABLES SHARED
MP12879	MP12879TW	TW	104110649	4/1/2015	I629887	7/11/2018	In Force	RECONFIGURABLE INTERCONNECT ELEMENT WITH LOCAL LOOKUP TABLES SHARED
MP12880	MP12880	US	14/628,058	2/20/2015	10003676	6/19/2018	In Force	METHOD AND APPARATUS FOR GENERATING PARALLEL LOOKUP REQUESTS UTILIZIN
MP12880	MP12880TW	TW	104110834	4/2/2015	I665894	7/11/2019	In Force	METHOD AND APPARATUS FOR GENERATING PARALLEL LOOKUP REQUESTS UTILIZIN
MP12881	MP12881	US	14/632,709	2/26/2015	10430472	10/1/2019	In Force	APPARATUS AND METHOD FOR COLLECTING RESPONSES TO A PLURALITY OF PARALL
MP12881	MP12881TW	TW	104110654	4/1/2015	I665888	7/11/2019	In Force	APPARATUS AND METHOD FOR COLLECTING RESPONSES TO A PLURALITY OF PARALL
MP12882	MP12882	US	14/675,246	3/31/2015	9553819	1/24/2017	In Force	SYSTEMS AND METHODS FOR TIMING ADJUSTMENT OF METADATA PATHS IN A NET
MP12883	MP12883	US	14/657,921	3/13/2015	10001999	6/19/2018	In Force	SYSTEM AND METHOD FOR CONFIGURING A PLURALITY OF REGISTERS WITH SOFT E
MP12883	MP12883TW	TW	104110651	4/1/2015	I656474	4/11/2019	In Force	SYSTEM AND METHOD FOR CONFIGURING A PLURALITY OF REGISTERS WITH SOFT E
MP12884	MP12884	US	14/806,894	7/23/2015	9916274	3/13/2018	In Force	APPARATUS AND METHOD FOR ON-CHIP CROSSBAR DESIGN IN A NETWORK SWITCH
MP12885	MP12885	US	14/850,873	9/10/2015	9823960	11/21/2017	In Force	APPARATUS AND METHOD FOR PARALLEL CRC UNITS FOR VARIABLY-SIZED DATA FRA
MP12887	MP12887	US	15/047,987	2/19/2016	9870173	1/16/2018	In Force	APPARATUS AND METHOD FOR OPTIMIZED N-WRITE/1-READ PORT MEMORY DESIG
MP12888	MP12888	US	15/140,394	4/27/2016	9948482	4/17/2018	In Force	APPARATUS AND METHOD FOR ENABLING FLEXIBLE KEY IN A NETWORK SWITCH
MP12891	MP12891	US	15/419,962	1/30/2017	10091137	10/2/2018	In Force	APPARATUS AND METHOD FOR SCALABLE AND FLEXIBLE WILDCARD MATCHING IN A
MP12897	MP12897	US	15/613,889	6/5/2017			Pending	PROGRAMMABLE HARDWARE SCHEDULER FOR DIGITAL PROCESSING SYSTEMS
MP12898	MP12898	US	15/613,760	6/5/2017			Pending	METHOD AND APPARATUS FOR SCHEDULING ARBITRATION AMONG A PLURALITY OF
MP12900	MP12900	US	15/588,240	5/5/2017			Pending	METHOD AND APPARATUS FOR JOB PRE-SCHEDULING BY DISTRIBUTED JOB MANAG
MP12901	MP12901	US	15/602,620	5/23/2017			Pending	RE-ORDERING BUFFER FOR A DIGITAL MULTI-PROCESSOR SYSTEM WITH CONFIGURA
MP12907	MP12907	US	16/040,249	7/19/2018	10497413	12/3/2019	In force	WRITE AND READ COMMON LEVELING FOR 4-BIT WIDE DRAMS
MP12908	MP12908	US	14/279,712	5/16/2014	9501245	11/22/2016	In Force	SYSTEMS AND METHODS FOR NVME CONTROLLER VIRTUALIZATION TO SUPPORT M
MP12908	MP12908TW	TW	104107519	3/10/2015	I625674	6/1/2018	In Force	SYSTEMS AND METHODS FOR NVME CONTROLLER VIRTUALIZATION TO SUPPORT M
MP12915	MP12915	US	14/542,393	11/14/2014	10447608	10/15/2019	In Force	PACKET SCHEDULING USING HIERARCHICAL SCHEDULING PROCESS WITH PRIORITY P
MP12921	MP12921	US	13/184,199	7/15/2011	8843764	9/23/2014	In Force	Secure Software And Hardware Association Technique
MP12921	MP12921C1	US	14/340,225	7/24/2014	9602282	3/21/2017	In Force	Secure Software And Hardware Association Technique
MP5523	MP5523WOEP	DE	14802261.9	10/30/2014	3066785	12/4/2019	In Force	Managing Idle Mode of Operation in Network Switches

PATENT
REEL: 057897 FRAME: 0544

Exhibit B - 2C CAVIUM LLC TO CI Group B

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP0315	MP0315	US	10/667,197					
MP0375	MP0375D1	US	11/751,593	5/21/2007	7640370	12/29/2009	In Force	METHOD AND APPARATUS FOR CONTROLLING DATA TRANSFER BET
MP0375	MP0375D1C1	US	12/616,111	11/10/2009	8856391	10/7/2014	In Force	METHOD AND APPARATUS FOR CONTROLLING DATA TRANSFER BET
MP0452	MP0452	US	10/795,727					
MP0479	MP0479	US	10/801,197					
MP10226	MP10226PR	US	62/802,113	2/6/2019			Pending	Method and Apparatus for Extendable Hardware Queues
MP10289	MP10289PR	US	62/767,753	11/15/2018			Pending	LOW-POWER SERIALIZER WITH HALF-RATE CLOCKING FOR SERIAL C
MP10295	MP10295C1	US	0				Not Filed	Modular Memory-Like Layout For FinFET Analog Designs
MP10326	MP10326	US	16/049,732	7/30/2018			Pending	WAKEUP RADIO (WUR) PACKET PREAMBLE DESIGN
MP10383	MP10383C1	US	16/702,628	12/4/2019			Pending	Ethernet Transceiver with PHY-Level Signal-Loss Detector
MP10400	MP10400C1	US	0				Not Filed	TWO DIMENSIONAL MAGNETIC RECORDING (TDMR) OFF-TRACK PER
MP10473	MP10473	US	16/690,803	11/21/2019			Pending	SERIAL MANAGEMENT INTERFACE WITH IMPROVED RELIABILITY
MP10473	MP10473PR	US	62/770,537	11/21/2018			Pending	Reliable SMI Access
MP10482	MP10482PR	US	62/771,879	11/27/2018			Pending	Latency optimization using a Smart Samplers Placement
MP10493	MP10493PR	US	62/814,165	3/5/2019			Pending	Flash Controller
MP10494	MP10494	US	16/583,541	9/26/2019			Pending	POLYGONAL BGA SEMICONDUCTOR PACKAGE
MP10494	MP10494C1	US	0				Not Filed	POLYGONAL BGA SEMICONDUCTOR PACKAGE
MP10496	MP10496	US	16/406,898	5/8/2019			Pending	WIFI BACKOFF TIMER
MP10499	MP10499	US	16/566,378	9/10/2019			Pending	METHOD AND APPARATUS FOR TRANSMITTING SIGNALS OVER LON
MP10500	MP10500	US	16/583,639	9/26/2019			Pending	METHOD AND APPARATUS FOR TESTING A MULTI-DIE INTEGRATED
MP10507	MP10507PR	US	62/770,047	11/20/2018			Pending	SELECT BANDWIDTH - REDUCE EMPTY Q NULL SELECT
MP10508	MP10508PR	US	62/771,890	11/27/2018			Pending	Effective Guaranteed Message Buffering
MP1066	MP1066PR	US	60/794,956					
MP11011	MP11011	US	16/525,105	7/29/2019			Pending	CONTROLLING PERFORMANCE OF A SOLID STATE DRIVE
MP11016	MP11016PR	US	62/790,701	1/10/2019			Pending	EFFICIENT FREQUENCY DOMAIN IMPLEMENTATION FOR FEED FOR
MP11022	MP11022	US	16/526,932	7/30/2019			Pending	Shared Memory Block Configuration
MP11039	MP11039	US	16/560,816	9/4/2019			Pending	CONFIGURABLE HASH-BASED LOOKUP IN NETWORK DEVICES
MP11045	MP11045PR	US	62/790,708	1/10/2019			Pending	ARCHITECTURE FOR SUPPORTING MULTI-SPEED AND MULTI-PORT P
MP11059	MP11059PR	US	62/836,536	4/19/2019			Pending	OPERATIONS AND MANAGEMENT (OAM) IN ETHERNET NETWORKS
MP11081	MP11081	US	16/697,361	11/27/2019			Pending	NETWORK SWITCH WITH ENDPOINT AND DIRECT MEMORY ACCESS
MP11081	MP11081PR	US	62/772,506	11/28/2018			Pending	PCIE SWITCH CONCEPT FOR AUTOMOTIVE APPLICATIONS
MP11081	MP11081WO	WO	PCT/US2019/063	11/27/2019			Pending	NETWORK SWITCH WITH ENDPOINT AND DIRECT MEMORY ACCESS

PATENT
REEL: 057897 FRAME: 0545

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP11089	MP11089WO	WO	PCT/US2019/059	10/31/2019			Pending	PADDING FOR WAKEUP RADIO (WUR) PACKETS
MP11090	MP11090WO	WO	PCT/IB2019/059	10/26/2019			Pending	Artificial Intelligence-Enabled Management of Storage Media Access
MP11096	MP11096KR	KR	0	10/30/2019			Not Filed	Thermal Compensation for Laser in Heat Assisted Magnetic Recordin
MP11096	MP11096TW	TW	108139298	10/30/2019			Pending	Thermal Compensation for Laser in Heat Assisted Magnetic Recordin
MP11096	MP11096WO	WO	PCT/US2019/058	10/29/2019			Pending	Thermal Compensation for Laser in Heat Assisted Magnetic Recordin
MP11102	MP11102PR	US	62/808,053	2/20/2019			Pending	High density fractional bit Solid State Drives using coded set partitio
MP11103	MP11103PR	US	62/808,072	2/20/2019			Pending	High density packing of memory cells and diversity gain extraction in
MP11104	MP11104	US	0				Not Filed	Secure WiFi
MP11105	MP11105PR	US	62/778,602	12/12/2018			Pending	Sector based association of STA with AP
MP11108	MP11108PR	US	62/767,999	11/15/2018			Pending	Feedforward IQ Imbalance Correction
MP11113	MP11113	US	0				Not Filed	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11113	MP11113CN	CN	0				Not Filed	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11113	MP11113EP	EP	0				Not Filed	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11113	MP11113KR	KR	0				Not Filed	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11113	MP11113PR	US	62/791,542	1/11/2019			Pending	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11113	MP11113TW	TW	0				Not Filed	Method of Using RAID to Recover Data Upon a Program Status Failur
MP11119	MP11119PR	US	62/791,553	1/11/2019			Pending	Wide Input Common-Mode Folded-Cascode Amplifier with Adaptive
MP11120	MP11120CN	CN	201911136433.9	11/19/2019			Pending	HYBRID ARQ WITH VARYING MODULATION AND CODING
MP11120	MP11120EP	EP	19209668.3	11/18/2019			Pending	HYBRID ARQ WITH VARYING MODULATION AND CODING
MP11120	MP11120PR	US	62/770,082	11/20/2018			Pending	Hybrid ARQ (HARQ) for link adaptation in WLAN
MP11122	MP11122PR	US	62/771,901	11/27/2018			Pending	Fully Flexible Assignment of Interrupt Requests in a Multifunction PC
MP11123	MP11123PR	US	62/775,210	12/4/2018			Pending	EHT Packet Format Designs: DCM Signaling
MP11124	MP11124PR	US	62/775,232	12/4/2018			Pending	EHT Packet Format Designs: Masking & CRC generation
MP11125	MP11125	US	16/703,694	12/4/2019			Pending	Reducing Offset of a Differential Signal Output by a Capacitive Coupli
MP11125	MP11125PR	US	62/775,781	12/5/2018			Pending	Circuits and methods for reducing dynamic offset of capacitive coupl
MP11125	MP11125SG	SG	10201911728V	12/5/2019			Pending	Reducing Offset of a Differential Signal Output by a Capacitive Coupli
MP11127	MP11127	US	16/702,983	12/4/2019			Pending	Balanced Current Mirrors for Biasing a Magnetic Resistor in a Hard D
MP11127	MP11127PR	US	62/775,795	12/5/2018			Pending	Speed-balanced current mirror for magnetic resistor bias in HDD pre
MP11128	MP11128PR	US	62/770,086	11/20/2018			Pending	DIFFERENT ENCODING/SIGNALING SCHEMES FOR A SEQUENCE OF D
MP11128	MP11128WO	WO	PCT/IB2019/059	11/19/2019			Pending	SIGNALING OF ENCODING SCHEMES IN PACKETS TRANSMITTED OVE
MP11131	MP11131CN	CN	0				Not Filed	METHOD TO TRANSMIT DATA TO PREAMP THROUGH DIFFERENTIAL
MP11131	MP11131EP	EP	0				Not Filed	METHOD TO TRANSMIT DATA TO PREAMP THROUGH DIFFERENTIAL
MP11131	MP11131KR	KR	0				Not Filed	METHOD TO TRANSMIT DATA TO PREAMP THROUGH DIFFERENTIAL
MP11131	MP11131PR	US	62/783,041	12/20/2018			Pending	METHOD TO TRANSMIT DATA TO PREAMP THROUGH DIFFERENTIAL

PATENT
REEL: 057897 FRAME: 0546

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP11132	MP11132PR	US	62/771,920	11/27/2018			Pending	Plastic mm-wave Waveguide with Plastic Foam as insulator
MP11133	MP11133PR	US	62/808,647	2/21/2019			Pending	Distributed Multiple Input Multiple Output (DMIMO) at MAC Layer
MP11134	MP11134PR	US	62/808,703	2/21/2019			Pending	Dual use of solar cell as memory cell
MP11138	MP11138PR	US	62/780,088	12/14/2018			Pending	WiFi 11ax UL MULTI-USER MULTIPLE INPUT MULTIPLE OUTPUT (MU
MP11139	MP11139PR	US	62/768,007	11/15/2018			Pending	General Error Reporting and Handling
MP11142	MP11142PR	US	62/799,598	1/31/2019			Pending	REDUCED SECURITY RISK OF AUTHENTICATION BETWEEN THE HOST
MP11143	MP11143PR	US	62/782,200	12/19/2018			Pending	Breathing Rate Detection System Using WiFi Signals
MP11144	MP11144CN	CN	0				Not Filed	ZONE SERVO SELF SERVO WRITE (SSW) WITH ZONED SPIRAL SERVO
MP11144	MP11144EP	EP	0				Not Filed	ZONE SERVO SELF SERVO WRITE (SSW) WITH ZONED SPIRAL SERVO
MP11144	MP11144KR	KR	0				Not Filed	ZONE SERVO SELF SERVO WRITE (SSW) WITH ZONED SPIRAL SERVO
MP11144	MP11144PR	US	62/782,211	12/19/2018			Pending	ZONE SERVO SELF SERVO WRITE (SSW) WITH ZONED SPIRAL SERVO
MP11144	MP11144TW	TW	0				Not Filed	ZONE SERVO SELF SERVO WRITE (SSW) WITH ZONED SPIRAL SERVO
MP11146	MP11146PR	US	62/803,204	2/8/2019			Pending	Exposed-die Heat-Sink design
MP11148	MP11148	US	0				Not Filed	Drive Health Management
MP11148	MP11148CN	CN	0				Not Filed	Drive Health Management
MP11148	MP11148EP	EP	0				Not Filed	Drive Health Management
MP11148	MP11148KR	KR	0				Not Filed	Drive Health Management
MP11148	MP11148PR	US	62/799,608	1/31/2019			Pending	Drive Health Management
MP11148	MP11148TW	TW	0				Not Filed	Drive Health Management
MP11150	MP11150PR	US	62/808,740	2/21/2019			Pending	BASIC SERVICE SET (BSS) INFORMATION BROADCAST FOR ASSOCIATI
MP11151	MP11151PR	US	62/777,653	12/10/2018			Pending	PROTECTION ON MULTI-MASTER ACCESS TO THE SHARED RESOURC
MP11152	MP11152PR	US	62/808,743	2/21/2019			Pending	6 GHz BAND CHANNELIZATION
MP11153	MP11153PR	US	62/790,716	1/10/2019			Pending	Automatically track analog front end response by digital method in c
MP11154	MP11154PR	US	62/783,052	12/20/2018			Pending	SHORT PREAMBLE DETECTION AND DOWNSHIFT
MP11155	MP11155PR	US	62/777,659	12/10/2018			Pending	BLOCKCHAIN BASED DECOMMISSIONING HDD/SSDs IN DATA CENTE
MP11155	MP11155PR2	US	62/829,537	4/4/2019			Pending	SELF-ENCRYPTION DRIVE (SED) ARCHITECTURE FOR DATA CENTER
MP11157	MP11157PR	US	62/808,750	2/21/2019			Pending	Method and apparatus to control and observe analog I/Os for testab
MP11158	MP11158PR	US	62/782,221	12/19/2018			Pending	PLACE & ROUTE BLOCKS PORTS LOCATION FOR REUSE
MP11159	MP11159	US	0				Not Filed	SOLID-STATE DRIVE WITH INITIATOR MODE
MP11159	MP111592	US	0				Not Filed	NVMe-oF Termination at the Drive Level
MP11159	MP111592CN	CN	0				Not Filed	NVMe-oF Termination at the Drive Level
MP11159	MP111592EP	EP	0				Not Filed	NVMe-oF Termination at the Drive Level
MP11159	MP111592KR	KR	0				Not Filed	NVMe-oF Termination at the Drive Level
MP11159	MP111592TW	TW	0				Not Filed	NVMe-oF Termination at the Drive Level

PATENT
REEL: 057897 FRAME: 0547

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP11159	MP11159CN	CN	0				Not Filed	SOLID-STATE DRIVE (SSD) INITIATOR MODE
MP11159	MP11159EP	EP	0				Not Filed	SOLID-STATE DRIVE (SSD) INITIATOR MODE
MP11159	MP11159KR	KR	0				Not Filed	SOLID-STATE DRIVE (SSD) INITIATOR MODE
MP11159	MP11159PR	US	62/783,060	12/20/2018			Pending	SOLID-STATE DRIVE (SSD) INITIATOR MODE
MP11159	MP11159PR2	US	62/818,557	3/14/2019			Pending	NVMe-oF Termination at the Drive Level
MP11159	MP11159TW	TW	0				Not Filed	SOLID-STATE DRIVE (SSD) INITIATOR MODE
MP11160	MP11160PR	US	62/850,970	5/21/2019			Pending	Open Loop Feed-Forward Adaptive Bias Power Amplifier
MP11162	MP11162PR	US	62/798,231	1/29/2019			Pending	REDUCED AREA LOW LATENCY LATCH FIRST-IN FIRST OUT (FIFO)
MP11162	MP11162PR2	US	62/821,316	3/20/2019			Pending	REDUCED AREA LOW LATENCY LATCH FIRST-IN FIRST OUT (FIFO)
MP11163	MP11163CN	CN	0				Not Filed	forward timestamping
MP11163	MP11163PR	US	62/802,121	2/6/2019			Pending	forward timestamping
MP11165	MP11165PR	US	62/790,724	1/10/2019			Pending	HYBRID TERNARY CONTENT-ADDRESSABLE MEMORY (TCAM) EXACT
MP11167	MP11167PR	US	62/802,126	2/6/2019			Pending	USXGMII PCH SUPPORT
MP11169	MP11169PR	US	62/798,240	1/29/2019			Pending	PROGRAMMABLE HEADER ALTERATION
MP11170	MP11170PR	US	62/791,559	1/11/2019			Pending	LINK LIST CONTROLLER UNIT
MP11173	MP11173PR	US	62/821,813	3/21/2019			Pending	Fast Dynamic Frequency Scaling Phase Locked Loop (PLL) with Wide
MP11174	MP11174PR	US	62/823,497	3/25/2019			Pending	NEW PILOT DESIGN FOR NEXT GENERATION V2X (NGV)
MP11175	MP11175PR	US	62/831,596	4/9/2019			Pending	BASIC SERVICE SET (BSS) WITH MULTIPLE CHANNEL SEGMENTS OR >
MP11175	MP11175PR2	US	62/845,749	5/9/2019			Pending	NEXT GENERATION WIRELESS 20MHz OPERATION
MP11178	MP11178PR	US	62/821,135	3/20/2019			Pending	Continuous time amplitude stabilization loop for crystal oscillators
MP11180	MP11180PR	US	62/803,220	2/8/2019			Pending	PACKET ACCUMULATOR
MP11182	MP11182PR	US	62/803,234	2/8/2019			Pending	Operational User Privilege Decrease For Non-Compliant Users
MP11183	MP11183PR2	US	62/938,836	11/21/2019			Pending	FLOW ANALYSIS AND MANAGEMENT
MP11185	MP11185PR	US	62/810,215	2/25/2019			Pending	METHOD AND APPARATUS USING A LOGIC ANALYZER TO DEBUG AN
MP11186	MP11186PR	US	62/810,227	2/25/2019			Pending	METHOD AND APPARATUS FOR ACCELERATING MEMORY ACCESS
MP11187	MP11187PR	US	62/810,871	2/26/2019			Pending	Mapping cache method combining software and hardware
MP12022	MP12022WO	US	12/235,210	9/22/2008	7822055	10/26/2010	In Force	FIBRE CHANNEL CREDIT EXTENDER AND REPEATER
MP12024	MP12024	US	10/310,653	12/5/2002	7248580	7/24/2007	In Force	HARDWARE-ENFORCED LOOP-LEVEL HARD ZONING FOR FIBRE CHA
MP12123	MP12123PR	US	60/609,910					
MP12157	MP12157PR	US	60/669,655					
MP12186	MP12186	US	11/376,886					
MP12211	MP12211WO	KR	10-2008-700597	12/20/2006			Pending	METHOD AND DECODER FOR TAIL-BITING DECODING
MP12220	MP12220WO	KR	10-2008-700554	3/5/2007	1.00924061e+12	10/21/2009	In Force	CHANNEL PROFILER AND METHOD OF PROFILING AN INCOMING SIG
MP12225	MP12225WO	KR	10-2008-700553	5/2/2007	100973935	8/3/2010	In Force	METHOD AND APPARATUS FOR CORRECTING LINEAR ERROR PHASE

PATENT
REEL: 057897 FRAME: 0548

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP12237	MP12237	US	11/874,752					
MP12244	MP12244	US	11/949,755	12/3/2007	8555260	10/8/2013	In Force	DIRECT HARDWARE PROCESSING OF INTERNAL DATA STRUCTURE FI
MP12249	MP12249WOI	IL	207299	1/29/2008			Pending	SIGNAL PROCESSING UNIT AND METHOD AND CORRESPONDING TR
MP12256	MP12256WO	WO	PCT/CA2008/000	4/17/2008	DNA		Pending	SYSTEM AND METHOD FOR OPTIMIZING USE OF CHANNEL STATE IN
MP12263	MP12263	US	12/176,750	7/21/2008	8619558	12/31/2013	In Force	MEMORY MANAGEMENT IN A NETWORK ADAPTER
MP12300	MP12300PR	US	61/224,570					
MP12317	MP12317PR	US	61/330,803					
MP12322	MP12322C1	US	12/822,583					
MP12329	MP12329C1	US	12/881,402					
MP12340	MP12340C1	US	12/974,431					
MP12342	MP12342C1	US	13/012,711					
MP12400	MP12400PR	US	61/589,181					
MP12404	MP12404PR4	US	61/714,597					
MP12404	MP12404PR5	US	61/714,600					
MP12785	MP12785	US	15/455,070	3/9/2017	10402201	9/3/2019	In Force	Method and Apparatus for Detecting Memory Conflicts Using Disting
MP12794	MP12794	US	15/722,986	10/2/2017			Pending	METHOD AND APPARATUS FOR CACHE PRE-FETCH WITH OFFSET DIR
MP12803	MP12803	US	16/186,313	11/9/2018			Pending	SYSTEMS AND METHODS FOR PROGRAMMABLE HARDWARE ARCHIT
MP12803	MP12803-2	US	16/226,508	12/19/2018			Pending	SINGLE INSTRUCTION SET ARCHITECTURE (ISA) FORMAT FOR MULTI
MP12803	MP12803-3	US	16/226,534	12/19/2018			Pending	STREAMING ENGINE FOR MACHINE LEARNING ARCHITECTURE
MP12803	MP12803-4	US	16/226,539	12/19/2018			Pending	ARRAY-BASED INFERENCE ENGINE FOR MACHINE LEARNING
MP12803	MP12803-5	US	16/226,550	12/19/2018			Pending	ARCHITECTURE FOR DENSE OPERATIONS IN MACHINE LEARNING INF
MP12803	MP12803-6	US	16/226,559	12/19/2018			Pending	ARCHITECTURE FOR IRREGULAR OPERATIONS IN MACHINE LEARNIN
MP12803	MP12803-7	US	16/226,564	12/19/2018			Pending	ARCHITECTURE OF CROSSBAR OF INFERENCE ENGINE
MP12827	MP12827	US	16/224,601	12/18/2018			Pending	SYSTEM AND METHOD FOR DROOP DETECTION
MP12828	MP12828	US	16/224,638	12/18/2018			Pending	SYSTEM AND METHOD FOR COMPENSATING FOR A DROOP EVENT
MP12828	MP12828-2	US	16/224,638	12/18/2018			Pending	SYSTEM AND METHOD FOR COMPENSATING FOR A DROOP EVENT
MP12829	MP12829	US	16/173,877	10/29/2018			Pending	METHODS AND APPARATUS FOR JOB SCHEDULING IN A PROGRAMM
MP12831	MP12831	US	16/148,796	10/1/2018			Pending	METHODS AND APPARATUS FOR DYNAMIC ACKNOWLEDGEMENT LI
MP12832	MP12832	US	16/384,878	4/15/2019			Pending	METHODS AND APPARATUS FOR TWO-STAGE ACK/DTX DETECTION
MP12834	MP12834	US	16/400,992	5/1/2019			Pending	Methods and Apparatus for Symbol-to-Symbol Multiplexing of Contr
MP12835	MP12835	US	16/236,455	12/29/2018			Pending	METHODS AND APPARATUS FOR SUB-BLOCK BASED ARCHITECTURE
MP12836	MP12836	US	16/404,029	5/6/2019			Pending	Methods and Apparatus for Providing A Demapping System to Dema
MP12837	MP12837	US	16/421,917	5/24/2019			Pending	METHODS AND APPARATUS FOR PROVIDING A RESOURCE ELEMENT
MP12838	MP12838	US	16/427,069	5/30/2019			Pending	METHODS AND APPARATUS FOR DESCRAMBLING RECEIVED UPLINK

PATENT
REEL: 057897 FRAME: 0549

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP12839	MP12839	US	16/434,057	6/6/2019			Pending	METHODS AND APPARATUS FOR COMBINING RECEIVED UPLINK TRA
MP12841	MP12841	US	16/457,863	6/28/2019			Pending	METHODS AND APPARATUS FOR DECODING RECEIVED UPLINK TRAN
MP12899	MP12899	US	15/595,308	5/15/2017	10402228	9/3/2019	In Force	Method and Apparatus for Assigning Processing Work in Parallel Co
MP12899	MP12899D1	US	16/518,892	7/22/2019			Pending	Apparatus for Assigning Processing Work in Parallel Computing
MP12924	MP12924	US	16/110,957	8/23/2018			Pending	Methods And Apparatus For Simultaneous Multiprotocol Processing
MP12930	MP12930	US	16/566,015	9/10/2019			Pending	METHOD OF CACHE PREFETCHING THAT INCREASES THE HIT RATE O
MP12933	MP12933PR	US	62/841,202	4/30/2019			Pending	Method and Apparatus for Compressing Incoming Data Stream Usin
MP12934	MP12934PR	US	62/841,207	4/30/2019			Pending	Method and Apparatus for Compressing Incoming Data Stream via P
MP12935	MP12935CN	CN	0				Not Filed	Discovery of Codeword Decoding Order in SIC Receiver Using Reinfo
MP12935	MP12935PR	US	62/843,419	5/4/2019			Pending	Methods and Apparatus for Discovering Codeword Decoding Order i
MP12936	MP12936CN	CN	0				Not Filed	Methods and Apparatus for Providing an Adaptive Beam-Forming An
MP12936	MP12936DE	DE	0				Not Filed	Methods and Apparatus for Providing an Adaptive Beam-Forming An
MP12936	MP12936JP	JP	0				Not Filed	Methods and Apparatus for Providing an Adaptive Beam-Forming An
MP12936	MP12936KR	KR	0				Not Filed	Methods and Apparatus for Providing an Adaptive Beam-Forming An
MP12936	MP12936PR	US	62/846,661	5/11/2019			Pending	Methods and Apparatus for Providing an Adaptive Beam-Forming An
MP12937	MP12937I1	US	16/419,994	5/22/2019			Pending	ARCHITECTURE TO SUPPORT TANH AND SIGMOID OPERATIONS FOR
MP12938	MP12938I1	US	16/420,028	5/22/2019			Pending	ARCHITECTURE FOR TABLE-BASED MATHMATICAL OPERATIONS FOR
MP12939	MP12939I1	US	16/420,103	5/22/2019			Pending	DATA TRANSMISSION BETWEEN MEMORY AND ON CHIP MEMORY
MP12940	MP12940I1	US	16/420,055	5/22/2019			Pending	ARCHITECTURE TO SUPPORT COLOR SCHEME-BASED SYNCHRONIZA
MP12941	MP12941I1	US	16/420,078	5/22/2019			Pending	ADDRESS INTERLEAVING FOR MACHINE LEARNING
MP12942	MP12942I1	US	16/420,092	5/22/2019			Pending	ARCHITECTURE TO SUPPORT SYNCHRONIZATION BETWEEN CORE A
MP13000	MP13000PR	US	62/850,988	5/21/2019			Pending	SLEEP TIME COMPUTATION IN IEEE PS MODE
MP13001	MP13001PR	US	62/868,341	6/28/2019			Pending	Methods and Apparatus for Signal Bandwidth detection in WiFi Syste
MP13002	MP13002PR	US	62/837,093	4/22/2019			Pending	BLIND EQUALIZER SIGN ERROR LAST MEAN SQUARES (LMS) ALGORIT
MP13003	MP13003PR	US	62/850,998	5/21/2019			Pending	Accelerate Key Access
MP13004	MP13004PR	US	62/816,747	3/11/2019			Pending	METHODS OF PORTING SYSTEM LEVEL TEST TO AUTOMATED TEST E
MP13006	MP13006PR	US	62/852,580	5/24/2019			Pending	P-N TRANSISTORS SPEED CHARACTERIZATION-METHOD AND IMPLE
MP13007	MP13007PR	US	62/837,100	4/22/2019			Pending	Send-S 2D Detector For AutoPHY 1000BASE-T1
MP13008	MP13008PR	US	62/816,759	3/11/2019			Pending	SOLID-STATE DRIVE (SSD) ERROR RECOVERY FLOW BASED ON REINF
MP13010	MP13010PR	US	62/816,760	3/11/2019			Pending	SELF SERVO WRITE PATTERN FREQUENCY MODIFICATION
MP13011	MP13011PR	US	62/832,741	4/11/2019			Pending	RESOURCE UNIT (RU) INDICATION FOR UPLINK (UL) MULTI-USER (M
MP13012	MP13012PR	US	62/823,504	3/25/2019			Pending	BASIC SERVICE SET (BSS) WITH MULTIPLE CHANNEL SEGMENTS OR >
MP13012	MP13012PR2	US	62/831,593	4/9/2019			Pending	Next Generation Wireless 20MHz Operation
MP13012	MP13012PR3	US	62/870,437	7/3/2019			Pending	BASIC SERVICE SET (BSS) WITH MULTIPLE CHANNEL SEGMENTS OR >

PATENT
REEL: 057897 FRAME: 0550

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP13013	MP13013PR	US	62/821,933	3/21/2019			Pending	RESOURCE UNIT (RU) INDICATION FOR DOWNLINK (DL) MULTI-USER
MP13014	MP13014CN	CN	201910169178.1	3/6/2019			Pending	A METHOD AND AN APPARATUS FOR WAKING A PHYSICAL LAYER OF
MP13016	MP13016PR	US	62/852,597	5/24/2019			Pending	DUMMY DIE REPLACEMENT FOR PERIPHERAL DIE ON MCM PACKAG
MP13017	MP13017PR	US	62/821,936	3/21/2019			Pending	ACCESS POINT (AP) COORDINATED ORTHOGONAL FREQUENCY MUL
MP13017	MP13017PR2	US	62/837,106	4/22/2019			Pending	ACCESS POINT (AP) COORDINATED ORTHOGONAL FREQUENCY MUL
MP13017	MP13017PR3	US	62/934,452	11/12/2019			Pending	ACCESS POINT (AP) COORDINATED ORTHOGONAL FREQUENCY MUL
MP13019	MP13019PR	US	62/810,785	2/26/2019			Pending	Random Access Interleaved Sectors for Magnetic Recording
MP13020	MP13020PR	US	62/832,757	4/11/2019			Pending	EXTRA HIGH THROUGHPUT (EHT) AGGREGATED PLCP PROTOCOL DA
MP13021	MP13021PR	US	62/849,043	5/16/2019			Pending	BASIC SERVICE SET (BSS) OPERATION WITH BAND AGGREGATION - C
MP13021	MP13021PR2	US	62/877,207	7/22/2019			Pending	BASIC SERVICE SET (BSS) OPERATION WITH BAND AGGREGATION - C
MP13025	MP13025PR	US	62/832,764	4/11/2019			Pending	EXTRA HIGH THROUGHPUT (EHT) AGGREGATED PLCP PROTOCOL DA
MP13026	MP13026PR	US	62/814,195	3/5/2019			Pending	ADAPTIVE SINGLE SOLID-STATE (SSD) CONTROLLER BANDWIDTH TO
MP13027	MP13027	US	16/578,478	9/23/2019			Pending	Multi-Protocol Frame Format
MP13028	MP13028PR	US	62/866,466	6/25/2019			Pending	SYNCHRONOUS WRITE PATTERN FREQUENCY MODIFICATION
MP13029	MP13029PR	US	62/832,768	4/11/2019			Pending	In-band sleep/wake-up command and status
MP13030	MP13030PR	US	62/816,765	3/11/2019			Pending	Full Duplex data transmission via TDM data transmission over chann
MP13032	MP13032PR	US	62/816,767	3/11/2019			Pending	ASYMMETRICAL AUTOMOTIVE ETHERNET PHY
MP13050	MP13050PR	US	62/934,436	11/12/2019			Pending	DATACENTER ON WHEELS
MP13051	MP13051	US	0				Not Filed	Peer-to-peer NVMe-oF SSD Communication over Fabric Without Hos
MP13051	MP13051PR	US	62/818,566	3/14/2019			Pending	Peer-to-peer NVMe-oF SSD Communication over Fabric Without Hos
MP13052	MP13052PR	US	62/818,621	3/14/2019			Pending	NVMe-oF SOLID-STATE DRIVE (SSD)
MP13055	MP13055PR	US	62/866,285	6/25/2019			Pending	Machine Learning Switch for Real Time Automotive System Monitori
MP13058	MP13058PR	US	62/854,812	5/30/2019			Pending	Qualification tests of Channel state information (CSI) Reports in WLA
MP13060	MP13060PR	US	62/860,192	6/11/2019			Pending	Ring Oscillator Based Temperature Sensor with Low Supply Sensitivit
MP13061	MP13061PR	US	62/854,820	5/30/2019			Pending	BASICE SERVICE SET (BSS) WITH MULTIPLE CHANNEL SEGMENTS: BA
MP13064	MP13064PR	US	62/934,442	11/12/2019			Pending	RAPID DETECTION OF 100 OR 1000 BASE-T1 ON SLAVE SIDE
MP13065	MP13065PR	US	62/869,906	7/2/2019			Pending	Multi frequency spiral track
MP13067	MP13067PR	US	62/852,612	5/24/2019			Pending	BASICE SERVICE SET (BSS) WITH BAND AGGREGATION - POWER SAV
MP13067	MP13067PR2	US	62/879,801	7/29/2019			Pending	BASIC SERVICE SET (BSS) WITH BAND AGGREGATION - POWER SAVE
MP13067	MP13067PR3	US	62/886,812	8/14/2019			Pending	BASICE SERVICE SET (BSS) WITH BAND AGGREGATION - POWER SAV
MP13067	MP13067PR4	US	62/888,950	8/19/2019			Pending	BASICE SERVICE SET (BSS) WITH BAND AGGREGATION - POWER SAV
MP13067	MP13067PR5	US	62/897,155	9/6/2019			Pending	BASICE SERVICE SET (BSS) WITH BAND AGGREGATION - POWER SAV
MP13068	MP13068PR	US	62/854,834	5/30/2019			Pending	TRAFFIC SPECIFICATION ANNOUNCEMENT FOR TARGET WAKE TIME
MP13069	MP13069PR	US	62/857,646	6/5/2019			Pending	VHTSIGB EQUALIZATION

PATENT
REEL: 057897 FRAME: 0551

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP13073	MP13073PR	US	62/857,656	6/5/2019			Pending	Split-Cascode Transistors Technique for 50% Duty Cycle Passive Mixe
MP13076	MP13076PR	US	62/852,620	5/24/2019			Pending	HIGH SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG
MP13077	MP13077PR	US	62/863,699	6/19/2019			Pending	MULTI-BAND OPERATION: SYNCHRONIZED AND UNSYNCHRONIZED
MP13079	MP13079PR	US	62/863,713	6/19/2019			Pending	MULTI-BAND OPERATION: SINGLE BAND STATION (STA) AND LEGAC
MP13081	MP13081PR	US	62/853,635	5/28/2019			Pending	ACCESS POINT (AP) POWER SAVE: BASIC SERVICE SET (BSS) QUIET PE
MP13082	MP13082PR	US	62/854,841	5/30/2019			Pending	METHOD AND APPARATUS FOR EFFICIENTLY INCREASING THE AVAIL
MP13083	MP13083PR	US	62/869,916	7/2/2019			Pending	METHOD OF REAL-TIME INTEGRATED CIRCUIT (IC) CHIP ROBUSTNES
MP13085	MP13085PR	US	62/857,661	6/5/2019			Pending	Gain-Boosted Transformer Coupled Common Gate Low-Noise Ampli
MP13086	MP13086PR	US	62/857,666	6/5/2019			Pending	HYBRID ARQ (HARQ) TRANSMISSION ENABLER-ENCODER AND PREA
MP13087	MP13087PR	US	62/859,553	6/10/2019			Pending	NULL DATA PACKET (NDP) POWER CONTROL FOR ERROR VECTOR M
MP13089	MP13089PR	US	62/859,560	6/10/2019			Pending	BALL GRID ARRAY (BGA) PACKAGE UPPER CONNECTION TO MEMOR
MP13091	MP13091PR	US	62/866,475	6/25/2019			Pending	ENCODING PROCESS AND PRE-FORWARD ERROR CORRECTION (FEC)
MP13092	MP13092PR	US	62/869,926	7/2/2019			Pending	Low Leakage Highly Reliable Continuous Diffusion Structures and Me
MP13094	MP13094PR	US	62/875,419	7/17/2019			Pending	DIGITALLY ASSISTED PROCESS AND TEMPERATURE AWARE ULTRA-F
MP13096	MP13096PR	US	62/875,432	7/17/2019			Pending	DOUBLE PARITY RAID IMPLEMENTATION IN SSD CONTROLLERS
MP13099	MP13099PR	US	62/879,781	7/29/2019			Pending	VERIFICATION SHADOW PIPE
MP13101	MP13101PR	US	62/879,789	7/29/2019			Pending	On-Chip High Density Capacitor, Structures and Method of Making t
MP13102	MP13102PR	US	62/886,822	8/14/2019			Pending	HARDWARE BASED SUCCESSIVE INTERFERENCE CANCELLATION (SIC)
MP13105	MP13105PR	US	62/876,452	7/19/2019			Pending	IMPLEMENTING TRANSLATION LOOK-ASIDE BUFFER INVALIDATE (TL
MP13106	MP13106PR	US	62/876,460	7/19/2019			Pending	Multi-level Correlated Prefetcher for an Out-of-Order Processor Cor
MP13107	MP13107PR	US	62/876,468	7/19/2019			Pending	Using Backpressure Latency to Adjust Prefetch Lookup Distance in O
MP13108	MP13108PR	US	62/876,492	7/19/2019			Pending	Vector Prefetcher in an Out-of-Order Core
MP13109	MP13109PR	US	62/876,499	7/19/2019			Pending	Long-range Schedules for an Out-of-Order Core
MP13110	MP13110PR	US	62/876,505	7/19/2019			Pending	SOFTWARE-DIRECTED OUT-OF-ORDER EXECUTED WITHOUT EXCEPTI
MP13111	MP13111PR	US	62/875,439	7/17/2019			Pending	FREQUENCY SCALING TO REDUCE BOOT TIME
MP13113	MP13113PR	US	62/879,795	7/29/2019			Pending	OBJECT-ORIENTED MEMORY
MP13115	MP13115PR	US	62/871,541	7/8/2019			Pending	METHOD FOR SYNCHRONIZING TIME REFERENCES ON MULTIPLE DE
MP13117	MP13117PR	US	62/927,584	10/29/2019			Pending	BLIND EQUALIZER FOR HIGH ORDER PULSE AMPLITUDE MODULATIO
MP13118	MP13118PR	US	62/893,070	8/28/2019			Pending	Pre-Code for A Two-Way Asymmetrical PHY over a single pair of cabl
MP13124	MP13124PR	US	62/936,238	11/15/2019			Pending	SYSTEM AND TECHNIQUE FOR IMPROVING RADIATED IMMUNITY A
MP13125	MP13125PR	US	62/936,244	11/15/2019			Pending	"LOOP INDUCTANCE NOISE CANCELLATION" TO SOLVE TRANSIENT IS
MP13127	MP13127PR	US	62/943,682	12/4/2019			Pending	Apparatus of implementing 2-port read and 1-port write using 8T SR
MP13129	MP13129PR	US	62/943,690	12/4/2019			Pending	Using Machine Learning to Manipulate Memory Accesses to Alter As
MP13130	MP13130PR2	US	62/909,080	10/1/2019			Pending	MULTI-BAND OPERATION: AGGREGATE MAC PROTOCOL DATA UNIT

PATENT
REEL: 057897 FRAME: 0552

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP13130	MP13130PR3	US	62/934,418	11/12/2019			Pending	MULTI-BAND OPERATION: AGGREGATE MAC PROTOCOL DATA UNIT
MP13143	MP13143PR	US	62/927,588	10/29/2019			Pending	CROSS ENTROPY BASED ADAPTATION OF LINEAR FINITE IMPULSE RE
MP13144	MP13144PR	US	62/927,591	10/29/2019			Pending	CROSS ENTROPY BASED ADAPTATION OF TARGET AND LINEAR FINIT
MP13145	MP13145PR	US	62/943,692	12/4/2019			Pending	CROSS ENTROPY BASED ADAPTATION OF NON-LINEAR FINITE IMPUL
MP13146	MP13146PR	US	62/943,699	12/4/2019			Pending	MODIFIED BRANCH-METRIC FOR NON-LINEAR FINAL IMPULSE RESP
MP13155	MP13155PR	US	62/916,105	10/16/2019			Pending	Ultra-Core CPU for High Performance Chips
MP13157	MP13157	US	16/708,085	12/9/2019			Pending	Self-Encryption Drive (SED)
MP13157	MP13157C1	US	16/708,203	12/9/2019			Pending	Self-Encryption Drive (SED)
MP13157	MP13157CN	CN	201911262133.5	12/10/2019			Pending	METHOD AND APPARATUS FOR DECOMMISSIONING A HARD DISK D
MP13157	MP13157EP	EP	19214955.7	12/10/2019			Pending	METHOD AND APPARATUS FOR DECOMMISSIONING A HARD DISK D
MP13157	MP13157KR	KR	0	12/10/2019			Not Filed	METHOD AND APPARATUS FOR DECOMMISSIONING A HARD DISK D
MP13157	MP13157PR	US	62/934,701	11/13/2019			Pending	METHOD AND APPARATUS FOR DECOMMISSIONING A HARD DISK D
MP13159	MP13159PR	US	62/916,113	10/16/2019			Pending	Shingled Magnetic Recording using data compression
MP13160	MP13160PR	US	62/912,495	10/8/2019			Pending	Methodology for Effective Interleaving in Random Access Interleave
MP13166	MP13166	US	0				Not Filed	Method and apparatus for HW efficient implementation of Int9 qua
MP13168	MP13168	US	0				Not Filed	OCM port throttling for bandwidth
MP13169	MP13169	US	0				Not Filed	Mesh architecture for high bandwidth broadcast, multicast network
MP13171	MP13171	US	0				Not Filed	Mechanism to manage power to a power profile by throttling perfor
MP13172	MP13172	US	0				Not Filed	Throttling mechanism for managing thermal and power -- pulse squa
MP13183	MP13183	US	0				Not Filed	INSTRUCTION SCHEDULING ALGORITHM TO PREVENT SIDE-CHANNE
MP13183	MP13183PR	US	62/944,243	12/5/2019			Pending	INSTRUCTION SCHEDULING ALGORITHM TO PREVENT SIDE-CHANNE
MP13184	MP13184	US	0				Not Filed	DYNAMICALLY MARKING INSTRUCTIONS AS SENSITIVE TO ALLOW H
MP13184	MP13184PR	US	62/944,245	12/5/2019			Pending	DYNAMICALLY MARKING INSTRUCTIONS AS SENSITIVE TO ALLOW H
MP13185	MP13185	US	0				Not Filed	MICROARCHITECTURAL TAG FLOW FOR SENSITIVE INSTRUCTIONS T
MP13185	MP13185PR	US	62/944,251	12/5/2019			Pending	MICROARCHITECTURAL TAG FLOW FOR SENSITIVE INSTRUCTIONS T
MP13186	MP13186	US	0				Not Filed	USE OF RIGHT TO REPLACE TO PROTECT AGAINST PRIME-AND-PROB
MP13186	MP13186PR	US	62/944,263	12/5/2019			Pending	USE OF RIGHT TO REPLACE TO PROTECT AGAINST PRIME-AND-PROB
MP13187	MP13187	US	0				Not Filed	PREVENTING SIDE-CHANNEL ATTACKS BY INTRODUCING NOISY INST
MP13187	MP13187PR	US	62/944,265	12/5/2019			Pending	PREVENTING SIDE-CHANNEL ATTACKS BY INTRODUCING NOISY INST
MP13189	MP13189	US	0				Not Filed	MICROPARTITIONS TO PREVENT SPECULATION-BASED SECURITY AT
MP13189	MP13189PR	US	62/944,269	12/5/2019			Pending	MICROPARTITIONS TO PREVENT SPECULATION-BASED SECURITY AT
MP13194	MP13194PR	US	62/936,232	11/15/2019			Pending	CAR AS AN "OPEN PLATFORM"
MP13206	MP13206PR	US	62/944,274	12/5/2019			Pending	Using Differential Cache Block Size in the Processor Core and DDR ch
MP13208	MP13208PR	US	62/944,278	12/5/2019			Pending	Implementing Last-Level Cache Way Allocation with a Processor Cor

PATENT
REEL: 057897 FRAME: 0553

Family	IP Right ID	Country	Application Number	Filing Date	Patent Number	Issue Date	IP Right Status	Title
MP1477	MP1477	US	10/329,124					
MP2325	MP2325I1C1	US	13/924,333	6/21/2013	9294130	3/22/2016	In Force	QUASI-CYCLIC LOW-DENSITY PARITY-CHECK (QC-LDPC) ENCODER
MP2522	MP2522PR	US	61/039,772					
MP2744	MP2744C1	US	13/928,771	6/27/2013	9055296	6/9/2015	In Force	Processing Rasterized Data
MP3004	MP3004I1C1	US	14/089,501	11/25/2013	9122590	9/1/2015	In Force	Flash Memory Read Performance
MP3008	MP3008I1C1	US	14/462,821	8/19/2014	9695832	7/4/2017	In Force	Apparatuses For Controlling Operation Of A Motor Of A Fan Assembl
MP4563	MP4563sUWa	US	13/457,001	4/26/2012	8522246	8/27/2013	In Force	METHOD FOR PACKET FLOW CONTROL USING CREDIT PARAMETERS
MP4563	MP4563sUWZ	US	13/960,954	8/7/2013	8997105	3/31/2015	In Force	METHOD FOR PACKET FLOW CONTROL USING CREDIT PARAMETERS
MP4832	MP4832	US	14/180,990	2/14/2014	9408274	8/2/2016	In Force	Light Emitting Diodes Generating White Light
MP5208	MP5208PR	US	61/763,344					
MP5348	MP5348PR	US	61/832,067					
MP5424	MP5424I1	US	15/069,483	3/14/2016	9699545	7/4/2017	In Force	LOW-POWER METHOD AND CIRCUITRY OF DETERMINING HEADPHO
MP5483	MP5483	US	14/515,363	10/15/2014			Pending	METHODS AND NETWORK DEVICE FOR PERFORMING CUT-THROUG
MP6385	MP6385	US	15/886,728	2/1/2018			Pending	Methods and Apparatus for Partially Encrypted Firmware

RECORDED: 10/24/2021
PATENT
REEL: 057897 FRAME: 0554