PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7188154

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
REDPINE SIGNALS, INC.	08/31/2021

RECEIVING PARTY DATA

Name:	CEREMORPHIC, INC.
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Internal Address:	SUITE 540
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95131

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17677198

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	JAY A. CHESAVAGE
SIGNATURE:	/Jay A. Chesavage/
DATE SIGNED:	02/22/2022

Total Attachments: 5
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PATENT ASSIGNMENT

This Patent Assignment ("**Assignment**"), dated as of **Aug 31, 2021** (the "**Effective Date**"), is entered into by and between Redpine Signals, Inc ("**Redpine**"), a corporation of California, and Ceremorphic, Inc ("**Ceremorphic**"), a corporation of California. "**Redpine**" and "**Ceremorphic**" may hereinafter be referred to collectively as the "**Parties**" or individually as a "**Party**."

RECITALS

WHEREAS, "**Redpine**" is the owner of record of all right, title and interest in and to the following trademark and trademark application (the "**Trademarks**") listed on EXHIBIT A, and patents and patent applications (the "**Patents**") listed on EXHIBIT B, and;

WHEREAS, for valuable consideration, and effective **Aug 31, 2021**, the Parties wish hereby to provide for the transfer of ownership of the Trademarks and Patents from "**Redpine**" to "**Ceremorphic**",

NOW THEREFORE, for good and valuable consideration of US $1.00 (United States One Dollar), the receipt and sufficiency of which is hereby acknowledged, the Parties hereby agree as follows:

"**Redpine**" hereby assigns, grants and conveys to "**Ceremorphic**" all of the "**Redpine**" right, title and interest in and to said Trademarks and to Patents and each of them, and in and to all patent reissues, divisions, continuations, renewals, extensions and continuations-in-part thereof, international patents, patent applications (including national phase applications filed pursuant to any PCT Applications referenced in EXHIBIT B), trademarks, and trademark applications filed thereof, and all rights of "**Redpine**" associated therewith, including the right to sue for any past infringement.

IN WITNESS WHEREOF, the Parties hereto have executed and delivered this Trademark and Patent Assignment as of the date first hereinabove written.

ASSIGNOR:
Redpine Signals, Inc.
2107 N. 1st St.
Suite 540
San Jose, Ca. 95131

DocuSigned by:
By: venkat Mattela Date 11/29/2021
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Venkat Mattela, CEO, Redpine Signals, Inc.

ASSIGNEE:
Ceremorphic, Inc
2107 N. 1st St.
Suite 540
San Jose, Ca. 95131

By: DocuSigned by: Venkat Mattela 8C294F899FD04D2... Date 11/29/2021

Venkat Mattela, CEO, Ceremorphic, Inc.

EXHIBIT A - Trademarks

AttorneyRef	Application s/n	FilingDate	PatentNum	IssueDate	Title
tm-Ceremorphic(img)	88268280	1/19/19			CEREMORPHIC (image)
tm-Ceremorphic(word)	88268283	1/19/19			Ceremorphic (text)
tm-flexmac_1	90841085	7/21/21			FLEXMAC
tm-flexmac-aban	87624725	9/27/17			FLEXMAC
tm-flexmath-expired	87624883	9/27/17			FLEXMATH
tm-flexmath-refile	90557828	3/3/21			FLEXMATH
tm-lunimas	87627357	9/29/17			LUNIMAS
tm-neurochain	88449641	5/28/19			NEUROCHAIN
tm-Quantum Machines_1	90841111	7/21/21			QUANTUM MACHINES
tm-Quantum Machines-aban	87451325	5/16/17			QUANTUM MACHINES
tm-queblocks	87826321	3/8/18	5639722	12/25/18	QUEBLOCKS
tm-quecloud	87826388	3/8/18	5735095	4/23/19	QUECLOUD
tm-quessence	87648406	10/17/17	5728859	4/16/19	Quessence
tm-Threadarch	77433464	3/27/08	3637552	6/16/09	THREADARCH

EXHIBIT B - Patents and Patent Applications

AttorneyRef	Application s/n	FilingDate	PatentNum	IssueDate	Title
CER-0152	17/006,819	8/29/20	11101800	8/24/21	Interlayer Exchange Coupling Logic Cells
CER-0040-C1	16/715,759	12/16/19	10931301	2/23/21	Decompression Engine for Executable Microcontroller Code
CER-0040	16/140,526	9/24/18	10541708	1/21/20	Decompression Engine for Executable Microcontroller Code
CER-0030	15/979,257	5/14/18	10528641	1/7/20	Encoder and Decoder for Transmission of Coefficients to a Neural Network
CER-0010	11/899,557	9/6/07	7761688	7/20/10	MULTIPLE THREAD IN-ORDER ISSUE IN-ORDER COMPLETION DSP AND MICRO-CONTROLLER
CER-0020	12/024,804	2/1/08	7657683	2/2/10	CROSS-THREAD INTERRUPT CONTROLLER FOR A MULTI-THREAD PROCESSOR
CER-0050	15/459,204	3/15/17			Two-Factor Authentication with User-selected Passcode Modification
CER-0050-PCT	PCT/US18/22535	3/15/18			TWO-FACTOR AUTHENTICATION WITH USER-SELECTED PASSCODE MODIFICATION
CER-0060	16/992,098	8/13/20			System and Method for Flash and RAM allocation for Reduced Power Consumption in a Processor

CER-0060-PCT	PCT/US20/50590	9/11/20			System and Method for Flash and RAM allocation for Reduced Power Consumption in a Processor
CER-0060-prov	62/899,084	9/11/19			System and Method for Flash and RAM allocation in a Wireless Signal Processor
CER-0070	16/945,936	8/3/20			Multi-Threaded Processor with Thread Granularity
CER-0070-prov	62/899,079	9/11/19			Multi-Threaded Processor with Thread Granularity
CER-0090	15/978,095	5/12/18			METHOD AND APPARATUS FOR COMPRESSION AND DECOMPRESSION OF A NUMERICAL FILE
CER-0100-prov	62/711,555	7/29/18			METHOD AND SYSTEM FOR SAVING POWER IN A REAL TIME HARDWARE PROCESSING UNIT
CER-0100	16/445,238	6/19/19			METHOD AND SYSTEM FOR SAVING POWER IN A REAL TIME HARDWARE PROCESSING UNIT
CER-0100-C1	17/461,923	8/30/21			METHOD AND SYSTEM FOR SAVING POWER IN A REAL TIME HARDWARE PROCESSING UNIT
CER-0110	17/006,815	8/29/20			Analog Multiplier Accumulator for Dot Product Computation
CER-0121	17/180,831	2/21/21			Floating Point Dot Product Multiplier-Accumulator
CER-0122	17/180,856	2/21/21			Process for Floating Point Dot Product Multiplier-Accumulator
CER-0151	17/006,818	8/29/20			Interlayer Exchange Coupling Logic Cells
CER-0161	17/139,226	12/31/20			Unit Element for Asynchronous Analog Multiplier Accumulator
CER-0162	17/139,242	12/31/20			Cascade Multiplier using Unit Element Analog Multiplier-Accumulator
CER-0163	17/139,935	12/31/20			Scaleable Analog Multiplier-Accumulator with Shared Result Bus
CER-0164	17/139,945	12/31/20			Differential Analog Multiplier-Accumulator
CER-0165	17/139,955	12/31/20			Differential Analog Multiplier for a Signed Binary Input
CER-0170	17/214,804	3/27/21			Reconfigurable Multi-Thread Processor for Simultaneous Operations on Split Instructions and Operands
CER-0200	17/114,498	12/8/20			Interlayer Exchange Coupled Adder
CER-0213	17/334,704	5/29/21			Chip to Chip Communication routing using Header Amplitude
CER-0214	17/334,703	5/29/21			Chip to Chip Network Routing using DC Bias and Differential Signaling
CER-0220	17/463,535	8/31/21			Instruction Cache for multi-thread processor
CER-0230 17/588,767	63/215,455	6/26/21			Chip to Chip Interconnect Beyond Sealring Boundary
CER-0240	17/234,792	4/19/21			Interlayer Exchange Coupled Multiplier
CER-0250	17/234,814	4/20/21			Nanomagnetic Multiplier using Dipole Nanomagnetic Structures
CER-0271	17/163,493	1/31/21			Architecture for Multiplier Accumulator using Unit Elements for Multiplication, Bias, Accumulation, and Analog to Digital Conversion over a Shared Charge Transfer Bus (Fig 2)

CER-0272	17/163,494	1/31/21			Differential Unit Element for Multiply-Accumulate Operations on a Shared Charge Transfer Bus (Fig 3A/B)
CER-0273	17/163,556	2/1/21			Layout Structure for Shared Analog Bus in Unit Element Multiplier (Fig 3C)
CER-0274	17/163,588	2/1/21			Bias Differential Unit Element for Binary Weighted Analog Bus (Fig 4A/B)
CER-0275	17/164,689	2/1/21			Successive Approximation Register Using Switched Unit Elements (Fig 5A+)
CER-0280	63/173,397	4/10/21			Interlayer Exchanged Coupled Nanomagnetic Adder
CER-0291	17/214,802	3/27/21			MITIGATION OF BRANCH MISPREDICTION PENALTY IN A HARDWARE MULTI-THREAD MICROPROCESSOR
CER-0292	17/214,805	3/27/21			METHOD FOR REDUCING LOST CYCLES AFTER BRANCH MISPREDICTION IN A MULTI-THREAD MICROPROCESSOR
CER-0310	17/359,545	6/26/21			Efficient Storage of Blockchain in Embedded Device
CER-0320	17/359,546	6/26/21			Device Authentication using Blockchain
CER-0341	17/352,370	6/21/21			Power Saving Floating Point Multiplier-Accumulator with Precision-Aware Accumulation
CER-0342	17/352,372	6/21/21			Process for Performing Floating Point Multiply-Accumulate Operations with Precision Based on Exponent Differences for Saving Power
CER-0343	17/352,373	6/21/21			Power Saving Floating Point Multiplier-Accumulator With a High Precision Accumulation Detection Mode
CER-0344	17/352,374	6/21/21			Process for Dual Mode Floating Point Multiplier-Accumulator with High Precision Mode for Near Zero Accumulation Results
CER-0351	17/334,782	5/30/21			Architecture for Analog Multiplier-Accumulator with Binary Weighted Charge Transfer Capacitors
CER-0352	17/334,816	5/31/21			Multiplier-Accumulator Unit Element with Binary Weighted Charge Transfer Capacitors
CER-0353	17/334,817	5/31/21			Bias Unit Element with Binary Weighted Charge Transfer Capacitors
CER-0354	17/334,887	5/31/21			Chopper Stabilized Analog Multiplier Accumulator with Binary Weighted Charge Transfer Capacitors
CER-0355	17/334,890	5/31/21			Chopper Stabilized Analog Multiplier Unit Element with Binary Weighted Charge Transfer Capacitors
CER-0356	17/334,899	5/31/21			Chopper Stabilized Bias Unit Element with Binary Weighted Charge Transfer Capacitors
CER-0357	17/335,206	6/1/21			Analog Multiplier Accumulator with Unit Element Gain Balancing
CER-0360	63/173,412	4/10/21			Three Dimensional Interlayer Exchange Coupled Convolution
CER-0358	17/515,523	10/31/2021			Modular Analog Multiplier-Accumulator Unit Element for Multi-Layer Neural Networks