PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
TRANSMETA LLC	01/28/2009

RECEIVING PARTY DATA

Name:	INTELLECTUAL VENTURE FUNDING LLC
Street Address:	502 E. JOHN STREET
City:	CARSON
State/Country:	NEVADA
Postal Code:	89706

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14295062

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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NAME OF SUBMITTER:	JONATHAN LEE
SIGNATURE:	/Jonathan Lee/
DATE SIGNED:	02/14/2022

Total Attachments: 51
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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Transmeta LLC, a Delaware limited liability company, with an office at 2460 N. 1st Street, Suite 200, San Jose, CA 95131, (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Intellectual Venture Funding LLC, a Nevada limited liability company, with an address at 502 E. John Street; Carson City, NV 89706 (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) all provisional patent applications, patents applications and patents owned or purported to be owned by Company as of the Closing including, without limitation, the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	**Country**	**Filing Date**	**Title of Patent and First Named Inventor**
5,832,205 (08/700,302)	US	11/3/1998 (8/20/1996)	A MEMORY CONTROLLER FOR A MICROPROCESSOR FOR DETECTING A FAILURE OF SPECULATION ON THE PHYSICAL NATURE OF A COMPONENT BEING ADDRESSED Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm John
CA2283559 (CA2283559)	CA	5/25/2004 (8/11/1997)	Improved Memory Control System for Microprocessor KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
CNZL97182010.4 (CN97182010.4)	CN	8/11/2004 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
JP3615770 (JP1999-512073)	JP	2/2/2005 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
JP2001-519954	JP	8/11/1997	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
KR10-0463810 (KR10-1999-0012139)	KR	12/17/2004 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
DE69739078.0 (DE69739078.0)	DE	10/29/2008 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
GB1002271 (GB97937205.9)	GB	10/29/2008 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
FR1002271 (FR97937205.9)	FR	10/29/2008 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
5,905,855 (08/807,542)	US	5/18/1999 (2/28/1997)	Method and apparatus for correcting errors in computer systems Klaiber, Alex; Bedichek, Robert; Keppel, David
CA2276494 (CA2276494)	CA	5/4/2004 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CNZL98802783.6 (CN98802783.6)	CN	11/30/2005 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
JP3654910 (JP10-9537681)	JP	(2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
KR10-0463809 (KR10-1999-7007910)	KR	12/17/2004 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
DE69831732 (DE69831732)	DE	9/28/2005 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
FR0961972 (FR198905051.3)	FR	9/28/2005 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
GB0961972(GB198905051 .3)	GB	9/28/2005(2/13/19 98)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMSKLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
5,926,832 (08/721,698)	US	7/20/1999 (9/26/1996)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
CA2262928 (CA2262928)	CA	1/30/2001 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
CNZL971080027.8 (CN971080027.8)	CN	3/10/2004 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
JP3753743 (JP1998-515799)	JP	12/22/2005 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
KR12-0385426 (KR10-1999-0702571)	KR	5/14/2003 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
DE69737423.8 (DE69737423)	DE	11/8/2008 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
FR1008050 (FR97944366.0)	FR	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
GB1008050 (GB97944366.0)	GB	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
LU1008050 (LU97944366.0)	LU	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
5958061 (08/685,721)	US	9/28/1999 (7/24/1996)	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
KR10-0522468 (KR10-1999-7012138)	KR	10/11/2005 (7/11/1997)	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CA2283772 (CA2283772)	CA	10/15/2002 (7/11/1997)	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
CNZL97182374.X (CN97182374.X)	CN	5/7/2003 (7/11/1997)	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
EP97933377.0	EP	7/11/1997	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
JP3654913 (JP11-508580)	JP	6/2/2005 (11/10/1999)	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
6011908 (08/772,686)	US	1/4/2000 (12/23/1996)	Gated store buffer for an advanced microprocessor Wing, Malcolm J.; D'Souza, Godfrey P.
CA2270122 (CA2270122)	CA	9/4/2001 (12/12/1997)	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
CNZL97180942.9 (CN97180942.9)	CN	3/12/2003 (12/12/1997)	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
JP3537448(JP10-528830)	JP	3/26/2004(12/12/1997)	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSORWING MALCOLM J; D SOUZA GODFREY P
EP97951635.8	EP	12/12/1997	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
KR10-0384967 (KR10-1999-7005717)	KR	6/25/2003 (6/22/1999)	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
6,031,992 (08/678,541)	US	2/29/2000 (7/5/1996)	Combining hardware and software to provide an improved microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
CA2283776 (CA2283776)	CA	2/29/2000 (6/25/1997)	Combining hardware and software to provide an improved microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
CNZL97182273.5 (CN97182273.5)	CN	8/25/2004 (6/25/1997)	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
JP3776132 (JP11-504361)	JP	5/17/2006 (6/25/1997)	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
KR10-0443759 (KR10-1999-7012137)	KR	7/29/2004 (6/25/1997)	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
EP97936951.9	EP	6/25/1997	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,172,925 (09/333,178)	US	1/9/2001 (6/14/1999)	Memory array bitline timing circuit Bloker, Raymond E.
6,199,152 (08/702,771)	US	3/6/2001 (8/22/1996)	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
CA2283560 (CA2283560)	CA	12/9/2003	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
CNZL97182229.8 (CN97182229.8)	CN	6/4/2008 (8/11/1997)	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
JP3621116 (JP11-512072)	JP	11/26/2004 (8/11/1997)	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
KR10-0421687 (KR10-1999-7012140)	KR	2/24/2004 (8/11/1997)	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
09/699,947	US	10/30/2000	TRANSLATED MEMORY PROTECTION APPARATUS FOR AN ADVANCED MICROPROCESSOR Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
10/438,158	US	5/13/2003	Translated memory protection apparatus for an advanced microprocessor Edmund J Kelly; Robert F Cmelik; Malcolm J King
11/248,813	US	10/11/2006	TRANSLATED MEMORY PROTECTION APPARATUS FOR AN ADVANCED MICROPROCESSOREdmund J. Kelly;Robert F. Cmelik;Malcolm J. Wing
5,497,499 (08/219,425)	US	3/5/1996 (3/29/1994)	Superscalar risc instruction scheduling Garg, Sanjiv; Iadonato, Kevin R.; Nguyen, Le T.; Wang, Johannes
5,737,624 (08/594,401)	US	4/7/1998 (1/31/1996)	Superscalar risc instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
5,974,526 (08/990,414)	US	10/26/1999 (12/15/1997)	Superscalar RISC instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
6289433 (09/329,354)	US	9/11/2001 (6/10/1999)	Superscalar RISC instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
DE69311330 (DE69311330.8)	DE	(3/26/1993)	Superscalar Risc Instruction Scheduling Sanjiv Garg
JP3571263 (JP2000-008144)	JP	7/2/2004 (3/26/1993)	Register Name Change System Sanjiv Garg
JP3571264 (JP2000-008145)	JP	7/2/2004 (3/26/1993)	Register Name Change System Sanjiv Garg
JP3571265 (JP2000-008146)	JP	9/29/2004 (3/26/1993)	Computer System Sanjiv Garg
JP3571266 (JP2000-008148)	JP	7/2/2004 (3/26/1993)	Computer System Sanjiv Garg

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP3571267 (JP2000-008149)	JP	7/2/2004 (3/26/1993)	Superscalar Processor Sanjiv Garg
JP3730252 (JP05-517293)	JP	12/21/2005 (3/26/1993)	Superscalar RISC instruction scheduling Sanjiv Garg
7,051,187 (10/086,197)	US	5/23/2006 (3/1/2002)	Superscalar RISC instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
11/730,566	US	4/2/2007	Superscalar RISC instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
90/008,712	US	6/11/2007	Superscalar RISC instruction scheduling Garg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
90/008,691	US	6/11/2007	Superscalar Risc Instruction Scheduling (unknown)
KR10-0294277 (KR10-1994-0703382)	KR	4/13/2001 (9/28/1994)	Superscalar Processor Sanjiv Garg
KR10-0371927 (KR10-2000-7014693)	KR	1/28/2003 (3/26/1993)	Superscalar Processor Sanjiv Garg
KR10-0371930 (KR10-2000-7014694)	KR	1/28/2003 (3/26/1993)	Superscalar Processor Sanjiv Garg
6,356,615 (09/417,930)	US	3/12/2002 (10/13/1999)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
CA2380077 (CA2380077)	CA	3/6/2007 (9/6/2000)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
CNZL00814184.3 (CN00814184.3)	CN	9/6/2000 (9/6/2000)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
GB1234277(GB00961695.4)	GB	6/18/2008(9/6/2000)	Programmable event counter systemCoon, Brett; Keppel, David; Price, Charles R.
KR10-0596761 (KR10-2002-7004729)	KR	6/27/2006 (4/12/2002)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
6,363,336 (09/417,356)	US	3/26/2002 (10/13/1999)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
CA2384254 (CA2384254)	CA	11/2/2004 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
CNZL00814186.X (CN00814186.X)	CN	4/13/2005 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
JP2001-530689	JP	9/6/2000	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP2006-112312	JP	4/14/2006	Fine grain translation discrimination method and device Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
KR10-0573446 (KR10-2002-7004731)	KR	4/17/2006 ()	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
CY1240582 (CY00960034.7)	CY	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
DE60036960.9 (DE60036960.9)	DE	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
FI1240582 (FI09600034.7)	FI	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
FR1240582 (FR09600034.7)	FR	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
GB1240582 (GB09600034.7)	GB	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
GR1240582 (GR09600034.7)	GR	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
IT1240582 (IT09600034.7)	IT	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
LU1240582 (LU09600034.7)	LU	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
MC1240582 (MC09600034.7)	MC	6/18/2008 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
6,415,379 (09/417,981)	US	7/2/2002 (10/13/1999)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
CA2379976	CA	9/6/2000	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
CNZL00814315.3(CN00814315.3)	CN	7/12/2006(9/6/2000)	Method and apparatus for maintaining context while executing translated instructionsKeppel, David; Cmelik,Robert; Bedichek,Robert
CN210118881.8	CN	9/6/2000	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
JP3786603 (JP2001-530687)	JP	6/14/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
KR10-0498272 (KR10-2002-7004740)	KR	6/21/2005 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CY1226492 (CY00974084.6)	CY	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
FR1226492 (FR00974084.6)	FR	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
GB1226492 (GB00974084.6)	GB	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
IE1226492 (IE00974084.6)	IE	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
DE60028069.1 (DE60028069.1)	DE	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
6,429,491 (09/421,614)	US	8/6/2002 (10/20/1999)	Electrostatic discharge protection for MOSFETs Schnaitter, William N.
5,895,503 (08/458,479)	US	4/20/1999 (6/2/1995)	Address translation method and mechanism using physical address information including during a segme Belgard, Richard A.
6,226,733 (08/905,356)	US	5/1/2001 (8/4/1997)	Address translation mechanism and method in a computer system Belgard, Richard A.
5,960,466 (08/905,410)	US	9/28/1999 (8/4/1997)	Computer address translation using fast address generator during a segmentation operation performed on a virtual address Belgard, Richard A.
6,430,668 (09/757,439)	US	8/6/2002 (1/10/2001)	Speculative address translation for processor using segmentation and optical paging Belgard, Richard
6,813,699 (10/166,432)	US	11/2/2004 (6/10/2002)	Speculative address translation for processor using segmentation and optional paging Belgard, Richard
10/979,499	US	11/1/2004	Speculative address translation for processor using segmentation and optional paging Richard Belgard
95/000,257	US	6/8/2007	Speculative address translation for processor using segmentation and optional paging Belgard, Richard
90/008,722	US	6/15/2007	Address translation method and mechanism using physical address information including during a segmentation process Belgard, Richard
95/000,275	US	6/18/2007	Speculative address translation for processor using segmentation and optional paging Belgard, Richard
90/008,723	US	6/21/2007	Address translation mechanism and method in a computer systemBelgard, Richard
6,513,110 (09/464,644)	US	1/28/2003 (12/15/1999)	Check instruction and method Keppel, David; Serris, Paul S.; D'Souza, Godfrey

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6,571,316 (09/595,077)	US	5/27/2003 (6/16/2000)	Cache memory array for multiple address spaces D'Souza, Godfrey P.; Serris, Paul S.
6,594,821 (09/539,987)	US	7/15/2003 (3/30/2000)	Translation consistency checking for modified target instructions by comparing to original copy Banning, John; Anvin, H. Peter; Bedichek,Robert; Rozas, Guillermo J.; Shaw, Andrew; Torvalds, Linus; Wilson, Jason
7,096,460 (10/463,846)	US	8/22/2006 (6/16/2003)	Switching to original modifiable instruction copy comparison check to validate prior translation when translated sub-area protection exception slows down operation Banning, John; Anvin, H. Peter; Bedichek,Robert; Rozas, Guillermo J.; Shaw, Andrew; Torvalds, Linus; Wilson, Jason
7,404,181 (11/507,779)	US	7/22/2008 (8/21/2006)	Switching to original code comparison of modifiable code for translated code validity when frequency of detecting memory overwrites exceeds threshold Banning, John; Anvin, H. Peter; Bedichek,Robert; Rozas, Guillermo J.; Shaw, Andrew; Torvalds, Linus; Wilson, Jason
12/177,836	US	7/22/2008	SWITCHING TO ORIGINAL CODE COMPARISON OF MODIFIABLE CODE FOR TRANSLATED CODE VALIDITY WHEN FREQUENCY OF DETECTING MEMORY OVERWRITES EXCEEDS THRESHOLD John Banning; H. Peter Anvin; Robert Bedicheck; Guillermo J. Rozas; Andrew Shaw; Linus Torvalds; Jason Wilson
6,604,188 (09/421,972)	US	8/5/2003 (10/20/1999)	Pipeline replay support for multi-cycle operations wherein all VLIW instructions are flushed upon detection of a multi-cycle atom operation in a VLIW instruction Coon, Brett; D'Souza, Godfrey; Serris, Paul
10/463,820	US	6/16/2003	PIPELINE REPLAY SUPPORT FOR MULTI-CYCLE OPERATIONS Brett Coon; Godfrey D'Souza; Paul Serris
12/042,224	US	3/4/2008	Pipeline replay support for multicycle operations Brett Coon; Godfrey D'Souza; Paul Serris
6,615,300 (09/596,279)	US	9/2/2003 (6/19/2000)	Fast look-up of indirect branch destination in a dynamic translation system Banning, John; Coon, Brett; Torvalds, Linus; Choy, Brian; Wing, Malcolm; Gainer, Patrick
7,111,096 (10/463,233)	US	9/19/2006 (6/17/2003)	Fast look-up of indirect branch destination in a dynamic translation system Banning, John; Coon, Brett; Torvalds, Linus; Choy, Brian; Wing, Malcolm; Gainer, Patrick
11/524,044	US	9/19/2006	FAST LOOK-UP OF INDIRECT BRANCH DESTINATION IN A DYNAMIC TRANSLATION SYSTEMJohn Banning;Brett Coon;Linus Torvalds;Brian Choy;Malcolm Wing;Patrick Gainer
6,640,297 (09/596,280)	US	10/28/2003 (6/19/2000)	Link pipe system for storage and retrieval of sequences of branch addresses Banning, John; Coon, Brett; Hao, Eric
6,668,287 (09/464,661)	US	12/23/2003 (12/15/1999)	Software direct memory access Boyle, Patrick; Keppel, David; Klaiber, Alex; Kelly, Edmund

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6,714,904 (09/417,358)	US	3/30/2004 (10/13/1999)	SYSTEM FOR USING RATE OF EXCEPTION EVENT GENERATION DURING EXECUTION OF TRANSLATED INSTRUCTIONS TO CONTROL OPTIMIZATION OF THE TRANSLATED INSTRUCTIONS Torvalds, Linus; Keppel, David
CA2380001 (CA2380001)	CA	7/4/2006 (9/6/2000)	Controlling instruction translation using dynamic feedback Torvalds, Linus; Keppel, David
CNZL00814338.2 (CN00814338.2)	CN	4/27/2005 (9/6/2000)	Controlling instruction translation using dynamic feedback Torvalds, Linus; Keppel, David
JP3844692 (JP2001-530712)	JP	8/25/2006 (9/6/2000)	Controlling instruction translation using dynamic feedback Torvalds, Linus; Keppel, David
KR10-0496944 (KR10-2002-7004728)	KR	6/14/2005 (9/6/2000)	Controlling instruction translation using dynamic feedback Torvalds, Linus; Keppel, David
EP00974085.3	EP	9/6/2000	Controlling instruction translation using dynamic feedback Torvalds, Linus; Keppel, David
10/670,900	US	9/24/2003	CONTROLLING INSTRUCTION TRANSLATION USING DYNAMIC FEEDBACK Linus Torvalds; David Keppel
6,725,361 (09/595,199)	US	4/20/2004 (6/16/2000)	METHOD AND APPARATUS FOR EMULATING A FLOATING POINT STACK IN A TRANSLATION PROCESS Rozas, Guillermo; Dunn, David; Dobrikin, David; Klaiber, Alex; Nelsen, Daniel H.
6,728,865 (09/420,748)	US	4/27/2004 (10/20/1999)	PIPELINE REPLAY SUPPORT FOR UNALIGNED MEMORY OPERATIONS Coon, Brett; D'Souza, Godfrey; Serris, Paul
7,134,001 (10/463,223)	US	11/7/2006 (6/16/2003)	PIPELINE REPLAY SUPPORT FOR UNALIGNED MEMORY OPERATIONS Coon, Brett; D'Souza, Godfrey; Serris, Paul
11/594,672	US	11/7/2006	PIPELINE REPLAY SUPPORT FOR UNALIGNED MEMORY OPERATIONS Coon, Brett; D'Souza, Godfrey; Serris, Paul
6,738,893 (09/557,650)	US	5/18/2004 (4/25/2000)	METHOD AND APPARATUS FOR SCHEDULING TO REDUCE SPACE AND INCREASE SPEED OF MICROPROCESSOR OPERATIONS Rozas, Guillermo J.
6,738,892(09/421,615)	US	5/18/2004(10/20/1999)	USE OF ENABLE BITS TO CONTROL EXECUTION OF SELECTED INSTRUCTIONSCoon, Brett; Keppel, David
6,748,589 (09/421,484)	US	6/8/2004 (10/20/1999)	Method for increasing the speed of speculative execution Johnson, Richard; Rozas, Guillermo

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12/037,853	US	2/26/2008	Method for increasing the speed of speculative execution Johnson, Richard; Rozas, Guillermo
6,754,892 (09/464,638)	US	6/22/2004 (12/15/1999)	Instruction packing for an advanced microprocessor Johnson, Stephen C.
6,820,216 (09/822,929)	US	11/16/2004 (3/30/2001)	Method and apparatus for accelerating fault handling Cmelik,Robert; Wing, Malcolm
6,826,682 (09/603,743)	US	11/30/2004 (6/26/2000)	Floating point exception handling in pipelined processor using special instruction to detect generated exception and execute instructions singly from known correct state Rozas, Guillermo J.; Dunn, David; Cmelik,Robert
7,337,307 (10/938,091)	US	2/26/2008 (9/10/2004)	Exception handling with inserted status check command accommodating floating point instruction forward move across branch Rozas, Guillermo J.; Dunn, David; Cmelik,Robert
12/037,872	US	2/26/2008	Accelerating floating point operations Rozas, Guillermo J.; Dunn, David; Cmelik,Robert
6,829,719 (09/822,933)	US	12/7/2004 (3/30/2001)	Method and apparatus for handling nested faults Anvin, H. Peter; Keppel, David
10/980,127	US	11/1/2004	method and apparatus for handling nested faults Anvin, H. Peter; Keppel, David
6,831,494 (10/439,665)	US	12/14/2004 (5/16/2003)	Voltage compensated integrated circuits Fu,Robert; Osborn, Neal A.; Burr,James B.
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6,845,353 (09/471,447)	US	1/18/2005 (12/23/1999)	Interpage prologue to protect virtual address mappings Bedichek,Robert; Keppel, David; Banning, John
11/110,085	US	1/18/2005	INTERPAGE PROLOGUE TO PROTECT VIRTUAL ADDRESS MAPPINGS Robert Bedichek; David Keppel; John Banning
6,851,040 (09/930,625)	US	2/1/2005 (8/15/2001)	Method and apparatus for improving segmented memory addressing Anvin, H. Peter; Klaiber, Alex; Rozas, Guillermo J.; Gupta, Parag
7,334,109 (11/026,623)	US	2/19/2008 (12/30/2004)	Method and apparatus for improving segmented memory addressing Anvin, H. Peter; Klaiber, Alex; Rozas, Guillermo J.; Gupta, Parag
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EP00961665.7	EP	9/6/2000	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
CA2379978 (CA2379978)	CA	7/25/2006 (9/6/2000)	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
CNZL00814344.7 (CN00814344.7)	CN	6/16/2004 (9/6/2000)	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
JP3844691 (JP2001-530697)	JP	8/25/2006 (9/6/2000)	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
KR10-2002-7004733	KR	9/6/2000	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
7,331,041 (11/077,623)	US	2/12/2008 (3/10/2005)	Method of optimizing compiler vs interpreter mode operation in a code translator based upon amount of time spent in each mode Torvalds, Linus; Anvin, H. Peter
6,882,172 (10/124,152)	US	4/19/2005 (4/16/2002)	System and method for measuring transistor leakage current with a ring oscillator Suzuki, Shingo; Burr,James
10/334,918	US	12/31/2002	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
6,885,210 (10/672,793)	US	4/26/2005 (9/26/2003)	System and method for measuring transistor leakage current with a ring oscillator with backbias controls Suzuki, Shingo
CN200380109600.1	CN	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
JP2004-565786	JP	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
7,180,322 (10/956,207)	US	2/20/2007 (9/30/2004)	Closed loop feedback control of integrated circuits Koniaris, Kleanthes G.; Burr,James B.
7,112,978 (10/956,217)	US	9/26/2006 (9/30/2004)	Frequency specific closed loop feedback control of integrated circuits Koniaris, Kleanthes G.; Burr,James B.
6,903,564 (10/712,847)	US	6/7/2005 (11/12/2003)	Device aging determination circuit Suzuki, Shingo
7,212,022 (10/870,751)	US	5/1/2007 (6/16/2004)	System and method for measuring time dependent dielectric breakdown with a ring oscillator Suzuki, Shingo
7,126,365 (10/870,752)	US	10/24/2006 (6/16/2004)	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo

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CN200580019615.8	CN	6/14/2005	System and method for measuring time dependent dielectric breakdown Suzuki, Shingo
TW094119807	TW	6/15/2005	System and method for measuring time dependent dielectric breakdown with a ring oscillator Suzuki, Shingo
CN200580019614.3	CN	6/14/2005	System and method for measuring negative bias thermal instability Inventorship not available
JP2007-516852	JP	6/14/2005	System and method for measuring negative bias thermal instabilityInventorship not available
TW094119808	TW	6/15/2005	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo
11/528,031	US	9/26/2005	FREQUENCY SPECIFIC CLOSED LOOP FEEDBACK CONTROL OF INTEGRATED CIRCUITS Kleanthes G. Koniaris; James B. Burr
11/238,446	US	9/28/2005	BALANCED ADAPTIVE BODY BIAS CONTROL Vjekoslav Svilan; James B. Burr
11/241,552	US	9/30/2005	Method and system for latchup suppression Vjekoslav Svilan; Tien-Min Chen; Kleanthes G Koniaris; James B Burr
7,315,178 (11/248,440)	US	1/1/2008 (10/11/2005)	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo
7,456,628 (12/006,473)	US	11/25/2008 (1/2/2008)	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo
12/277,227	US	(11/24/2008)	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo
7,235,998 (11/269,989)	US	6/26/2007 (11/8/2005)	System and method for measuring time dependent dielectric breakdown with a ring oscillator Suzuki, Shingo
7,336,092 (11/490,356)	US	2/26/2008 (7/19/2006)	Closed loop feedback control of integrated circuits Koniaris, Kleanthes G.; Burr,James B.
HK06108946.2	HK	8/11/2006	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
7,336,090 (11/512,900)	US	2/26/2008 (8/29/2006)	Frequency specific closed loop feedback control of integrated circuits Koniaris, Kleanthes G.; Burr,James B.
JP2007-516853	JP	12/5/2006	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo

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HK1101086 (HK07109084.1)	HK	6/14/2005 (8/21/2007)	System and method for measuring negative bias thermal instability with a ring oscillator Suzuki, Shingo
12/037,784	US	2/26/2008	Closed loop feedback control of integrated circuits Koniaris, Kleanthes G.; Burr,James B.
7,205,758 (10/771,015)	US	4/17/2007 (2/2/2004)	SYSTEMS AND METHODS FOR ADJUSTING THRESHOLD VOLTAGE Masleid,Robert Paul; Burr,James B.
7,256,639 (10/956,218)	US	8/14/2007 (9/30/2004)	SYSTEMS AND METHODS FOR INTEGRATED CIRCUITS COMPRISING MULTIPLE BODY BIAS DOMAINS Koniaris, Kleanthes G.; Burr,James B.
11/880,351	US	7/19/2007	Systems and methods for integrated circuits comprising multiple body bias domains Kleanthes G. Koniaris; James B. Burr
10/956,722	US	9/30/2004	SYSTEMS AND METHODS FOR INTEGRATED CIRCUITS COMPRISING MULTIPLE BODY BIASING DOMAINSKleanthes G. Koniaris;Robert Paul Masleid;James B. Burr
11/787,908	US	4/17/2007	SYSTEMS AND METHODS FOR ADJUSTING THRESHOLD VOLTAGE Robert Paul Masleid, James B Burr
7,248,988 (10/791,099)	US	7/24/2007 (3/1/2004)	System and method for reducing temperature variation during burn in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
6,897,671 (10/791,241)	US	5/24/2005 (3/1/2004)	System and method for reducing heat dissipation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
6,900,650 (10/791,459)	US	5/31/2005 (3/1/2004)	System and method for controlling temperature during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
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CN200580009762.7	CN	3/1/2005	System and method for reducing heat dissipation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
CN200580006304.8	CN	3/1/2005	System and method for controlling temperature during burn-in Lawrence Sheng; Eric Cheng; Chen-Li Ho
JP2007-501956	JP	3/1/2005	System and method for regulating temperature during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
JP2007-501957	JP	3/1/2005	System and method pertaining to burn-in testing Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
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TW094106925	TW	3/8/2005	System and method for reducing temperature variation during burn in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
TW094106927	TW	3/8/2005	System and method for reducing temperature variation during burn in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
7,242,205 (11/136,038)	US	7/10/2007 (5/23/2005)	System and method for reducing heat dissipation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
11/139,116	US	5/26/2005	System and method for controlling temperature during burn-inEric Chien-Li Sheng; David Hoffman; John Laurence Niven
11/827,290	US	7/10/2007	System and method for reducing heat dissipation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
11/881,006	US	7/24/2007	System and method for reducing temperature variation during burn in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
HK07103917.7	HK	4/16/2007	System and method for reducing temperature variation during burn in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
HK07104403.6	HK	8/21/2007	System and method for reducing heat dissipation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
HK07109124.3	HK	8/21/2007	System and method for reducing temperature variation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
6,930,534 (10/439,659)	US	8/16/2005 (5/16/2003)	Temperature compensated integrated circuits Fu,Robert
11/125,555	US	5/9/2005	Inventorship not available
6,936,898 (10/334,272)	US	8/30/2005 (12/31/2002)	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.
7,098,512 (10/683,732)	US	8/29/2006 (10/10/2003)	Layout patterns for deep well region to facilitate routing body-bias voltage Pelham, Mike; Burr,James B.
CN200380108046.5	CN	12/29/2003	Well regions of semiconductor devices Pelham, Mike; Burr,James B.
JP2004-565751	JP	12/29/2003	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.
7,332,763 (10/765,316)	US	2/19/2008 (1/26/2004)	Selective coupling of voltage feeds for body bias voltage in an integrated circuit device Burr,James B.; Fu,Robert
7,211,478 (11/199,896)	US	5/1/2007 (8/8/2005)	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.

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HK1092278 (HK06108743.7)	HK	12/29/2003 (8/7/2006)	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.
7,323,367 (11/799,496)	US	1/29/2008 (5/1/2007)	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.
12/011,665	US	1/28/2008	Diagonal deep well region for routing body-bias voltage for MOSFETS in surface well regions Pelham, Mike; Burr,James B.
12/069,670	US	2/11/2008	Selective coupling of voltage feeds for body bias voltage in an integrated circuit deviceBurr,James B.; Fu,Robert
12/033,840	US	2/19/2008	Selective coupling of voltage feeds for body bias voltage in an integrated circuit device Burr,James B.; Fu,Robert
6,940,314 (10/334,264)	US	9/6/2005 (12/31/2002)	Dynamic node keeper system and method Bloker, Ray; Gupta, Parag
7,221,189 (11/199,950)	US	5/22/2007 (8/8/2005)	Dynamic node keeper system and method Bloker, Ray; Gupta, Parag
6,943,614 (10/769,140)	US	9/13/2005 (1/29/2004)	Fractional biasing of semiconductors Kuei, David
11/199,985	US	8/8/2005	Fractional biasing of semiconductors Kuei, David
5,438,668 (07/857,599)	US	8/1/1995 (3/31/1992)	System and method for extraction, alignment and decoding of CISC instructions into a nano-instruction bucket for execution by a RISC computer Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
FR0636257 (FR93906870.6)	FR	11/8/2000 (3/30/1993)	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
GB0636257 (GB93906870.6)	GB	11/8/2000 (3/30/1993)	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
DE69329644.5 (DE69329644.5)	DE	11/8/2000 (3/30/1993)	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
FR1028370 (FR00108579.4)	FR	9/15/2004 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
GB1028370 (GB00108579.4)	GB	9/15/2004 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
DE69333630.7 (DE69333630.7)	DE	9/15/2004 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes

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JP3544331 (JP2000-007259)	JP	4/16/2004 (3/30/1993)	Converting method for instruction stream Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP3544332 (JP2000-007260)	JP	4/16/2004 (3/30/1993)	Computer System Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP3544333 (JP2000-007263)	JP	4/16/2004 (3/30/1993)	Computer System Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP3544334(JP2000-007264)	JP	4/16/2004(3/30/1993)	Converting method for instruction streamCoon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP3544335 (JP2000-007265)	JP	4/16/2004 (3/30/1993)	Alignment system for composite instruction stream Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP3547052 (JP05-517306)	JP	4/23/2004 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
KR10-0343530 (KR10-1994-0703361)	KR	6/25/2002 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
5,546,552 (08/440,225)	US	8/13/1996 (5/12/1995)	Method for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le T.; Wang, Johannes
5,619,666 (08/460,272)	US	4/8/1997 (6/2/1995)	System for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
5,983,334 (08/784,339)	US	11/9/1999 (1/16/1997)	Superscalar microprocessor for out-of-order and concurrently executing at least two RISC instructions translating from in-order CISC instructions Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
6,263,423 (09/401,860)	US	7/17/2001 (9/22/1999)	System and method for translating non-native instructions to native instructions for processing on a Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
KR10-0371929 (KR10-2001-7005744)	KR	1/28/2003 (5/7/2001)	System and method for translating non-native instructions to native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
6,954,847 (10/061,295)	US	10/11/2005 (2/4/2002)	System and method for translating non-native instructions to native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
7,343,473 (11/167,289)	US	3/11/2008 (6/28/2005)	System and method for translating non-native instructions to native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
12/046,318	US	3/11/2008	System and method for translating non-native instructions to native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
6,990,658 (09/417,980)	US	1/24/2006 (10/13/1999)	Method for translating instructions in a speculative microprocessor featuring committing state Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
CA2379997 (CA2379997)	CA	8/19/2008 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
CNZL00814345.5(CN00814345.5)	CN	7/7/2004(9/6/2000)	A method for translating instructions in a speculative microprocessorTorvalds, Linus; Bedichek,Robert; Johnson, Stephen
DE60028808.0 (DE60028808.0)	DE	3/14/2007 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
FR1230594 (FR00963330.6)	FR	6/14/2006 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
GB1230594 (GB00963330.6)	GB	6/14/2006 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
CY1230594 (CY00963330.6)	CY	9/6/2000	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
JP3626139 (JP2001-530698)	JP	12/10/2004 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
KR10-0576389 (KR10-2002-7004734)	KR	4/26/2006 (4/12/2002)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
11/069,497	US	2/28/2005	a method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
7,012,461 (10/747,022)	US	3/14/2006 (12/23/2003)	Stabilization component for a substrate potential regulation circuit Chen, Tien-Min; Fu,Robert
11/358,482	US	2/21/2006	STABILIZATION COMPONENT FOR A SUBSTRATE POTENTIAL REGULATION CIRCUIT Tien-Min Chen; Robert Fu
7,039,792 (10/607,480)	US	5/2/2006 (6/25/2003)	Method and system for implementing a floating point compare using recorded flags Anvin, H. Peter
7,049,699 (10/712,129)	US	5/23/2006 (11/12/2003)	Low RC structures for routing body-bias voltage Masleid,Robert Paul; Burr,James B.; Pelham, Michael
7,062,631 (10/623,021)	US	6/13/2006 (7/17/2003)	Method and system for enforcing consistent per-physical page cacheability attributes Klaiber, Alexander C.; Dunn, David

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/314,494	US	12/20/2005	a data structure for enforcing consistent per-physical page cacheability attributes Klaiber, Alexander C.; Dunn, David
7,071,747 (10/869,012)	US	7/4/2006 (6/15/2004)	Inverting zipper repeater circuit Masleid,Robert P.
11/435,692	US	5/16/2006	Inverting zipper repeater circuit Masleid,Robert P.
7,089,397 (10/613,801)	US	8/8/2006 (7/3/2003)	Method and system for caching attribute data for matching attributes with physical addresses Anvin, H. Peter; Rozas, Guillermo J.; Klaiber, Alexander; Banning, John P.
7,380,098 (11/454,355)	US	5/27/2008 (6/16/2006)	Method and system for caching attribute data for matching attributes with physical addresses Anvin, H. Peter; Rozas, Guillermo J.; Klaiber, Alexander; Banning, John P.
12/127,648	US	5/27/2008	Method and system for caching attribute data for matching attributes with physical addresses Anvin, H. Peter; Rozas, Guillermo J.; Klaiber, Alexander; Banning, John P.
7,089,404(09/332,338)	US	8/8/2006(6/14/1999)	Method and apparatus for enhancing scheduling in an advanced microprocessorRozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
CA2377164 (CA2377164)	CA	9/25/2007 (6/12/2000)	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
CNZL00808883.7 (CN00808883.7)	CN	5/18/2005 (6/12/2000)	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
EP00944658.4	EP	6/12/2000	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
KR10-0758367 (KR10-2001-7016123)	KR	9/6/2007 (12/14/2001)	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
10/783,473	US	2/20/2004	Method and Apparatus for Enhancing Scheduling in an Advanced Microprocessor D'Souza, Godfrey; Rozas, Guillermo; Price, Charles ; Serris, Paul
JP3872809 (JP2005-334136)	JP	10/27/2006 (11/18/2005)	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
11/400,631	US		Systems and methods fro reordering processor instructions Brian Holscher; Guillermo J Rozas; James Van Zoeren; David Dunn
7,100,061 (09/484,516)	US	8/29/2006 (1/18/2000)	Adaptive power control Halepete, Sameer; Anvin, H. Peter; Chen, Zongjian; D'Souza, Godfrey P.; Fleischmann, Marc; Klayman, Keith; Lawrence, Thomas; Read, Andrew
11/411,309	US	4/25/2006	Adaptive power control Halepete, Sameer; Anvin, H. Peter; Chen, Zongjian; D'Souza, Godfrey P.; Fleischmann, Marc; Klayman, Keith; Lawrence, Thomas; Read, Andrew
95/000,243	US	6/13/2007	Adaptive power control Halepete, Sameer; Anvin, H. Peter; Chen, Zongjian; D'Souza, Godfrey P.;

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Fleischmann, Marc; Klayman, Keith; Lawrence, Thomas; Read, Andrew
7,118,273 (10/411,955)	US	10/10/2006 (4/10/2003)	System for on-chip temperature measurement in integrated circuits Schnaitter, William N.
7,108,420 (10/961,311)	US	9/19/2006 (10/7/2004)	System for on-chip temperature measurement in integrated circuits Schnaitter, William N.
11/524,526	US	9/19/2006	System for on-chip temperature measurement in integrated circuits William N Schnaitter
7,111,146 (10/607,934)	US	9/19/2006 (6/27/2003)	METHOD AND SYSTEM FOR PROVIDING HARDWARE SUPPORT FOR MEMORY PROTECTION AND VIRTUAL MEMORY ADDRESS TRANSLATION FOR A VIRTUAL MACHINE Anvin, H. Peter
11/500,575	US	8/7/2006	METHOD AND SYSTEM FOR PROVIDING HARDWARE SUPPORT FOR MEMORY PROTECTION AND VIRTUAL MEMORY ADDRESS TRANSLATION FOR A VIRTUAL MACHINEAnvin, H. Peter
7,336,103 (10/864,271)	US	2/26/2008 (6/8/2004)	STACKED INVERTER DELAY CHAIN Masleid, Robert P.; Burr, James B.
7,304,503 (10/879,645)	US	12/4/2007 (6/28/2004)	REPEATER CIRCUIT WITH HIGH PERFORMANCE REPEATER MODE AND NORMAL REPEATER MODE, WHEREIN HIGH PERFORMANCE REPEATER MODE HAS FAST RESET CAPABILITY Masleid,Robert Paul; Dholabhai, Vatsal
TW094118970	TW	6/8/2005	Repeater circuit with high performance repeater mode and normal repeater mode, wherein high performance repeater mode has fast reset capability Masleid,Robert Paul; Dholabhai, Vatsal
CN0580018670.5	CN	6/8/2005	Repeater circuit with high performance and normal repeater modes and reset capability Masleid Robert Paul; Dholabhai Vatsal
HK07106433.5	HK	6/14/2007	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES AND RESET CAPABILITY MASLEID, Robert, Paul; Dholabhai, Vatsal
JP2007-527698	JP	6/8/2005	Repeater circuit with high performance repeater mode and normal repeater mode, wherein high performance repeater mode has fast reset capability Masleid Robert Paul; DHOLABHAI, Vatsal
11/999,293	US	12/4/2007	REPEATER CIRCUIT WITH HIGH PERFORMANCE REPEATER MODE AND NORMAL REPEATER MODE, WHEREIN HIGH PERFORMANCE REPEATER MODE HAS FAST RESET CAPABILITY Masleid,Robert Paul; Dholabhai, Vatsal
7,119,580 (10/879,879)	US	10/10/2006 (6/28/2004)	REPEATER CIRCUIT WITH HIGH PERFORMANCE REPEATER MODE AND NORMAL REPEATER MODE Masleid,Robert Paul; Dholabhai, Vatsal; Stoiber, Steven Thomas; Singh, Gurmeet
TW094118968	TW	6/8/2005	Repeater circuit with high performance repeater mode and normal repeater mode Masleid,Robert Paul; Dholabhai, Vatsal; Stoiber, Steven Thomas;

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Singh, Gurmeet
CN0580018680.9	CN	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES Masleid Robert Paul;Dholabhai Vatsal;Stoiber Steven Thomas;Singh Gurmeet
HK07106434.4	HK	6/14/2007	Repeater circuit with high performance repeater mode and normal repeater mode Masleid,Robert Paul; Dholabhai, Vatsal; Stoiber, Steven Thomas; Singh, Gurmeet
JP2007-527699	JP	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES Inventorship not available
TW094118969	TW	6/8/2005	Repeater circuit with high performance repeater mode and normal repeater mode Masleid,Robert Paul; Dholabhai, Vatsal; Stoiber, Steven Thomas; Singh, Gurmeet
7,142,018 (10/879,807)	US	11/28/2006 (6/28/2004)	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS Masleid,Robert Paul; Kowalczyk, Andre
TW094118971	TW	6/8/2005	Circuits and methods for detecting and assisting wire transitionsMasleid,Robert Paul; Kowalczyk, Andre
11/473,608	US	6/22/2006	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS Masleid,Robert Paul; Kowalczyk, Andre
7,295,041 (11/005,762)	US	11/13/2007 (12/6/2004)	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS Masleid,Robert Paul; Kowalczyk, Andre
7,375,556 (11/171,845)	US	5/20/2008 (6/30/2005)	ADVANCED REPEATER UTILIZING SIGNAL DISTRIBUTION DELAY Scott Pitkethly; Robert Paul Masleid;
7,405,597 (11/172,013)	US	7/29/2008 (6/30/2005)	ADVANCED REPEATER WITH DUTY CYCLE ADJUSTMENT Scott Pitkethly
12/181,221	US	7/28/2008	Inventorship not available
12/124,136	US	5/20/2008	Advanced Repeater Utilizing Signal Distribution Delay Scott Pitkethly; Masleid,Robert Paul;
CN0580018676.2	CN	6/8/2005	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS Masleid Robert Paul;Dholabhai Vatsal
HK07106436.2	HK	6/14/2007	Circuits and methods for detecting and assisting wire transitions Masleid,Robert Paul; Kowalczyk, Andre

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP2007-527735	JP	6/8/2005	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS Inventorship not available
7,173,455 (10/879,808)	US	2/6/2007 (6/28/2004)	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Masleid,Robert Paul; Dholabhai, Vatsal; Klingner, Christian
CN0580018677.7	CN	6/8/2005	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Masleid Robert Paul; Dholabhai Vatsal; Klingner Christian
HK07106435.3	HK	6/14/2007	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF MASLEID, Robert, Paul DHOLABHAI, Vatsal; KLINGNER, Christian
JP2007-527736	JP	6/8/2005	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Inventorship not available
11/703,323	US	2/6/2007	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Masleid Robert Paul; Dholabhai Vatsal; Klingner Christian
11/021,221	US	12/23/2004	CONFIGURABLE DELAY CHAIN WITH SWITCHING CONTROL FOR TAIL DELAY ELEMENTS Robert Paul Masleid
11/021,222	US	12/23/2004	CONFIGURABLE TAPERED DELAY CHAIN WITH MULTIPLE SIZES OF DELAY ELEMENTSRobert Paul Masleid
11/021,632	US	12/23/2004	POWER EFFICIENT MULTIPLEXER Robert Paul Masleid
7,330,054 (11/021,633)	US	2/12/2008 (12/23/2004)	LEAKAGE EFFICIENT ANTI-GLITCH FILTER Masleid,Robert Paul
7,310,008 (11/020,746)	US	12/18/2007 (12/23/2004)	CONFIGURABLE DELAY CHAIN WITH STACKED INVERTER DELAY ELEMENTS Masleid,Robert Paul
12/002,988	US	12/18/2007	CONFIGURABLE DELAY CHAIN WITH STACKED INVERTER DELAY ELEMENTS Masleid,Robert Paul
7,332,931 (11/021,197)	US	2/19/2008 (12/23/2004)	LEAKAGE EFFICIENT ANTI-GLITCH FILTER WITH VARIABLE DELAY STAGES Masleid,Robert Paul
12/033,712	US	2/19/2008	LEAKAGE EFFICIENT ANTI-GLITCH FILTER Masleid,Robert Paul
12/037,884	US	2/26/2008	STACKED INVERTER DELAY CHAIN Masleid,Robert Paul; James B.Burr
7,129,771 (10/747,015)	US	10/31/2006 (12/23/2003)	SERVO LOOP FOR WELL BIAS VOLTAGE SOURCE Chen, Tien-Min

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,362,165 (11/591,431)	US	4/22/2008 (10/31/2006)	SERVO LOOP FOR WELL BIAS VOLTAGE SOURCE Tien-Min Chen
12/107,733	US	4/22/2008	SERVO LOOP FOR WELL BIAS VOLTAGE SOURCE Tien-Min Chen
7,149,851 (10/646,461)	US	12/12/2006 (8/21/2003)	METHOD AND SYSTEM FOR CONSERVATIVELY MANAGING STORE CAPACITY AVAILABLE TO A PROCESSOR ISSUING STORES Rozas, Guillermo; Klaiber, Alexander; Dunn, David; Serris, Paul; Shah, Lacky
11/638,236	US	12/12/2006	METHOD AND SYSTEM FOR CONSERVATIVELY MANAGING STORE CAPACITY AVAILABLE TO A PROCESSOR ISSUING STORES Rozas, Guillermo; Klaiber, Alexander; Dunn, David; Serris, Paul; Shah, Lacky
7,149,872 (10/629,031)	US	12/12/2006 (7/28/2003)	SYSTEM AND METHOD FOR IDENTIFYING TLB ENTRIES ASSOCIATED WITH A PHYSICAL ADDRESS OF A SPECIFIED RANGE Rozas, Guillermo; Klaiber, Alexander; Anvin, H. Peter; Dunn, David
7,380,096 (11/449,950)	US	5/27/2008 (6/8/2006)	SYSTEM AND METHOD FOR IDENTIFYING TLB ENTRIES ASSOCIATED WITH A PHYSICAL ADDRESS OF A SPECIFIED RANGE Rozas, Guillermo; Klaiber, Alexander; Anvin, H. Peter; Dunn, David
12/127,768	US	5/27/2008	a system and method for identifying tlb entries associated with a physical address of a specified range Guillermo Rozas; Alexander Klaiber; H. Peter Anvin; David Dunn
7,151,417 (10/870,754)	US	12/19/2006 (6/16/2004)	SYSTEM AND METHOD FOR CHARACTERIZING A POTENTIAL DISTRIBUTION Suzuki, Shingo
11/642,187	US	12/19/2006	SYSTEM AND METHOD FOR CHARACTERIZING A POTENTIAL DISTRIBUTIONShingo Suzuki
7,174,528 (10/683,961)	US	2/6/2007 (10/10/2003)	METHOD AND APPARATUS FOR OPTIMIZING BODY BIAS CONNECTIONS IN CMOS CIRCUITS USING A DEEP N-WELL GRID STRUCTURE Burr,James B.; Schnaitter, William N.
11/649,443	US	1/3/2007	method and apparatus for optivizong body bias connections in cmos circuits using a deep n-well grid structure James B Burr; William Schnaitter
7,203,932 (10/335,459)	US	4/10/2007 (12/30/2002)	METHOD AND SYSTEM FOR USING IDIOM RECOGNITION DURING A SOFTWARE TRANSLATION PROCESS Gaudet, Dean; O'Clair, Brian
7,212,064 (11/056,549)	US	5/1/2007 (2/11/2005)	METHODS AND SYSTEMS FOR MEASURING TEMPERATURE USING DIGITAL SIGNALS Schnaitter, William N.
7,217,962 (11/171,673)	US	5/15/2007 (6/30/2005)	WIRE MESH PATTERNS FOR SEMICONDUCTOR DEVICES Masleid,Robert Paul

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7,225,299 (10/622,028)	US	5/29/2007 (7/16/2003)	SUPPORTING SPECULATIVE MODIFICATION IN A DATA CACHE Rozas, Guillermo; Klaiber, Alexander; Dunn, David; Serris, Paul; Shah, Lacky
11/807,629	US	5/29/2007	SUPPORTING SPECULATIVE MODIFICATION IS A DATA CACHE Guillermo Rozas; Alexander Klaiber; David Dunn; Paul Serris; Lacky Shah
7,227,397 (11/096,770)	US	6/5/2007 (3/31/2005)	SYSTEM, METHOD AND CIRCUITS FOR GENERATING A SIGNAL Schnaitter, William
11/540,387	US	9/29/2006	SIGNAL GENERATOR WITH OUTPUT FREQUENCY GREATER THAN THE OSCILLATOR FREQUENCY William N. Schnaitter; Guillermo J. Rozas
7,228,242 (10/334,748)	US	6/5/2007 (12/31/2002)	ADAPTIVE POWER CONTROL BASED ON PRE PACKAGE CHARACTERIZATION OF INTEGRATED CIRCUITS Read, Andrew; Wing, Malcolm; Kordus, Louis C.; Stewart, Thomas E.
JP2004-565787	JP	12/29/2003	Adaptive power control based on pre package characterization of integrated circuits Inventorship not available
11/810,516	US	6/5/2007	adaptive power control based on pre package characterization of integrated circuits Andrew Read; Malcolm Wing; Louis C. Kordus; Thomas E Stewart
7,249,246 (10/600,989)	US	7/24/2007 (6/20/2003)	METHODS AND SYSTEMS FOR MAINTAINING INFORMATION FOR LOCATING NON-NATIVE PROCESSOR INSTRUCTIONS WHEN EXECUTING NATIVE PROCESSOR INSTRUCTIONS Banning, John P.; Anvin, H. Peter; Rozas, Guillermo J.
7,256,634 (11/176,918)	US	8/14/2007 (7/6/2005)	ELASTIC PIPELINE LATCH WITH A SAFE MODE Masleid,Robert Paul
TW095124306	TW	7/4/2006	ELASTIC PIPELINE LATCH Masleid,Robert Paul
11/893,221	US	8/14/2007	ELASTIC PIPELINE LATCH WITH A SAFE MODERobert Paul Masleid
7,260,731 (09/694,433)	US	8/21/2007 (10/23/2000)	SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR Read, Andrew; Halepete, Sameer; Klayman, Keith
11/894,991	US	8/21/2007	SAVING POWER WHEN IN OR TRANSITIONING TO A STATIC MODE OF A PROCESSOR Read, Andrew; Halepete, Sameer; Klayman, Keith
7,305,647 (11/193,723)	US	12/4/2007 (7/28/2005)	USING STANDARD PATTERN TILES AND CUSTOM PATTERN TILES TO GENERATE A SEMICONDUCTOR DESIGN LAYOUT HAVING A DEEP WELL STRUCTURE FOR ROUTING BODY-BIAS VOLTAGE Pelham, Michael
11/999,279	US	12/4/2007	USING STANDARD PATTERN TILES AND CUSTOM PATTERN TILES TO GENERATE A SEMICONDUCTOR DESIGN LAYOUT HAVING A DEEP WELL STRUCTURE FOR ROUTING BODY-BIAS VOLTAGE Pelham, Michael

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,310,723 (10/406,022)	US	12/18/2007 (4/2/2003)	METHODS AND SYSTEMS EMPLOYING A FLAG FOR DEFERRING EXCEPTION HANDLING TO A COMMIT OR ROLLBACK POINT Rozas, Guillermo J.; Klaiber, Alexander
12/002,983	US	12/18/2007	methods and systems that defer exception handling Rozas, Guillermo J.; Klaiber, Alexander
7,313,779 (10/964,409)	US	12/25/2007 (10/12/2004)	METHOD AND SYSTEM FOR TILING A BIAS DESIGN TO FACILITATE EFFICIENT DESIGN RULE CHECKING Masleid,Robert Paul; Stoiber, Steven T.
12/005,018	US	12/20/2007	Tiling bias design and design rule checking Masleid,Robert Paul; Stoiber, Steven T.
5,493,687 (07/726,773)	US	2/20/1996 (7/8/1991)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
JP3607701 (JP05-502403)	JP	10/15/2004 (7/8/1992)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
JP3864160 (JP2004-010368)	JP	10/6/2006 ()	RISC microprocessor architecture implementing multiple typed resistor set Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
JP3880056 (JP2004-010369)	JP	11/17/2006 (1/19/2004)	RISC microprocessor architecture employing multiple register set Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
DE69230057.0 (DE69230057.0)	DE	9/29/1999 (7/8/1992)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
FR0547216 (FR92915765.9)	FR	9/29/1999 (7/8/1992)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
GB0547216 (GB92915765.9)	GB	9/29/1999 (7/8/1992)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
KR10-0294964(KR10-1993-0700692)	KR	4/23/2001(7/8/1992)	RISC microprocessor architecture implementing multiple typed register setsGarg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
5,560,035 (08/465,239)	US	9/24/1996 (6/5/1995)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
5,682,546 (08/665,845)	US	10/28/1997 (6/19/1996)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le Trong; Chen, Sho Long
5,838,986 (08/937,361)	US	11/17/1998 (9/25/1997)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le Trong; Chen, Sho Long
6,044,449 (09/188,708)	US	3/28/2000 (11/10/1998)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le Trong; Chen, Sho Long
6,249,856 (09/480,136)	US	6/19/2001 (1/10/2000)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le Trong; Chen, Sho Long

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/060,086	US	1/31/2002	RISC microprocessor architecture implementing multiple typed register sets Derek J. Lentz; Le Trong Nguyen; Sanjiv Garg; Sho Long Chen
11/651,009	US	1/9/2007	RISC microprocessor architecture implementing multiple typed register sets Derek J. Lentz; Le Trong Nguyen; Sanjiv Garg; Sho Long Chen
7,334,198 (10/334,638)	US	2/19/2008 (12/31/2002)	Software controlled transistor body bias Ditzel, David R.; Burr,James B.
12/033,832	US	2/19/2008	Software controlled transistor body bias Ditzel, David R.; Burr,James B.
CN0380109985.1	CN	12/29/2003	Circuit Management Ditzel, David R.; Burr,James B.
HK1089826 (HK06110063.5)	HK	(12/29/2003)	Circuit Management Ditzel, David R.; Burr,James B.
JP2004-565788	JP	12/29/2003	Software controlled body bias Ditzel, David R.; Burr,James B.
11/169,403	US	6/28/2005	Method and system for providing trusted access to a JTAG scan interface in a microprocessor David Dunn; Keith Klayman
7,334,173 (11/241,104)	US	2/19/2008 (9/29/2005)	Method and system for protecting processors from unauthorized debug access Morgan, Andrew; Dunn, David
TW095136358	TW	9/29/2006	Securing scan test architecture Morgan, Andrew; Dunn, David
12/033,864	US	2/19/2008	Method and system for protecting processors from unauthorized debug access Morgan, Andrew; Dunn, David
7,330,080 (10/981,964)	US	2/12/2008 (11/4/2004)	Ring based impedance control of an output driver Stoiber, Steven T.; Siu, Stuart
11/986,337	US	11/20/2007	Ring based impedance control of an output driver Stoiber, Steven T.; Siu, Stuart
7,330,959(10/830,921)	US	2/12/2008(4/23/2004)	Use of MTRR and page attribute table to support multiple byte order formats in a computer systemAnvin, H. Peter
12/030,149	US	2/12/2008	Supporting multiple byte order formats in a computer system Anvin, H. Peter
7,376,798 (11/102,127)	US	5/20/2008 (4/7/2005)	Memory management methods and systems that support cache consistency Rozas, Guillermo J.
12/121,531	US	5/15/2008	Memory management methods and systems that support cache consistency Rozas, Guillermo J.
7,388,260 (10/816,269)	US	6/17/2008 (3/31/2004)	Structure for spanning gap in body-bias voltage routing structure Robert Masleid; James B Burr; Michael Pelham

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
12/140,197	US	6/16/2008	Structure for spanning gap in body-bias voltage routing structure Robert Masleid; James B Burr; Michael Pelham
7,394,681 (11/273,897)	US	7/1/2008 (11/14/2005)	Column select multiplexer circuit for a domino random access memory array Robert Masleid
12/165,432	US	6/30/2008	Column select multiplexer circuit for a domino random access memory array Robert Masleid
7,414,485 (11/322,595)	US	8/19/2008 (12/30/2005)	Circuits, systems and methods relating to dynamic ring oscillators Robert P. Masleid
12/194,504	US	8/19/2008	Dynamic ring oscillators Robert P. Masleid
09/417,332	US	10/13/1999	Method for integration of interpretation and translation in a microprocessor BEDICHEK, ROBERT; TORVALDS, LINUS; KEPPEL, DAVID
10/273,681	US	10/17/2002	Apparatus for controlling semiconductor chip characteristics Godfrey P D'Souza; Keith Klayman
10/334,921	US	12/31/2002	a method and system for securing processor information for export and retrieval Andrew Morgan; Guillermo J Rozas; Dean Gaude
7,444,471 (10/335,405)	US	10/28/2008 (12/30/2002)	Method and system for using external storage to amortize CPU cycle utilization Brian O'Clair; Dean Gaudet
12/259,262	US	10/27/2008	Method and system for using external storage to amortize CPU cycle utilization Brian O'Clair; Dean Gaudet
10/411,168	US	4/9/2003	SYSTEM AND METHOD FOR HANDLING DIRECT MEMORY ACCESSES Alexander C. Klaiber; Guillermo J. Rozas; David A. Dunn
11/400,368	US	5/22/2006	SYSTEM AND METHOD FOR HANDLING DIRECT MEMORY ACCESSES Alexander C. Klaiber; Guillermo J. Rozas; David A. Dunn
11/102,171	US	4/7/2005	COHERENCE DE-COUPLING BUFFER Guillermo Rozas
11/439,361	US	5/22/2006	A System and Method for Handling Direct Memory AccessesKlaiber, Alexander;Rozas, Guillermo;Dunn, David
10/609,158	US	6/27/2003	METHOD AND SYSTEM FOR SUPPORTING INPUT/OUTPUT FOR A VIRTUAL MACHINE Nathan Laredo; Linus Torvalds
7,451,300 (10/620,862)	US	11/11/2008 (7/15/2003)	EXPLICIT CONTROL OF SPECULATION H. Peter Anvin; David Dunn
12/268,304	US	11/10/2008	EXPLICIT CONTROL OF SPECULATION H. Peter Anvin; David Dunn

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/623,101	US	7/18/2003	Method and system for using one or more address bits and an instruction to increase an instruction set Bill Rozas, Alexander Klaiber, Eric Hao
10/607,638	US	6/27/2003	METHOD AND SYSTEM FOR IMPLEMENTING HARDWARE SUPPORT FOR VIRTUAL MEMORY ADDRESS TRANSLATION FOR A VIRTUAL MACHINE H. Peter Anvin
10/672,790	US	9/26/2003	SYSTEM AND METHOD OF INSTRUCTION MODIFICATION John Banning; Eric Hao; Brett Coon
10/672,796	US	9/26/2003	SYSTEM WITH SESCURE CRYPTOGRAPHIC CAPABILITIES USING A HARDWARE SPECIFIC DIGITAL SECRET Andrew Morgan; H. Peter Anvin
10/712,522	US	11/12/2003	Variable outlet charge pump circuit Robert Fu; Tien-Min Chen
10/712,523	US	11/12/2003	System for substrate potential regulation during power-up in integrated circuits Robert Fu; Tien-Min Chen
10/716,320	US	11/17/2003	a method and system for automatic calibrating intra-cycle timing relationship for sampling signals for an integrated circuit device Guillermo J Rozas
10/719,879	US	11/20/2003	ARCHITECTURE, SYSTEM, AND METHOD FOR OPERATING ON ENCRYPTED AND/OR HIDDEN INFORMATION Richard Johnson; Andrew Morgan; H. Peter Anvin; Linus Torvalds
10/740,939	US	12/18/2003	METHOD AND SYSTEM FOR SECURING PROCESSOR INTERNATL KEY INFORMATION FOR EXPORT AND RETRIEVAL Andrew Morgan; Dean Gaudet
10/747,016	US	12/23/2003	Feedback-controlled Body-bias Voltage Source Chen, Tien-Min
10/772,029	US	2/3/2004	METHOD FOR GENERATING A DEEP N-WELL PATTERN FOR AN INTEGRATED CIRCUIT DESGIN Michael Pelham; James B. Burr
10/808,225	US	3/23/3004	DEEP N-WELL CAPACITOR Robert P. Masleid; James B. Burr
10/810,196	US	3/25/2004	REQUEST TRACKING DATA PREFETCHER APPARATUSBrian Holscher;Dean Gaudet
10/874,407	US	6/22/2004	adaptive voltage control Steven Kawasumi; Eric Sheng
10/874,772	US	6/22/2004	ADAPTIVE CONTROL OF OPERATING AND BODY BIAS VOLTAGES Sheng, Eric; Ward, Matthew

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/956,220	US	9/30/2004	METHOD AND APPARATUS FOR PROTECTING CRYPTOGRAPHIC KEYS IN USER SPACE Andrew Morgan
10/964,448	US	10/12/2004	METHOD AND SYSTEM FOR AUTOMATED SCHEMATIC DIAGRAM CONVERSION TO SUPPORT SEMICONDUCTOR BODY-BIAS DESIGNS Steven T. Stoiber
11/018,880	US	12/20/2004	METHOD AND SYSTEM FOR CONFIGURABLE CONTACTS FOR IMPLEMENTING DIFFERENT BIAS DESIGNS OF AN INTEGRATED CIRCUIT DEVICE Robert Paul Masleid; Steven T. Stoiber
11/096,922	US	3/31/2005	MEMORY PROTECTION AND ADDRESS TRANSLATION HARDWARE SUPPORT FOR VIRTUAL MACHINES Guillermo J. Rozas; Nathan Laredo
11/394,521	US	3/31/2005	HARDWARE SUPPORT FOR VIRTUAL MACHINE AND OPERATING SYSTEM CONTEXT SWITCHING IN TRANSLATION Guillermo Rozas; Alex Klaiber
11/097,421	US	3/31/2005	A code translation verification system and method Markus Kaltenbach
11/102,289	US	4/7/2005	COHERENCE MEMORY ROZAS, GUILLERMO
11/102,538	US	4/7/2005	MAINTAINING INSTRUCTION COHERENCY IN A TRANSLATION-BASED COMPUTER SYSTEM ARCHITECTURE Guillermo Rozas; David Dunn
11/132,052	US	5/17/2005	LEVEL SHIFTER FOR NOISE AND LEAKAGE SUPPRESSION Venkata Kottapalli
11/169,404	US	6/28/2005	MULTI-THREADING BASED ON ROLLBACK Guillermo J. Rozas; Michael R. Neilly
11/296,591	US	12/6/2005	A secure memory access system and method Christian Ludloff, Kurt Daverman, Andrew Morgan
11/322,896	US	12/30/2005	Circuitys, systems and methods relating to a dynamic dual domino ring oscillator Robert P Masleid
11/393,555	US	3/29/2006	CONVERSION OF AN SOI DESIGN LAYOUT TO A BULK DESIGN LAYOUT David R. Ditzel; James B. Burr; Robert P. Masleid
11/395,017	US	3/31/2006	Multi-write memory circuit with a data input and a clock input Robert P Masleid
11/396,114	US	3/31/2006	Multi-Write Memory Circuit with Multiple Data InputsRobert P. Masleid;Scott Pitkethly
TW096111335	TW	3/30/2007	Memory circuit Robert P Masleid

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP07754447.6	EP	3/30/2007	Memory circuit Robert P Masleid
11/395,627	US	3/31/2006	Multi-portioned instruction memory John P. Banning; Guillermo J. Rozas
EP07754446.8	EP	3/30/2007	A multi-portioned instruction memory John P. Banning; Guillermo J. Rozas
11/395,710	US	3/31/2006	TECHNIQUES FOR DETECTING AND CORRECTING ERRORS IN A MEMORY DEVICE Guillermo Rozas
11/479,486	US	6/29/2006	PROCESSOR MODIFICATIONS TO INCREASE COMPUTER SYSTEM SECURITY David Dunn
11/479,618	US	6/30/2006	Cross Point Switch Robert P. Masleid, Scott Pitkethly
11/479,630	US	6/30/2006	DUAL PORTED REPLICATED DATA CACHE Guillermo Rozas; Alex Klaiber; Robert P. Masleid
11/479,703	US	6/29/2006	Processor and northbridge modifications to increase computer system security David A Dunn
11/480,107	US	6/30/2006	a triple latch flip flop system and method Scott Pitkethly, Robert P Masleid
11/529,865	US	9/29/2006	DYNAMIC CHIP CONTROL Kleanthes G. Koniaris; James B. Burr; Mark Hennecke
11/529,972	US	9/29/2006	Raised source/drain with super steep retrograde channel James B Burr; Archis Bagchi; Jawad Nasrullah
11/540,117	US	9/29/2006	METHODS AND SYSTEMS FOR DYNAMICALLY CHANGING DEVICE OPERATING CONDITIONS James B. Burr; Kleanthes G. Koniaris
11/540,766	US	9/29/2006	PROCESSING BYPASS REGISTER FILE SYSTEM AND METHOD Parag Gupta; Alexander Klaiber; James Van Zoeren
7,478,226 (11/540,789)	US	1/13/2009 (9/29/2006)	processing bypass directory tracking system and method Alexander Klaiber; Guillermo Rozas
12/353,064	US		processing bypass directory tracking system and method Alexander Klaiber; Guillermo Rozas
11/583,463	US	10/18/2006	CACHING TECHNIQUES Guillermo Rozas; Alexander Klaiber; Robert P. Masleid; John Banning; James Van Zoeren; Paul Serris

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/639,603	US	12/15/2006	System and methods for determining device temperature William N. Schnaitter
11/644,224	US	12/22/2006	system management mode code modifications to increase computer system securityDavid A Dunn
11/652,242	US	1/10/2007	METHOD FOR PROVIDING HARDWARE SUPPORT FOR A VIRTUALLY INDEXED AND TAGGED CACHE Alexander Klaiber; Guillermo Rozas
11/786,336	US	4/10/2007	HISTORY BASED PIPELINED BRANCH PREDICTION David D. Dunn; John P. Banning
10/334,919	US	12/31/2002	Adaptive power control based on post package characterization of integrated circuits Tom Stewart
JP2004-565752	JP	12/29/2003	Adaptive power control based on post package characterization of integrated circuits Tom Stewart
10/990,885	US	11/16/2004	Systems and methods for voltage distribution via epitaxial layers Robert P. Masleid
10/990,886	US	11/16/2004	Systems and methods for voltage distribution via multiple epitaxial layers Robert Paul Masleid
TW094139602	TW	11/11/2005	Systems and methods for voltage distribution via epitaxial layers Robert P. Masleid
TW094139603	TW	11/11/2005	Systems and methods for voltage distribution via multiple epitaxial layers Robert Paul Masleid
11/053,081	US	2/7/2005	System and method for providing a secure boot architecture Andrew Morgan; Christian Ludloff; Guillermo Rozas
TW095103879	TW	2/6/2006	System and method for providing a secure boot architecture Guillermo Rozas; Andrew Morgan; Christian Ludloff
CN0680008879.8	CN	2/3/2006	System and method for providing a secure boot architecture Guillermo Rozas; Andrew Morgan; Christian Ludloff
11/053,080	US	2/7/2005	Method and system for validating a computer system Guillermo J. Rozas
TW095103880	TW	2/6/2006	Method and system for validating a computer system Guillermo J. Rozas
CN0680011416.7	CN	2/3/2006	Method and system for validating a computer system Guillermo J. Rozas
11/096,354	US	3/31/2005	Method and system for elastic signal pipelining Guillermo J. Rozas; Robert P. Masleid
TW095111222	TW	3/30/2006	A system and method for elastic signal pipelining Guillermo J. Rozas; Robert P. Masleid

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/171,695	US	6/30/2005	Scannable dynamic circuit latch Robert Paul Masleid; Jose Sousa; Venkata Kottapalli
TW095123301	TW	6/28/2006	A dynamic circuit latch Robert Paul Masleid; Jose Sousa; Venkata Kottapalli
11/172,084	US	6/30/2005	Lower minimum retention voltage storage elements James B. Burr; Robert P. Masleid; Kleanthes G. Koniaris
TW095123636	TW	6/29/2006	Storage element circuitJames B. Burr; Robert P. Masleid; Kleanthes G. Koniaris
11/171,668	US	6/30/2005	Clock signal distribution system and method Scott Pitkethly
TW095123145	TW	6/27/2006	Clock signal distribution system and method Scott Pitkethly
11/274,098	US	11/14/2005	NON-RECTILINEAR ROUTING IN RECTILINEAR MESH Robert P. Masleid
11/477,970	US	6/28/2006	DOUBLE DIAMOND CLOCK AND POWER DISTRIBUTION Robert P. Masleid; Scott Pitkethly
11/479,616	US	6/30/2006	Clock signal distribution system and method Scott Pitkethly; Robert P Masleid
6,968,469 (09/595,198)	US	11/22/2005 (6/16/2000)	Instant Suspend to Ram Fleischmann, Marc; Anvin, H. Peter
11/201,624	US	8/10/2005	Instant suspend to RAM Marc Fleischmann; H. Peter Anvin
12/136,679	US	6/10/2008	System and method for saving and restoring a processor state without executing any instructions from a first instruction set Marc Fleischmann; H. Peter Anvin

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceedings brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

for past, current, and future infringement;

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h) (but excluding royalties and payments under, and any rights (other than the causes of action and other rights identified in (h) above) resulting from breach of contract with respect to, any agreement existing as of the date of this Assignment); and

(j) any other rights with respect to the Patents granted to Assignee by any prior owner of the Patents, and all claims or causes of action of Assignee relating to the Patents against any prior owner of the Patents.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at San Jose, California on January 28, 2009.

ASSIGNOR:

Transmeta LLC

BY: NOVAFORA, INC.
ITS: SOLE MEMBER

By: _____
Name: Jodi Pittman
Title: CFO
(Signature MUST be notarized)

STATE OF _____)
) ss.
COUNTY OF _____)

On _____, before me, _____, Notary Public in and for said State, personally appeared _____, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____ (Seal)

ACKNOWLEDGMENT

State of California
County of Santa Clara)

On January 28, 2009 before me, JENNIFER WEI ZHU, Notary Public
(insert name and title of the officer)

personally appeared Jodi Pittman,
who proved to me on the basis of satisfactory evidence to be the person(~~s~~) whose name(~~s~~) is/~~are~~ subscribed to the within instrument and acknowledged to me that ~~he~~/she/~~they~~ executed the same in ~~his~~/her/~~their~~ authorized capacity(ies), and that by ~~his~~/her/~~their~~ signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

ESH JENNIFER WEI ZHU
COMM. #1802394
Notary Public-California
ALAMEDA COUNTY
My Comm. Exp. JULY 9, 2012 ESH

Signature _____ **(Seal)**

Attachment 2, revised

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Transmeta LLC, a Delaware limited liability company with an office at 2460 N. 1st Street, Suite 200, San Jose, CA 95131 (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Intellectual Venture Funding LLC, a Nevada limited liability company, with an address at 502 E. John Street; Carson City, NV 89706 (***"Assignee"***), or its designees, all right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
PCT/US97/014118	WO	8/11/1997	A MEMORY CONTROLLER FOR A MICROPROCESSOR FOR DETECTING A FAILURE OF SPECULATION ON THE PHYSICAL NATURE OF A COMPONENT BEING ADDRESSED KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
EP1002271 (EP97937205.9)	EP	10/29/2008 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
PCT/US98/002673	WO	2/13/1998	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
EP0961972 (EP198905051.3)	EP	9/28/2005 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
PCT/US97/016911	WO	9/22/1997	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
EP1008050 (EP97944366.0)	EP	2/28/1997 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
IE1008050 (IE97944366.0)	IE	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
MC1008050 (MC970944366.0)	MC	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
PT1008050 (PT97944366.0)	PT	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
PCT/US97/012058	WO	7/11/1997	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
PCT/US97/022768	WO	12/12/1997	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
PCT/US97/011616	WO	6/25/1997	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
PCT/US97/014117	WO	8/11/1997	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP97939380.8	EP	8/11/1997	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
07/860,719	US	3/31/1992	Superscalar Risc Instruction Scheduling Sanjiv Garg
PCT/JP93/000375	WO	3/26/1993	Superscalar Risc Instruction Scheduling Sanjiv Garg
08/470,485	US	6/6/1995	Inventorship not available
08/483,893	US	6/7/1995	Inventorship not available
EP0636256 (EP93906834.2)	EP	6/4/1997 (3/26/1993)	Superscalar Risc Instruction Scheduling Sanjiv Garg
JP2000-008147	JP	3/26/1993	Instruction Executing Method Sanjiv Garg
09/906,099	US	7/17/2001	Superscalar RISC instruction schedulingGarg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
11/252,820	US	10/19/2005	Superscalar RISC instruction scheduling Inventors: Le Trong Nguyen; Sanjiv Garg; Johannes Wang; Kevin Ray Iadonato
09/329,352	US	6/10/1999	Inventorship not available
PCT/US00/024697	WO	9/6/2000	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
EP1234277 (EP00961695.4)	EP	6/18/2008 (9/6/2000)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
JP2001-530814	JP	9/6/2000	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
PCT/US00/024651	WO	9/6/2000	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
EP1240582 (EP00960034.7)	EP	10/13/2007 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
PCT/US00/040856	WO	9/6/2000	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
EP1226492 (EP00974084.6)	EP	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
10/464,816	US	6/18/2003	Link pipe system for storage and retrieval of sequences of branch addresses Banning, John; Coon, Brett; Hao, Eric

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/464,870	US	6/18/2003	SOFTWARE DIRECT MEMORY ACCESS Patrick Boyle; David Keppel; Alexander C. Klaiber; Edmund Kelly
PCT/US00/040857	WO	9/6/2000	CONTROLLING INSTRUCTION TRANSLATION USING DYNAMIC FEEDBACK Torvalds, Linus; Keppel, David
PCT/US00/033588	WO	12/7/2000	Interpage prologue to protect virtual address mappings Bedichek,Robert; Keppel, David; Banning, John
PCT/US00/024649	WO	9/6/2000	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
PCT/US03/041489	WO	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
AU2003300016	AU	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
PCT/US05/022585	WO	6/14/2005	System and method for measuring time dependent dielectric breakdown Suzuki, Shingo
PCT/US05/022584	WO	6/14/2005	System and method for measuring negative bias thermal instability Inventorship not available
PCT/US05/006830	WO	3/1/2005	System and method for reducing temperature variation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US05/006813	WO	3/1/2005	System and method for regulating temperature during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US05/006814	WO	3/1/2005	System and method pertaining to burn-in testingSheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US03/041402	WO	12/29/2003	Well regions of semiconductor devices Pelham, Mike; Burr,James B.
AU2003300399	AU	12/29/2003	Well regions of semiconductor devices Pelham, Mike; Burr,James B.
PCT/JP93/000417	WO	3/30/1993	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
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