PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
TRANSMETA LLC	01/28/2009

RECEIVING PARTY DATA

Name:	INTELLECTUAL VENTURE FUNDING LLC
Street Address:	502 E. JOHN STREET
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State/Country:	NEVADA
Postal Code:	89706

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	12649750

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	JONATHAN LEE
SIGNATURE:	/Jonathan Lee/
DATE SIGNED:	02/14/2022

Total Attachments: 51
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Attachment 2, revised

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Transmeta LLC, a Delaware limited liability company with an office at 2460 N. 1st Street, Suite 200, San Jose, CA 95131 (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Intellectual Venture Funding LLC, a Nevada limited liability company, with an address at 502 E. John Street; Carson City, NV 89706 (***"Assignee"***), or its designees, all right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

Patent or Application No.	**Country**	**Filing Date**	**Title of Patent and First Named Inventor**
PCT/US97/014118	WO	8/11/1997	A MEMORY CONTROLLER FOR A MICROPROCESSOR FOR DETECTING A FAILURE OF SPECULATION ON THE PHYSICAL NATURE OF A COMPONENT BEING ADDRESSED KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
EP1002271 (EP97937205.9)	EP	10/29/2008 (8/11/1997)	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature KELLY EDMUND J; CMELIK ROBERT F; WING MALCOLM JOHN
PCT/US98/002673	WO	2/13/1998	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
EP0961972 (EP198905051.3)	EP	9/28/2005 (2/13/1998)	METHOD AND APPARATUS FOR CORRECTING ERRORS IN COMPUTER SYSTEMS KLAIBER ALEX; BEDICHEK ROBERT; KEPPEL DAVID
PCT/US97/016911	WO	9/22/1997	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
EP1008050 (EP97944366.0)	EP	2/28/1997 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
IE1008050 (IE97944366.0)	IE	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
MC1008050 (MC970944366.0)	MC	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
PT1008050 (PT97944366.0)	PT	2/28/2007 (9/22/1997)	Method and apparatus for aliasing memory data in an advanced microprocessor Wing, Malcolm J.; Kelly, Edmund J.
PCT/US97/012058	WO	7/11/1997	Host microprocessor with apparatus for temporarily holding target processor state Kelly, Edmund J.; Wing, Malcolm John
PCT/US97/022768	WO	12/12/1997	A GATED STORE BUFFER FOR AN ADVANCED MICROPROCESSOR WING MALCOLM J; D SOUZA GODFREY P
PCT/US97/011616	WO	6/25/1997	Improved Microprocessor Cmelik, Robert F.; Ditzel, David R.; Kelly, Edmund J.; Hunter, Colin B.; Laird, Douglas A.; Wing, Malcolm John; Zyner, Grzegorz B.
PCT/US97/014117	WO	8/11/1997	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP97939380.8	EP	8/11/1997	Translated memory protection apparatus for an advanced microprocessor Kelly, Edmund J.; Cmelik, Robert F.; Wing, Malcolm J.
07/860,719	US	3/31/1992	Superscalar Risc Instruction Scheduling Sanjiv Garg
PCT/JP93/000375	WO	3/26/1993	Superscalar Risc Instruction Scheduling Sanjiv Garg
08/470,485	US	6/6/1995	Inventorship not available
08/483,893	US	6/7/1995	Inventorship not available
EP0636256 (EP93906834.2)	EP	6/4/1997 (3/26/1993)	Superscalar Risc Instruction Scheduling Sanjiv Garg
JP2000-008147	JP	3/26/1993	Instruction Executing Method Sanjiv Garg
09/906,099	US	7/17/2001	Superscalar RISC instruction schedulingGarg, Sanjiv; Iadonato, Kevin Ray; Nguyen, Le Trong; Wang, Johannes
11/252,820	US	10/19/2005	Superscalar RISC instruction scheduling Inventors: Le Trong Nguyen; Sanjiv Garg; Johannes Wang; Kevin Ray Iadonato
09/329,352	US	6/10/1999	Inventorship not available
PCT/US00/024697	WO	9/6/2000	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
EP1234277 (EP00961695.4)	EP	6/18/2008 (9/6/2000)	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
JP2001-530814	JP	9/6/2000	Programmable event counter system Coon, Brett; Keppel, David; Price, Charles R.
PCT/US00/024651	WO	9/6/2000	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
EP1240582 (EP00960034.7)	EP	10/13/2007 (9/6/2000)	Fine grain translation discrimination Banning, John; Anvin, H. Peter; Gribstad, Benjamin; Keppel, David; Klaiber, Alex; Serris, Paul
PCT/US00/040856	WO	9/6/2000	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
EP1226492 (EP00974084.6)	EP	5/17/2006 (9/6/2000)	Method and apparatus for maintaining context while executing translated instructions Keppel, David; Cmelik,Robert; Bedichek,Robert
10/464,816	US	6/18/2003	Link pipe system for storage and retrieval of sequences of branch addresses Banning, John; Coon, Brett; Hao, Eric

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/464,870	US	6/18/2003	SOFTWARE DIRECT MEMORY ACCESS Patrick Boyle; David Keppel; Alexander C. Klaiber; Edmund Kelly
PCT/US00/040857	WO	9/6/2000	CONTROLLING INSTRUCTION TRANSLATION USING DYNAMIC FEEDBACK Torvalds, Linus; Keppel, David
PCT/US00/033588	WO	12/7/2000	Interpage prologue to protect virtual address mappings Bedichek,Robert; Keppel, David; Banning, John
PCT/US00/024649	WO	9/6/2000	Method of changing modes of code generation Torvalds, Linus; Anvin, H. Peter
PCT/US03/041489	WO	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
AU2003300016	AU	12/29/2003	Adaptive power control Burr, James B.; Read, Andrew; Stewart, Tom
PCT/US05/022585	WO	6/14/2005	System and method for measuring time dependent dielectric breakdown Suzuki, Shingo
PCT/US05/022584	WO	6/14/2005	System and method for measuring negative bias thermal instability Inventorship not available
PCT/US05/006830	WO	3/1/2005	System and method for reducing temperature variation during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US05/006813	WO	3/1/2005	System and method for regulating temperature during burn-in Sheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US05/006814	WO	3/1/2005	System and method pertaining to burn-in testingSheng, Eric Chen-Li; Hoffman, David H.; Niven, John Laurence
PCT/US03/041402	WO	12/29/2003	Well regions of semiconductor devices Pelham, Mike; Burr,James B.
AU2003300399	AU	12/29/2003	Well regions of semiconductor devices Pelham, Mike; Burr,James B.
PCT/JP93/000417	WO	3/30/1993	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
EP0636257 (EP93906870.6)	EP	11/8/2000 (3/30/1993)	CISC to RISC instruction translation alignment and decoding Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
EP1028370 (EP00108579.4)	EP	9/15/2004 (3/30/1993)	System and method for translating a stream of non-native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
JP2000-007261	JP	1/1/2000	Processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP2000-007262	JP	1/1/2000	Conversion sytem for instruction stream Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
09/852,295	US	5/10/2001	System and method for translating non-native instructions to native instructions for processing on a host processor Coon, Brett; Miyayama, Yoshiyuki; Nguyen, Le Trong; Wang, Johannes
PCT/US00/024650	WO	9/6/2000	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
AT963330/2000	AT	9/6/2000	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
EP1230594 (EP00963330.6)	EP	6/14/2006 (9/6/2000)	A method for translating instructions in a speculative microprocessor Torvalds, Linus; Bedichek,Robert; Johnson, Stephen
PCT/US00/016209	WO	6/12/2000	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
JP2001-504103	JP	6/12/2000	Method and apparatus for enhancing scheduling in an advanced microprocessor Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
KR10-2005-7023578	KR	12/8/2005	Method of scheduling and executing instructions Rozas, Guillermo J.; D'Souza, Godfrey P.; Price, Charles R.; Serris, Paul S.
PCT/US01/001684	WO	1/16/2001	Adaptive power control Halepete, Sameer; Anvin, H. Peter; Chen, Zongjian; D'Souza, Godfrey P.; Fleischmann, Marc; Klayman, Keith; Lawrence, Thomas; Read, Andrew
10/824,702	US	4/14/2004	System for on-chip temperature measurement in integrated circuits Schnaitter, William N.
PCT/US05/020188	WO	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES AND RESET CAPABILITY Masleid, Robert Paul; Dholabhai, Vatsal
EP05759508.4	EP	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES AND RESET CAPABILITY MASLEID, Robert, Paul; DHOLABHAI, Vatsal
PCT/US05/020189	WO	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODESMASLEID, Robert, Paul;DHOLABHAI, Vatsal;STOIBER, Steven, Thomas;SINGH, Gurmeet
EP05760480.3	EP	6/8/2005	REPEATER CIRCUIT WITH HIGH PERFORMANCE AND NORMAL REPEATER MODES MASLEID, Robert, Paul; DHOLABHAI, Vatsal; STOIBER, Steven, Thomas; SINGH, Gurmeet
PCT/US05/020347	WO	6/8/2005	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS MASLEID, Robert Paul; KOWALCZYK, Andre

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP05756631.7	EP	6/8/2005	CIRCUITS AND METHODS FOR DETECTING AND ASSISTING WIRE TRANSITIONS MASLEID, Robert Paul; KOWALCZYK, Andre
PCT/US05/020348	WO	6/8/2005	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Masleid, Robert Paul; Dholabhai, Vatsal; Klingner, Christian
EP05757712.4	EP	6/8/2005	REPEATER CIRCUIT HAVING DIFFERENT OPERATING AND RESET VOLTAGE RANGES, AND METHODS THEREOF Masleid Robert Paul; Dholabhai Vatsal; Klingner Christian
60/486,629	US	7/10/2003	System and method for identifying page table entries with a physical address within a specified range Rozas, Guillermo; Klaiber, Alexander; Anvin, H. Peter; Dunn, David
PCT/US03/041490	WO	12/29/2003	MICROPROCESSOR AND MICROPROCESSOR OPERATION READ, Andrew, J.; WING, Malcolm;
EP03800281.2	EP	12/29/2003	MICROPROCESSOR AND MICROPROCESSOR OPERATION READ, Andrew, J.; WING, Malcolm
10/951,835	US	9/27/2004	adaptive power control based on pre package characterization of integrated circuits Andrew Read; Malcolm Wing
PCT/US06/026404	WO	7/5/2006	ELASTIC PIPELINE LATCH MASLEID, Robert Paul;
EP06786530.3	EP	7/5/2006	ELASTIC PIPELINE LATCH MASLEID, Robert Paul;
PCT/US01/050801	WO	10/18/2001	METHOD AND APPARATUS FOR REDUCING STATIC POWER LOSS Read, Andrew; Halepete, Sameer; Klayman, Keith
EP99102406.8	EP	7/8/1992	Process and method for utilizing register file resources Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
PCT/US92/005720	WO	7/8/1992	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
EP0547216 (EP92915765.9)	EP	9/29/1999 (7/8/1992)	RISC microprocessor architecture implementing multiple typed register sets Garg, Sanjiv; Lentz, Derek J.; Nguyen, Le T.; Chen, Sho L.
09/840,026	US	4/24/2001	RISC microprocessor architecture implementing multiple register sets Derek J. Lentz; Le Trong Nguyen; Sanjiv Garg; Sho Long Chen
PCT/US03/041491	WO	12/29/2003	Circuit ManagementDitzel, David R.; Burr,James B.
PCT/US06/038168	WO	9/28/2006	Securing scan test architecture Morgan, Andrew; Dunn, David

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
60/488,222	US	7/16/2003	SYSTEM AND METHOD OF INSTRUCTION MODIFICATION John Banning; Eric Hao
10/956,219	US	9/30/2004	Systems and methods for control of integrated circuits comprising body biasing systems Kleanthes G Koniaris, Stephen Lee and Mark Hennecke
PCT/US07/007930	WO	3/30/2007	Memory circuit Robert P Masleid
PCT/US07/007929	WO	3/30/2007	A multi-portioned instruction memory John P. Banning; Guillermo J. Rozas
12/002,581	US		Inventorship not available
PCT/US03/041403	WO	12/29/2003	Manufacture and operation of integrated circuit Tom Stewart
PCT/US05/041185	WO	11/7/2005	Systems and methods for voltage distribution via epitaxial layers Robert P. Masleid
PCT/US05/041541	WO	11/7/2005	Systems and methods for voltage distribution via multiple epitaxial layers Robert Paul Masleid
PCT/US06/004094	WO	2/3/2006	System and method for providing a secure boot architecture Andrew Morgan; Christian Ludloff; Guillermo Rozas
PCT/US06/004095	WO	2/3/2006	Method and system for validating a computer system Guillermo J. Rozas
PCT/US06/011661	WO	3/29/2006	A system and method for elastic signal pipelining Guillermo J. Rozas; Robert P. Masleid
PCT/US06/025214	WO	6/27/2006	A dynamic circuit latch Robert Paul Masleid; Jose Sousa; Venkata Kottapalli
PCT/US06/025215	WO	6/27/2006	Storage element circuit James B. Burr; Robert P. Masleid; Kleanthes G. Koniaris
PCT/US06/025739	WO	6/29/2006	Clock signal distribution system and method Scott Pitkethly

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this 28th day of January, 2009.

ASSIGNOR:

Transmeta LLC

BY: NOVAFORA, INC.
ITS: SOLE MEMBER

By: Jodi Pittman
Name: Jodi Pittman
Title: CFO