PATENT ASSIGNMENT COVER SHEET

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
XILINX GMBH	03/27/2019

RECEIVING PARTY DATA

Name:	XILINX, INC.
Street Address:	2100 LOGIC DRIVE
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95124

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17826068

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email:	jschon@pattersonsheridan.com, psdocketing@pattersonsheridan.com
Correspondent Name:	XILINX, INC.
Address Line 1:	2100 LOGIC DRIVE
Address Line 4:	SAN JOSE, CALIFORNIA 95124

ATTORNEY DOCKET NUMBER:	X-5429 US
NAME OF SUBMITTER:	KEITH TABOADA
SIGNATURE:	/Keith Taboada/
DATE SIGNED:	06/07/2022

Total Attachments: 3
source=X-5429 US Xilinx GmbH to Xilinx Inc Assignment- signed#page1.tif
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PATENT ASSIGNMENT

This Patent Assignment (the "Assignment") is made from **Xilinx GmbH**, a company organized and existing under the laws of Germany, whose principal place of business is Willy-Brandt-Allee 4, Munich 81829, Germany, (the "Assignor") to **Xilinx, Inc.**, a Delaware corporation, whose principal place of business is 2100 Logic Drive, San Jose, CA 95124 (the "Assignee").

Assignor desires to assign to Assignee and its successors all of Assignor's right, title and interest in and to the patents and any and all corresponding patent applications, divisional applications, continuing applications, provisionals, reissues, reexams, and extensions thereof related thereto or based thereon, any and all patents issuing thereon, and any and all foreign patents and patent applications corresponding thereto or relying thereon (including corresponding PCT applications and any patents resulting therefrom) for its filing or convention date (the "Patents") set forth in **Schedule A** which is attached hereto, together with the goodwill of the business pertaining thereto.

In consideration for good and valuable consideration, receipt and sufficiency of which is hereby acknowledged, Assignor does hereby assign, transfer, grant, sell and otherwise convey to Assignee and its successors all of Assignor's rights, title and interest in and to the Invention, including all common law rights therein, applications to register therefor, together with the good will of the business symbolized by the Patents and all claims for damages by reason of past infringements of the Patents with the right to sue for and collect the same for its own use and benefit, and for the use and on behalf of its successors, assigns and other legal representatives. Assignor authorizes the Director of Patents and Trademarks of the United States of America, and the empowered officials of all other governments to issue or transfer all said patents and patent applications to Assignee, as assignee thereof, or otherwise as Assignee may direct.

Dated: _27/3/19_

Assignor: Xilinx GmbH

By: _____

Name: Kevin Cooney

Title: CIO, Senior V.P. / Managing Director EMEA

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.
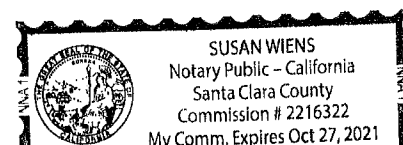

State of California)
County of Santa Clara)

On **March 27, 2019** _____, *before me, Susan Wiens, Notary Public, personally appeared Kevin Cooney, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.*

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Susan Wiens
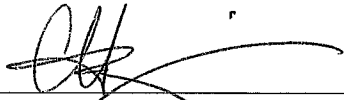*Signature of Notary Public*

**PATENT
REEL: 060117 FRAME: 0349**

Dated: *March 27, 2019*

Assignee: Xilinx, Inc.

By: _____

Name: Catia Hagopian
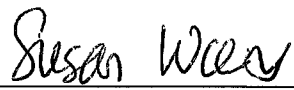
Title: Senior Vice President and General Counsel

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.
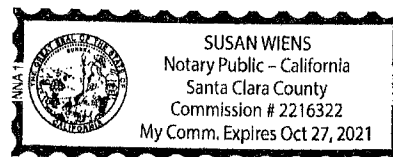

State of   California   )
County of Santa Clara   )

On March 27, 2019   , before me, Susan Wiens, Notary Public, personally appeared Catia Hagopian, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Susan Wien
Signature of Notary Public

SCHEDULE A

Attorney Docket No.	Country	Application Number	Filing Date	Title
X-5425	US	15/944,295	03-Apr-2018	Device with Data Processing Engine Array that Enables Partial Reconfiguration
X-5426	US	15/944,303	03-Apr-2018	Stall Logic for a Data Processing Engine in an Integrated Circuit
X-5427	US	15/944,602	03-Apr-2018	Event-Based Debug, Trace, and Profile in Device with Sata Processing Engine Array
X-5428	US	15/944,307	03-Apr-2018	Device with Data Processing Engine Array
X-5429	US	15/944,179	03-Apr-2018	Communicating Between Data Processing Engines Using Shared Memory
X-5430	US	15/944,160	03-Apr-2018	Data Processing Engine Arrangement in a Device
X-5431	US	15/944,393	03-Apr-2018	Data Selection Network For A Data Processing Engine In An Integrated Circuit
X-5432	US	15/944,578	03-Apr-2018	Cascade Streaming Between Data Processing Engines in an Array
X-5433	US	15/944,408	03-Apr-2018	Data Processing Engine Tile Architecture For An Integrated Circuit
X-5434	US	15/944,315	03-Apr-2018	Core for a Data Processing Engine in an Integrated Circuit
X-5437	US	15/944,464	03-Apr-2018	Streaming Interconnect Architecture for Data Processing Engine Array
X-5438	US	15/944,490	03-Apr-2018	Dual Mode Interconnect
X-5439	US	15/944,617	03-Apr-2018	System-on-Chip Interface Architecture