PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7571701

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
PERASO INC. F/K/A MOSYS, INC.	10/03/2022

RECEIVING PARTY DATA

Name:	INGALLS & SNYDER LLC
Street Address:	1325 AVENUE OF THE AMERICAS
Internal Address:	18TH FLOOR
City:	NEW YORK
State/Country:	NEW YORK
Postal Code:	10019

PROPERTY NUMBERS Total: 82

Property Type	Number
Patent Number:	5790138
Patent Number:	5923593
Patent Number:	5999474
Patent Number:	6075740
Patent Number:	6075720
Patent Number:	6256248
Patent Number:	6415353
Patent Number:	6457108
Patent Number:	6496437
Patent Number:	6573548
Patent Number:	6584036
Patent Number:	6642098
Patent Number:	6732229
Patent Number:	6784048
Patent Number:	6826069
Patent Number:	6841821
Patent Number:	7051264
Patent Number:	7167410
Patent Number:	7352307

Property Type	Number
Patent Number:	7382658
Patent Number:	7447104
Patent Number:	7477546
Patent Number:	7499307
Patent Number:	7533222
Patent Number:	7599396
Patent Number:	7728747
Patent Number:	7791975
Patent Number:	7894270
Patent Number:	7919367
Patent Number:	7929359
Patent Number:	8044724
Patent Number:	8135037
Patent Number:	8139399
Patent Number:	8161355
Patent Number:	8171234
Patent Number:	8217814
Patent Number:	8238169
Patent Number:	8266471
Patent Number:	8269538
Patent Number:	8274326
Patent Number:	8361863
Patent Number:	8368217
Patent Number:	8370725
Patent Number:	8436660
Patent Number:	8446755
Patent Number:	8451675
Patent Number:	8460995
Patent Number:	8473695
Patent Number:	8526265
Patent Number:	8527676
Patent Number:	8539196
Patent Number:	8547774
Patent Number:	8587046
Patent Number:	8635417
Patent Number:	8681574
Patent Number:	8704570
Patent Number:	8832336

Property Type	Number
Patent Number:	8836381
Patent Number:	8890332
Patent Number:	8901747
Patent Number:	8954803
Patent Number:	8988956
Patent Number:	9030894
Patent Number:	9037928
Patent Number:	9054578
Patent Number:	9118611
Patent Number:	9148154
Application Number:	12697141
Application Number:	13728910
Application Number:	13841025
Application Number:	13838971
Application Number:	13911999
Application Number:	13912191
Application Number:	13912033
Application Number:	13911218
Application Number:	14031031
Application Number:	14231730
Application Number:	14320632
Application Number:	14564618
Application Number:	14839576
Application Number:	14872002
Application Number:	14872137

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 9175467711
Email: nzn@msk.com
Correspondent Name: NICHOLAS NIETO
Address Line 1: 437 MADISON AVE
Address Line 2: 25TH FLOOR
Address Line 4: NEW YORK, NEW YORK 10022

NAME OF SUBMITTER:	NICHOLAS NIETO
SIGNATURE:	/NICHOLAS NIETO/
DATE SIGNED:	10/03/2022

Total Attachments: 9
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RELEASE OF PATENT SECURITY INTEREST

This RELEASE OF PA TENT SECURITY INTEREST (this "**Release**") is made and effective as of October 3, 2022, and granted by Ingalls & Snyder LLC, a New York limited liability company (the "**Purchaser's Agent**"), in its capacity as agent for the purchasers under the Purchase Agreement referred to below (the "**Secured Parties**"), in favor of MoSys, Inc., a Delaware corporation (now known as Peraso Inc., the "**Grantor**").

WHEREAS, pursuant to that certain Senior Secured Convertible Note Purchase Agreement (the "**Purchase Agreement**"), among the Grantor, the Purchaser's Agent and the purchasers party thereto, the Grantor executed and delivered to the Purchaser's Agent that certain Intellectual Property Security Agreement, dated as of the date of the Purchase Agreement (the "**IP Security Agreement**"), between the Grantor and the Purchaser's Agent;

WHEREAS, pursuant to the IP Security Agreement, the Grantor pledged and granted to the Purchaser's Agent for the ratable benefit of the Secured Parties a security interest in and to all of the right, title and interest of such Grantor in, to and under the Patent Collateral (as defined below);

WHEREAS, the IP Security Agreement was recorded with the United States Patent and Trademark Office at Reel 038081, Frame 0262 on March 14, 2016; and

WHEREAS, the Grantor has requested that the Purchaser's Agent enter into this Release in order to effectuate, evidence and record the release and reassignment to the Grantor of any and all right, title and interest the Purchaser's Agent and the Secured Parties may have in the Patent Collateral pursuant to the IP Security Agreement.

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Purchaser's Agent hereby states as follows:

1. Release of Security Interest. The Purchaser's Agent, on behalf of itself and the Secured Parties, their successors, legal representatives and assigns, hereby terminates, releases and discharges any and all security interests that it has pursuant to the IP Security Agreement in any and all right, title and interest of the Grantor, and reassigns to the Grantor any and all right, title and interest that it may have, in, to and under the following (collectively, the "**Patent Collateral**"):

(a) any and all patents, patent applications and other patent rights and any other governmental authority-issued indicia of invention ownership, including the patents and patent applications listed in Schedule 1 hereto, and all reissues, divisions, continuations, continuations-in-part, renewals, extensions and reexaminations thereof and amendments thereto;

(b) all rights of any kind whatsoever of such Grantor accruing under any of the foregoing provided by applicable law of any jurisdiction, by international treaties and conventions and otherwise throughout the world;

(c) any and all royalties, fees, income, payments and other proceeds now or hereafter due or payable with respect to any and all of the foregoing; and

(d) any and all claims and causes of action, with respect to any of the foregoing, whether occurring before, on or after the date hereof, including all rights to and claims for damages, restitution and injunctive and other legal and equitable relief for past, present and future infringement, dilution, misappropriation, violation, misuse, breach or default, with the right but no obligation to sue for such legal and equitable relief and to collect, or otherwise recover, any such damages.

2. Further Assurances. The Purchaser's Agent agrees to take all further actions, and provide to the Grantor and its successors, assigns and legal representatives all such cooperation and assistance, including, without limitation, the execution and delivery of any and all further documents or other instruments, as the Grantor and its successors, assigns and legal representatives may reasonably request in order to confirm, effectuate or record this Release.

3. Governing Law. This Release and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Release and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of New York, without giving effect to any choice or conflict of law provision or rule (whether of the State of New York or any other jurisdiction).

[SIGNATURE PAGE FOLLOWS]

IN WITNESS WHEREOF, the Purchaser's Agent has caused this Release to be duly executed and delivered by its officer thereunto duly authorized as of the date first above written.

THE PURCHASER'S AGENT:

INGALLS & SNYDER LLC

By: _____
Name: Thomas O. Boucher Jr.
Title: Manager

Acknowledged By:

THE GRANTOR:

PERASO INC. (f/k/a MoSys, Inc.)

By: James Sullivan
James Sullivan (Sep 27, 2022 07:04 PDT)
Name: James Sullivan
Title: CFO

[Signature Page to Release of Patent Security Interest]

SCHEDULE 1

PATENTS AND PATENT APPLICATIONS

DOCKET NUMBER	TITLE	ISSUE DATE	SERIAL NUMBER	PATENT NUMBER
MP-1016	Method and structure for improving display data bandwidth in a unified memory architecture system	1998-08-04	08587379	5790138
MP-1021	Multi-port DRAM cell and memory system using same	1999-07-13	08767707	5923593
MP-1024	Method and Apparatus for Complete Hiding of the Refresh of a Semiconductor Memory	1999-12-07	09165228	5999474
MP-1030	Method .. for Increasing The Time Available for Refresh For 1-T SRAM Compatible Devices	2000-06-13	09181840	6075740
MP-1029	Memory cell for DRAM embedded in logic	2000-06-13	09134488	6076720
MP-1039	Method and apparatus for increasing the time available for internal refresh for 1-T SRAM compatible devices	2001-07-03	09590943	6256248
MP-1048	Read/Write Buffers for Complete Hiding of the Refresh of a Semiconductor Memory and Method of Operating Same	2002-07-02	09405607	6415353
MP-1052	Method of operating a system-on-a-chip including entering a standby state in a non-volatile memory while operating the system-on-a-chip from a volatile memory	2002-09-24	09415032	6457108
MP-1055 US	Method and Apparatus for Forcing Idle Cycles to Enable Refresh Operations in a Semiconductor Memory	2002-12-17	09795750	6496437
MP-1060 US	DRAM Cell Having A Capacitor Structure Fabricated Partially in a Cavity and Method for Operating the Same	2003-06-03	10033690	6573548

DOCKET NUMBER	TITLE	ISSUE DATE	SERIAL NUMBER	PATENT NUMBER
MP-1061 (ATMOS)	SRAM Emulator	2003-06-24	10096945	6584036
MP-1063	DRAM cell having a capacitor structure fabricated partially in a cavity and method for operating same	2003-11-04	10374917	6642098
MP-1072	Method and apparatus for memory redundancy with no critical delay-path	2004-05-04	09503751	6732229
MP-1076	Method of Fabricating A DRAM Cell having a Thin Dielectric Access Transistor and a Thick Dielectric Storage	2004-08-31	10231800	6784048
MP-1079 (ATMOS)	Interleaved wordline architecture	2004-11-30	10737825	6826069
MP-1080	Non-volatile memory cell fabricated with slight modification to a conventional logic process and methods of operating same	2005-01-11	10355477	6841821
MP-1085	Error correcting memory and method of operating same	2006-05-23	10003602	7051264
MP-1187	Memory System and Memory Device Having a Serial Interface	2007-01-23	11114807	7167410
MP-1091	Comparator chain offset reduction	2008-04-01	11351877	7352307
MP-1093	NVM Embedded in a Conventional Logic Process & Methods for Operating Same	2008-06-03	11421986	7382658
MP-1102	Word Line Driver for DRAM Embedded in a Logic Process	2008-11-04	11559870	7447104
MP-1109	NVM Embedded in a Conventional Logic Process & Methods for Operating Same	2009-01-13	12021255	7477546
MP-1101	Scalable Embedded DRAM Array	2009-03-03	11534506	7499307
MP-1100	Dual-port SRAM memory using single-port memory cell	2009-05-12	11427785	7533222

DOCKET NUMBER	TITLE	ISSUE DATE	SERIAL NUMBER	PATENT NUMBER
MP-1188	Method of encoding and synchronizing a serial interface	2009-10-06	11178958	7599396
MP-1091 CON	Comparator Chain Offset Reduction	2010-06-01	12041578	7728747
MP-1116	Scalable Embedded DRAM Array	2010-09-07	12048170	7791975
MP-1136	Data Restoration Method for a Non-volatile Memory	2011-02-22	12378248	7894270
MP-1108	Method to Increase Charge Retention of Nonvolatile Memory Manufactured in a Single-Gate Logic Process	2011-04-05	12021229	7919367
MP-1138	Embedded DRAM with Bias-independent Capacitance	2011-04-19	12291762	7929359
MP-1149	Low Jitter Large Frequency Tuning LC PLL for Multi-Speed Clocking Applications	2011-10-25	12430430	8044724
MP-1188-01	Method and Apparatus to Encode and Synchronize a Serial Interface	2012-03-13	12548135	8135037
MP-1148	Multiple Cycle Memory Write Completion	2012-03-20	12577994	8139389
MP-1126	Automatic Refresh For Improving Data Retention And Endurance Characteristics Of An Embedded Non-Volatile Memory In A Standard Cmos Logic Process	2012-04-17	12378249	8161355
MP-1128	Multi-bank Multi-port Architecture	2012-05-01	12404955	8171234
MP-1206	Low Power Serial-to-Parallel Converter	2012-07-10	12971847	8217814
MP-1136-1D	Method and Apparatus for Restoring Data in a Non-Volatile Memory	2012-08-07	13027621	8238169
MP-1161	Memory Device including a Memory Block Having a Fixed Latency Data Output	2012-09-11	12702767	8266471

DOCKET NUMBER	TITLE	ISSUE DATE	SERIAL NUMBER	PATENT NUMBER
MP-1151	Signal Alignment System	2012-09-18	12768513	8269538
MP-1193	Equalization Circuit	2012-09-25	12872852	8274326
MP-1118	Embedded DRAM with Multiple Gate Oxide Thicknesses	2013-01-29	12291765	8361863
MP-1205-C2-PE	Integrated Circuit Package With Segregated Tx And Rx Data Channels	2013-02-05	13541658	8368217
MP-1160 a US	Communication Interface and Protocol (GCI; GigaChip Interface Protocol)	2013-02-05	12697763	8370725
MP-1191	Voltage-Mode Driver with Equalization	2013-05-07	12870549	8436660
MP-1148-1D	Multiple Cycle Memory Write Completion	2013-05-21	13369253	8446755
MP-1166-2	Methods For Accessing DRAM Cells Using Separate Bit Line Control	2013-05-28	13077811	8451675
MP-1190	Method of Forming a MIM Capacitor	2013-06-11	12804855	8460995
MP-1210 US	Memory System Including Variable Write Command Scheduling	2013-06-25	13077261	8473695
MP-1154	Three State Word Line Driver For A DRAM Memory Device	2013-09-03	12645321	8526265
MP-1159-C1-PE	Reducing latency in Serializer-Deserializer Links	2013-09-03	13467955	8527670
MP-1157	Hierarchical Organization of Large Memory Blocks	2013-09-17	12697132	8539196
MP-1164	Hierarchical Multi-Bank Multi-Port Memory Organization	2013-10-01	12697150	8547774
MP-1190-CIP1	SYSTEM WITH LOGIC AND EMBEDDED MIM CAPACITOR	2013-11-19	13191423	8587046
MP-1210-C1-PE	Memory System Including Variable Write Command Scheduling	2014-01-21	13468850	8635417

DOCKET NUMBER	TITLE	ISSUE DATE	SERIAL NUMBER	PATENT NUMBER
MP-1168-1	Separate Pass Gate Controlled Sense Amplifier	2014-03-25	13077798	8681574
MP-1221 US1	Dual Loop DLL	2014-0422	13720981	8704570
MP-1159 US	Reducing latency in Serializer-Deserializer Links	2014-09-09	12697223	8832336
MP-1192 US	Output Buffer, Voltage Mode Driver w/Equalization	2014-09-16	13787692	8836381
MP-1205-cip1	Integrated Circuit Package With Segregated Tx And Rx Data Channels	2014-11-18	13843427	8890332
MP-1205	Semiconductor Chip Layout	2014-12-02	12846763	8901747
MP-1147	Programmable Test Engine (PCOTE) for Emerging Memory Technologies	2015-02-10	13030358	8954803
MP-1240	Programmable Memory Built in Self Repair Circuit	2015-03-24	13834856	8988956
MP-1164-C1	Hierarchical Multi-Bank Multi-Port Memory Organization	2015-05-12	13972798	9030894
MP-1213	Memory Device With Background Built-In Self-Testing And Background Built-In Self-Repair	2015-05-19	13732783	9037928
MP-1219	Hybrid driver including a turbo mode	2015-06-09	13923160	9054678
MP-1185	Data Synchronization For Circuit Resources Without Using A Resource Buffer	2015-08-25	13215205	9118611
MP-1221-C2	Delay-Locked Loop With Independent Phase Adjustment Of Delayed Clock Output Pairs	2015-09-29	14231739	9148154

DOCKET NUMBER	TITLE	FILING DATE	SERIAL NUMBER	PUBLICATION NUMBER
MP-1162 a US	High Utilization Multi-Partitioned Serial Memory	2010-01-29	12697141	2011-0191548
MP-1212 (US)	METHODS AND CIRCUITS FOR ADJUSTING PARAMETERS OF A TRANSCEIVER	2012-12-28	13728910	2013-0169314
MP-1233 US	Memory with Bank-Conflict-Resolution (BCR) Module including Cache	2013-03-15	13841025	2013-0332665
MP-1235 US	Traffic Metering and Shaping for Network Packets	2013-03-15	13838971	2013-0329553
MP-1234 US	Memory Device With An Embedded Logic Unit	2013-06-06	13911999	2013-0329555
MP-1237-US	High Utilization Multi-Partitioned Memory With Write Cache, BIST, and Statistics Functions	2013-06-08	13912191	
MP-1236 US	Programmable Width Counter Boundary	2013-06-06	13912033	2013-0332708
MP-1210-CIP1	Memory System including Variable Write Burst and Broadcast Command Scheduling	2013-06-06	13911218	2013-0332681
MP-1214	Substitute Redundant Memory	2013-09-18	14031031	2014-0082453
MP-1221-C1	Delay-Locked Loop With Dual Loop Filters For Fast Response And Wide Frequency And Delay Range	2014-03-31	14231730	2014-0218083
MP-1213-C1	Memory Device With Background Built-in Self- Repair (BBISR) Using Background Built-in Self- Testing (BBIST)	2014-06-30	14320632	2014-0317460
MP-1246	Hybrid Driver Circuit	2014-12-09	14564618	
MP-1248	Hashing Circuit	2015-08-28	14839576	2018-0019029
MP-1247	Integrated Main Memory And Coprocessor With Low Latency	2015-09-30	14872002	
MP-1247-c1	Integrated Main Memory And Coprocessor With Low Latency	2015-09-30	14872137	