

## PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT7627069

<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	ASSIGNMENT

**CONVEYING PARTY DATA**

Name	Execution Date
DELTA ELECTRONICS, INC.	10/19/2022

**RECEIVING PARTY DATA**

<b>Name:</b>	ANCORA SEMICONDUCTORS INC.
<b>Street Address:</b>	6F., NO. 252, SHANYING RD., GUISHAN DIST.
<b>City:</b>	TAOYUAN CITY
<b>State/Country:</b>	TAIWAN
<b>Postal Code:</b>	333425

**PROPERTY NUMBERS Total: 22**

Property Type	Number
Patent Number:	9484418
Patent Number:	9385070
Patent Number:	8912663
Patent Number:	8957493
Patent Number:	9190393
Patent Number:	9508843
Patent Number:	9793370
Patent Number:	9755044
Patent Number:	9325308
Patent Number:	10229978
Patent Number:	10854720
Patent Number:	11296195
Patent Number:	9431327
Patent Number:	9324819
Patent Number:	11049796
Patent Number:	10685904
Patent Number:	9754932
Patent Number:	9502548
Patent Number:	9793390
Patent Number:	9893015

PATENT

Property Type	Number
Patent Number:	9847312
Patent Number:	10978403

**CORRESPONDENCE DATA**

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<b>NAME OF SUBMITTER:</b>	RANDY A. NORANBROCK
<b>SIGNATURE:</b>	/Randy A. Noranbrock/
<b>DATE SIGNED:</b>	11/03/2022

**Total Attachments: 3**

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## TRANSFER OF ASSIGNMENT RIGHTS

In re Application of : see attachment, Exhibit A

Serial No.: see attachment, Exhibit A

Filed: see attachment, Exhibit A

The PATENT RIGHTS referred to in this agreement include all divisions, reissues, continuations and extensions of the patents and patent applications identified above.

The PATENT RIGHTS assigned under this agreement are:

- U.S. patent rights only
- Worldwide patent rights. In this case, the assignee shall have the right to claim the Benefit of the filing date of any U.S. or foreign patent application for this invention.

The ASSIGNEE referred to in this agreement is:

*(Name of Assignee)* Ancora Semiconductors Inc.

*(Address)* 6F., No. 252, Shanying Rd., Guishan Dist., Taoyuan City 333425, Taiwan, R.O.C.

The ASSIGNEE is:

- An individual
- A Partnership
- A Corporation of Taiwan, R.O.C. *(specify state or country)*

Whereas, ASSIGNEE is desirous of acquiring less than the entire right, title and interest in the same;

The extent (by percentage) of ownership interest is 100 %

Now, therefore, in consideration of the sum of One dollars (\$ 1.00), the receipt whereof is acknowledged, and other good and valuable consideration, the assignor by these presents do sell, assign and transfer unto said assignee the entire right to the said invention in the United States and the rights, title and interest in and to any and all Patents which may be granted therefore in the United States consistent with ownership interest.

In re Application of: see attachment, Exhibit A  
Serial No.: see attachment, Exhibit A

Page 2

The undersigned do hereby declare that all statements made herein are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DELTA ELECTRONICS, INC.

Assignor

Kuo Liang Yeh 10/19/2002

Signature

Name: Kuoliang YEH

Title: General Counsel

No. 252, Shanying Rd., Guishan Dist., Taoyuan City 333, Taiwan, R.O.C.

Address

.....  
Date

**Exhibit A**  
**Patents and Patent Applications Assigned to Ancora Semiconductors Inc.**

No.	Title	Filing Date	Serial No.	Date of Patent	Patent No.
1	Semiconductor Device	2013/11/19	14/083,777	2016/11/01	9,484,418
2	SEMICONDUCTOR COMPONENT HAVING A LATERAL SEMICONDUCTOR DEVICE AND A VERTICAL SEMICONDUCTOR DEVICE	2013/06/28	13/930,817	2016/07/05	9,385,070
3	EMBEDDED PACKAGE STRUCTURE AND METHOD FOR MANUFACTURING THEREOF	2013/06/28	13/930,949	2014/12/16	8,912,663
4	SEMICONDUCTOR DEVICE	2014/02/20	14/185,322	2015/02/17	8,957,493
5	LOW PARASITIC CAPACITANCE SEMICONDUCTOR DEVICE PACKAGE	2014/07/17	14/333,795	2015/11/17	9,190,393
6	Heterojunction Semiconductor Device for Reducing Parasitic Capacitance	2014/09/25	14/496,471	2016/11/29	9,508,843
7	TRANSISTOR WITH OXIDIZED CAP LAYER	2015/05/26	14/721,796	2017/10/17	9,793,370
8	METHOD OF MANUFACTURING A TRANSISTOR WITH OXIDIZED CAP LAYER	2016/06/08	15/176,446	2017/09/05	9,755,044
9	SEMICONDUCTOR DEVICE AND CASCODE CIRCUIT	2014/05/30	14/291,654	2016/04/26	9,325,308
10	Semiconductor Device and Manufacturing Method Thereof	2015/05/29	14/724,963	2019/03/12	10,229,978
11	SEMICONDUCTOR DEVICE MANUFACTURING METHOD	2019/01/30	16/262,352	2020/12/01	10,854,720
12	SEMICONDUCTOR DEVICE MANUFACTURING METHOD	2020/09/30	17/038,693	2022/04/05	11,296,195
13	SEMICONDUCTOR DEVICE	2014/05/30	14/291,563	2016/08/30	9,431,327
14	SEMICONDUCTOR DEVICE	2014/11/26	14/555,056	2016/04/26	9,324,819
15	MANUFACTURING METHOD OF PACKAGING DEVICE	2020/04/23	16/856,797	2021/06/29	11,049,796
16	PACKAGING DEVICE AND MANUFACTURING METHOD THEREOF	2014/11/21	14/549,996	2020/06/16	10,685,904
17	SEMICONDUCTOR DEVICE	2015/11/05	14/933,059	2017/09/05	9,754,932
18	SEMICONDUCTOR DEVICE	2015/09/11	14/851,218	2016/11/22	9,502,548
19	LOW MILLER FACTOR SEMICONDUCTOR DEVICE	2015/12/01	14/955,481	2017/10/17	9,793,390
20	SEMICONDUCTOR DEVICE	2016/03/31	15/086,556	2018/02/13	9,893,015
21	PACKAGE STRUCTURE	2016/05/18	15/157,896	2017/12/19	9,847,312
22	PACKAGE STRUCTURE AND METHOD FOR FABRICATING THE SAME	2019/01/30	16/262,421	2021/04/13	10,978,403

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