

PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT7627886

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	DELTA ELECTRONICS, INC.	10/19/2022
RECEIVING PARTY DATA		
Name:	ANCORA SEMICONDUCTORS INC.	
Street Address:	6F., NO. 252, SHANYING RD.	
Internal Address:	GUISHAN DIST.	
City:	TAOYUAN CITY	
State/Country:	TAIWAN	
Postal Code:	333425	
PROPERTY NUMBERS Total: 1		
	Property Type	Number
	Patent Number:	9660637
CORRESPONDENCE DATA		
Fax Number:	(888)388-6582	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
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ATTORNEY DOCKET NUMBER:	TWT04247/US	
NAME OF SUBMITTER:	JAMES LYNN O'SULLIVAN	
SIGNATURE:	/James Lynn O'Sullivan/	
DATE SIGNED:	11/04/2022	
Total Attachments: 3		
source=TWT04247US-Ownership Transfer from DELTA to ANCORA#page1.tif		
source=TWT04247US-Ownership Transfer from DELTA to ANCORA#page2.tif		
source=TWT04247US-Ownership Transfer from DELTA to ANCORA#page3.tif		

TRANSFER OF ASSIGNMENT RIGHTS

In re Application of : see attachment, Exhibit A

Serial No.: see attachment, Exhibit A

Filed: see attachment, Exhibit A

The PATENT RIGHTS referred to in this agreement include all divisions, reissues, continuations and extensions of the patents and patent applications identified above.

The PATENT RIGHTS assigned under this agreement are:

- ☒ U.S. patent rights only
- ☐ Worldwide patent rights. In this case, the assignee shall have the right to claim the Benefit of the filing date of any U.S. or foreign patent application for this invention.

The ASSIGNEE referred to in this agreement is:

(Name of Assignee) Ancora Semiconductors Inc.

(Address) 6F., No. 252, Shanying Rd., Guishan Dist., Taoyuan City 333425, Taiwan, R.O.C.

The ASSIGNEE is:

- ☐ An individual
- ☐ A Partnership
- ☒ A Corporation of Taiwan, R.O.C. (specify state or country)

Whereas, ASSIGNEE is desirous of acquiring less than the entire right, title and interest in the same;

The extent (by percentage) of ownership interest is 100 %

Now, therefore, in consideration of the sum of One dollars (\$ 1.00), the receipt whereof is acknowledged, and other good and valuable consideration, the assignor by these presents do sell, assign and transfer unto said assignee the entire right to the said invention in the United States and the rights, title and interest in and to any and all Patents which may be granted therefore in the United States consistent with ownership interest.

In re Application of: see attachment, Exhibit A
Serial No.: see attachment, Exhibit A

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The undersigned do hereby declare that all statements made herein are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DELTA ELECTRONICS, INC.

Assignor

Karl Yeh 10/19/2022

Signature

Name: Kuoliang YEH

Title: General Counsel

No. 252, Shanying Rd., Guishan Dist., Taoyuan City 333, Taiwan, R.O.C.
Address

.....
Date

Exhibit A

Patents and Patent Applications Assigned to Ancora Semiconductors Inc.

No.1	Title	Filing Date	Serial No	Date of Patent	Patent No.
1	HETEROJUNCTION SEMICONDUCTOR DEVICE FOR REDUCING PARASITIC CAPACITANCE	2017/02/10	15/429,184	2019/03/19	10,236,236
2	Heterojunction Semiconductor Device for Reducing Parasitic Capacitance	2016/10/18	15/297,123	2018/09/25	10,084,076
3	POWER SEMICONDUCTOR DEVICE INTEGRATED WITH ESD PROTECTION CIRCUIT UNDER SOURCE PAD, DRAIN PAD, AND/OR GATE PAD	2017/03/24	15/468,133	2020/05/26	10,665,709
4	HETEROJUNCTION SEMICONDUCTOR DEVICE HAVING SOURCE AND DRAIN PADS WITH IMPROVED CURRENT CROWDING	2017/08/15	15/678,102	2020/11/10	10,833,185
5	Heterojunction Semiconductor Device for Reducing Parasitic Capacitance	2018/07/23	16/041,848	2019/11/05	10,468,516
6	HETEROJUNCTION SEMICONDUCTOR DEVICE FOR REDUCING PARASITIC CAPACITANCE	2018/12/27	16/233,115	2021/03/16	10,930,524
7	SEMICONDUCTOR DEVICE HAVING REDUCED CAPACITANCE BETWEEN SOURCE AND DRAIN PADS	2019/08/26	16/530,293	2021/02/02	10,910,491
8	Heterojunction Semiconductor Device for Reducing Parasitic Capacitance	2019/09/25	16/581,781	2020/02/25	10,573,736
9	SEMICONDUCTOR DEVICE	2020/12/14	17/121,706	N/A	N/A
10	SWITCHING CIRCUIT AND CURRENT COMPENSATING METHOD THEREIN	2016/01/05	14/988,703	2017/04/11	9,621,155
11	DRIVING CIRCUIT AND DRIVING METHOD	2015/12/22	14/977,662	2017/05/23	9,660,637
12	PACKAGING STRUCTURE	2016/02/25	15/052,899	2017/08/29	9,748,165
13	TRANSISTOR WITH A GATE METAL LAYER HAVING VARYING WIDTH	2016/08/15	15/236,497	2019/04/02	10,249,725
14	AUXILIARY CIRCUIT	2021/03/09	17/195,663	2022/06/14	11,362,654
15	AUXILIARY CIRCUIT AND POWER CONVERTER	2018/12/20	16/226,673	2021/04/06	10,972,093
16	CONVERSION CIRCUIT AND CONVERSION CIRCUITRY	2019/08/01	16/538,675	2020/09/22	10,784,768
17	CONVERSION CIRCUIT	2019/11/14	16/683,283	2020/09/22	10,784,770
18	CONVERSION CIRCUIT	2020/06/20	16/907,174	2022/04/19	11,309,887
19	CONVERSION CIRCUIT	2018/12/28	16/234,598	2020/08/04	10,734,882
20	CHIP PACKAGING WITH MULTILAYER CONDUCTIVE CIRCUIT	2020/04/12	16/846,397	2021/11/30	11,189,555
21	CONVERSION CIRCUIT	2019/08/21	16/547,561	2020/09/22	10,784,795
22	CONVERSION CIRCUIT	2022/06/27	17/809,011	N/A	N/A

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RECORDED: 11/04/2022

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