PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7712273

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
COHERENT LOGIX, INCORPORATED	12/23/2022

RECEIVING PARTY DATA

Name:	ACP POST OAK CREDIT I LLC
Street Address:	777 POST OAK BLVD SUITE 430
City:	HOUSTON
State/Country:	TEXAS
Postal Code:	77056

PROPERTY NUMBERS Total: 60

Property Type	Number
Patent Number:	7415594
Patent Number:	7761817
Patent Number:	7937558
Patent Number:	7949969
Patent Number:	7987338
Patent Number:	7987339
Patent Number:	8112612
Patent Number:	8171436
Patent Number:	8230408
Patent Number:	8438510
Patent Number:	8478964
Patent Number:	8552770
Patent Number:	5406369
Patent Number:	8644431
Patent Number:	8761318
Patent Number:	8788989
Patent Number:	8826228
Patent Number:	8832413
Patent Number:	8880866
Patent Number:	8963599

Property Type	Number
Patent Number:	9008242
Patent Number:	9134698
Patent Number:	9154142
Patent Number:	9195575
Patent Number:	9250867
Patent Number:	9252920
Patent Number:	9292464
Patent Number:	9323714
Patent Number:	9325329
Patent Number:	9424441
Patent Number:	9424213
Patent Number:	9430422
Patent Number:	9430369
Patent Number:	9442461
Patent Number:	9450590
Patent Number:	9477585
Patent Number:	9535877
Patent Number:	9558150
Patent Number:	9612984
Patent Number:	9720867
Patent Number:	9904542
Patent Number:	10114739
Patent Number:	9965258
Patent Number:	9990241
Patent Number:	9990227
Patent Number:	10007806
Patent Number:	10007293
Patent Number:	10110345
Patent Number:	10185608
Patent Number:	10185672
Patent Number:	10327235
Patent Number:	10383106
Patent Number:	10521285
Patent Number:	10536305
Patent Number:	10560932
Patent Number:	10592233
Patent Number:	10594438
Patent Number:	10685143

Property Type	Number
Patent Number:	10691451
Patent Number:	11063697

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ATTORNEY DOCKET NUMBER:	092132.0102
NAME OF SUBMITTER:	THAO TON
SIGNATURE:	/Thao Ton/
DATE SIGNED:	12/23/2022

Total Attachments: 16
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PATENT SECURITY AGREEMENT

This PATENT SECURITY AGREEMENT (this "Agreement"), dated as of December 23, 2022, is made by Coherent Logix, Incorporated (the "Grantor") in favor of ACP Post Oak Credit I LLC, as Collateral Agent (in such capacity, together with its successors and assigns in such capacity, the "Collateral Agent").

Recitals

The Collateral Agent, Coherent Logix, Incorporated and the Lenders from time to time party thereto have entered into a Senior Secured Term Loan Credit Agreement, dated as of December 23, 2022 (as amended, restated, supplemented or otherwise modified from time to time, the "Credit Agreement").

Pursuant to the Credit Agreement and as a condition to the extension of credit by the Lenders under the Credit Agreement, the Grantor executed and delivered a Guarantee and Collateral Agreement, dated as of December 23, 2022 (the "Collateral Agreement"), in favor of the Collateral Agent for the ratable benefit of the Secured Parties.

The Grantor solely and exclusively owns the patents and patent applications listed on Schedule A attached hereto (the "Patents"), which Patents have been issued by or are pending applications in the United States Patent and Trademark Office.

This Agreement has been executed in conjunction with the security interest granted under the Collateral Agreement to the Collateral Agent for the ratable benefit of the Secured Parties. In the event that any provisions of this Agreement are deemed to conflict with the Collateral Agreement, the provisions of the Collateral Agreement shall govern.

Agreement

NOW, THEREFORE, in consideration of the mutual covenants and agreements set forth herein and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, it is hereby agreed that:

1. Definitions. Unless otherwise indicated, all capitalized terms not defined herein shall have the respective meaning given to them in the Collateral Agreement.

2. The Security Interest. The Grantor hereby pledges, assigns and transfers to the Collateral Agent, and grants to the Collateral Agent, for the ratable benefit of the Secured Parties, a security interest in all of the following property, now owned or at any time hereafter acquired by the Grantor or in which the Grantor now has or at any time in the future may acquire any right, title or interests and whether now existing or hereafter coming into existence: (1) any and all patents and patent applications, including the Patents; (2) all inventions and improvements described and claimed therein; (3) all reissues, reexaminations, divisionals, continuations, renewals, extensions and continuations-in-part thereof; (4) all income, royalties, damages, claims and payments now or hereafter due or payable under and with respect thereto, including, without limitation, damages and payments for past and future infringements thereof; (5) all rights to sue for past, present and future infringements thereof; (6) all rights corresponding to any of the foregoing throughout the world; and (7) all Proceeds of the foregoing.

3. Governing Law. **THIS AGREEMENT SHALL BE GOVERNED BY, AND CONSTRUED IN ACCORDANCE WITH, THE LAWS OF THE STATE OF NEW YORK.**

****

IN WITNESS WHEREOF, the Grantor has executed this Agreement by its duly authorized representative as of the date first written above.

GRANTOR

COHERENT LOGIX, INCORPORATED

By: _____
Name: Michael Doerr
Title: Chief Executive Officer

Acknowledged and Agreed:

ACP POST OAK CREDIT I LLC
as Collateral Agent

By: _____
Name: Matthew E. Laterza
Title: Chief Operating Officer

Schedule A

Patents

Title	Serial No.	Date Filed	Patent No.	Date Issued
Processing System with Interspersed Stall Propagating Processors and Communication Elements	10/602,292	6/24/2003	7,415,594	8/19/2008
Processing System with Interspersed Processors and Communication Elements	2004-517818	12/27/2004	4,391,935	10/6/2009
Programming A Multi-Processor System	7759497.60	9/27/2008	2,008,182	5/12/2010
Programming A Multi-Processor System	602007006467.8-08		2,008,182	5/12/2010
Programming A Multi-Processor System			2,008,182	5/12/2010
Programming A Multi-Processor System			2,008,182	5/12/2010
Designing an ASIC Based on Execution of a Software Program on a Processing System	11/751,994	5/22/2007	7,761,817	7/20/2010
Processing System with Interspersed Processors and Communication Elements	3742194.80	1/25/2005	1,520,233	8/18/2010
Processing System with Interspersed Processors and Communication Elements	60333837.2-08		1,520,233	8/18/2010
Processing System with Interspersed Processors and Communication Elements			1,520,233	8/18/2010
Processing System with Interspersed Processors and Communication Elements			1,520,233	8/18/2010
Method and System for Execution of Hardware Description Language (HDL) Programs	2007-519350	12/15/2006	4,676,981	2/4/2011
Processing System with Interspersed Processors and Communication Elements (Continuation of 5860-00101)	12/028,565	2/8/2008	7,937,558	5/3/2011
Designing an ASIC Based on Execution of a Software Program on a Processing System (Continuation of 5860-00501)	12/837,767	7/16/2010	7,949,969	5/24/2011
Processing System with Interspersed Processors Using Shared Memory of Communication Elements (Continuation of 5860-00105; Similar To EP Div 5860-00106)	12/781,314	5/17/2010	7,987,338	7/26/2011
Processing System with Interspersed Processors and Dynamic Pathway Creation (Continuation of 5860-00105; Similar to EP Div 5860-00107)	12/827,416	6/30/2010	7,987,339	7/26/2011

Designing an ASIC Based on Execution of a Software Program on a Processing System	200780027938.00	11/22/2008	200,780,027,938	10/5/2011
Processing System with Interspersed Processors Using Selective Data Transfer Through Communication Elements (Continuation of 5860-00105; Similar to EP Div 5860-00109)	12/781,422	5/17/2010	8,112,612	2/7/2012
Converting Portions of a Software Program Executing on a Processing System to Hardware Descriptions (Continuation of 5860-00506)	13/110,248	5/18/2011	8,171,436	5/1/2012
Designing an ASIC Based on Execution of a Software Program on a Processing System	2009-512266	11/22/2008	5,009,979	6/12/2012
Multiprocessor with Interconnection Network Using Shared Memory (Divisional of 5860-00103)	10164530.70	5/31/2010	2,224,345	6/20/2012
Multiprocessor with Interconnection Network Using Shared Memory	60341376.50		2,224,345	6/20/2012
Multiprocessor with Interconnection Network Using Shared Memory			2,224,345	6/20/2012
Multiprocessor with Interconnection Network Using Shared Memory			2,224,345	6/20/2012
Execution of Hardware Description Language (HDL) Programs	11/168,794	6/28/2005	8,230,408	7/24/2012
Partial Hardening of a Software Program from a Software Implementation to a Hardware Implementation (Continuation Of 5860-00507	13/431,029	3/27/2012	8,438,510	5/7/2013
Stall Propagation in a Processing System with Interspersed Processors and Communication Elements (Continuation of 5860-00112)	13/341,252	12/30/2011	8,478,964	7/2/2013
Programming A Multi-Processor System	200780019634.X	9/27/2008	ZL200780019634.X	9/4/2013
Frequency Divider with Synchronous Range Extension Across Octave Boundaries	13/356,995	1/24/2012	8,552,770	10/8/2013
Multiprocessor System with Specific Pathways Creation (Divisional of 5860-00103)	10168942.00	7/8/2010	2,239,667	10/16/2013
Multiprocessor System with Specific Pathways Creation (German Counterpart of 5860-00107)	60345116.00		2,239,667	10/16/2013
Multiprocessor System with Specific Pathways Creation (French Counterpart of 5860-00107)			2,239,667	10/16/2013
Multiprocessor System with Specific Pathways Creation (Great Britain Counterpart of 5860-00107)			2,239,667	10/16/2013
Parallel Execution of Trellis-Based Methods	2012-516288	12/14/2011	5,406,369	11/8/2013

Parallel Execution of Trellis-Based Methods	12/817,318	6/17/2010	8,644,431	2/4/2014
Parallel Execution of Trellis-Based Methods (Continuation of 5860-01501)	13/734,325	1/4/2013	8,761,318	6/24/2014
Developing a Hardware Description Which Performs a Function By Partial Hardening of a Software Program on a Multi-Processor System (Continuation of 5860-00508)	13/862,842	4/15/2013	8,788,989	7/22/2014
Programming A Multi-Processor System	11/691,889	3/27/2007	8,826,228	9/2/2014
Processing System with Interspersed Processors and Communication Elements Having Improved Wormhole Routing (Continuation of 5860-00116)	13/904,359	5/29/2013	8,832,413	9/9/2014
Parallel Execution of Trellis-Based Methods (Divisional of 5860-01505)	2013-226842	10/31/2013	5,635,668	10/24/2014
Multiprocessor with Specific Architecture of Communication Elements (Divisional of 5860-00103)	10166234.40	6/16/2010	2,237,165	10/29/2014
Multiprocessor with Specific Architecture of Communication Elements	60346931.00		2,237,165	10/29/2014
Multiprocessor with Specific Architecture of Communication Elements			2,237,165	10/29/2014
Multiprocessor with Specific Architecture of Communication Elements			2,237,165	10/29/2014
Method and System for Disabling Communication Paths in a Multiprocessor Fabric by Setting Register Values to Disable the Communication Paths Specified by a Configuration	13/274,138	10/14/2011	8,880,866	11/4/2014
Frequency Divider with Synchronous Range Extension Across Octave Boundaries			2,668,723	11/26/2014
Frequency Divider with Synchronous Range Extension Across Octave Boundaries			2,668,723	11/26/2014
Frequency Divider with Synchronous Range Extension Across Octave Boundaries			2,668,723	11/26/2014
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems	14/106,269	12/13/2013	8,963,599	2/24/2015
Parallel Execution of Trellis-Based Methods	201080026721.00	12/16/2011	ZL201080026721.X	4/1/2015
Parallel Execution of Trellis-Based Methods Using Overlapping Sub-Sequences, (Continuation of 5860-01506)	14/273,278	5/8/2014	9,008,242	4/14/2015
System with Interspersed Processors and Configurable Communication Elements			2,237,164	8/9/2015
System with Interspersed Processors and Configurable Communication Elements			2,237,164	8/9/2015
System with Interspersed Processors and Configurable Communication Elements			2,237,164	8/9/2015

Multiprocessor with Specific Handling of Stalling Devices (Divisional of 5860-00103)	10165363.20	6/9/2010	2,237,164	8/19/2015
Three Dimensional Display Compute System	13/590,086	8/20/2012	9,134,698	9/15/2015
Disabling Communication in a Multiprocessor System	2013-534050	4/8/2013	5,815,717	10/2/2015
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems (Continuation of 5860-03800)	14/626,441	2/19/2015	9,154,142	10/6/2015
Frequency Divider with Synchronous Range Extension Across Octave Boundaries	2013-551286	6/24/2013	5,837,617	11/13/2015
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System	13/896,577	5/17/2013	9,195,575	11/24/2015
Parallel Execution of Trellis-Based Methods (Divisional of 5860-01507)	2014-211484	10/16/2014	5,873,154	1/22/2016
Programming A Multi-Processor System (Continuation of 5860-00401)	14/284,573	5/22/2014	9,250,867	2/2/2016
Parallel Processing of Overlapping Subsequences to Generate Soft Estimates (Continuation of 5860-01508)	14/633,666	2/27/2015	9,252,920	2/2/2016
Multiprocessor Systems with Improved Secondary Interconnection Network	14/086,648	11/21/2013	9,292,464	3/22/2016
Processing System with Synchronization Instruction	14/051,140	10/10/2013	9,323,714	4/26/2016
Automatic Selection of On-Chip Clock in Synchronous Digital Systems	14/106,202	12/13/2013	9,325,329	4/26/2016
Secondary Interconnection Network Improvements (Germany validation of 5860-02904)			2,932,398	7/13/2016
Secondary Interconnection Network Improvements (French validation of 5860-02904)			2,932,398	7/13/2016
Secondary Interconnection Network Improvements (British validation of 5860-02904)			2,932,398	7/13/2016
Multiprocessor Fabric Having Configurable Communication that is Selectively Disabled for Secure Processing (Continuation of 5860-01701)	14/504,960	10/2/2014	9,424,441	8/23/2016
Processing System With Interspersed Processors DMA-FIFO	13/791,345	3/8/2013	9,424,213	8/23/2016
Disabling Communication in a Multiprocessor System	201180049630.20	4/15/2013	ZL201180049630.2	8/24/2016
Processing System With Interspersed Processors With Multi-Layer Interconnect	13/851,683	3/27/2013	9,430,422	8/30/2016
Memory-Network Processor with Programmable Optimizations	14/285,838	5/23/2014	9,430,369	8/30/2016

Three Dimensional Display System	14/828,224	8/17/2015	9,442,461	9/13/2016
Clock Distribution Network for Multi-Frequency Multi-Processor Systems	14/106,138	12/13/2013	9,450,590	9/20/2016
Frequency Divider with Synchronous Range Extension Across Octave Boundaries	201280003904.90	1/24/2012	ZL201280003904.9	9/28/2016
Real Time Analysis and Control for a Multiprocessor System	14/074,925	11/8/2013	9,477,585	10/25/2016
Processing System With Interspersed Processors DMA-FIFO			2,923,279	11/2/2016
Processing System With Interspersed Processors DMA-FIFO			2,923,279	11/2/2016
Processing System With Interspersed Processors DMA-FIFO			2,923,279	11/2/2016
Processing System With Interspersed Processors With Multi-Layer Interconnect (German validation of 5860-02504)			2,932,275	11/2/2016
Processing System With Interspersed Processors With Multi-Layer Interconnect (French validation of 5860-02504)			2,932,275	11/2/2016
Processing System With Interspersed Processors With Multi-Layer Interconnect (UK validation of 5860-02504)			2,932,275	11/2/2016
Processing System with Interspersed Processors and Communication Elements Having Improved Communication Routing (Continuation of 5860-00120)	14/451,900	8/5/2014	9,535,877	1/3/2017
Programming A Multi-Processor System (Divisional of 5860-00405)	201310366809.10	8/21/2013	ZL201310366809.1	1/18/2017
Processing System with Synchronization Instruction, (Continuation of 5860-02201)	15/073,276	3/17/2016	9,558,150	1/31/2017
Automatic Selection of On-Chip Clock in Synchronous Digital Systems	13817791.00	6/25/2015	2,932,345	3/1/2017
Automatic Selection of On-Chip Clock in Synchronous Digital Systems			2,932,345	3/1/2017
Automatic Selection of On-Chip Clock in Synchronous Digital Systems			2,932,345	3/1/2017
Automatic Selection of On-Chip Clock in Synchronous Digital Systems			2,932,345	3/1/2017
Clock Distribution Network for Multi-Frequency Multi-Processor Systems			2,932,346	3/15/2017
Clock Distribution Network for Multi-Frequency Multi-Processor Systems			2,932,346	3/15/2017
Clock Distribution Network for Multi-Frequency Multi-Processor Systems			2,932,346	3/15/2017
Secondary Interconnection Network Improvements, (Continuation of 5860-02901)	15/043,905	2/15/2016	9,612,984	4/4/2017
3D Display Compute System	201280038749.40	2/8/2014	ZL201280038749.4	6/6/2017

Processing System With Interspersed Processors DMA-FIFO	201380060488.00	5/20/2015	ZL201380060488.0	7/4/2017
Processing System With Interspersed Processors DMA-FIFO	2015-544053	5/21/2015	6,122,135	7/4/2017
Processing System With Interspersed Processors With Multi-Layer Interconnect (Continuation of 5860-02501)	15/219,095	7/25/2016	9,720,867	8/1/2017
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems			2,932,600	8/2/2017
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems			2,932,600	8/2/2017
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems			2,932,600	8/2/2017
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			2,997,469	8/23/2017
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			2,997,469	8/23/2017
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			2,997,469	8/23/2017
Secondary Interconnection Network Improvements	201380070450.10	7/15/2015	ZL201380070450.1	10/10/2017
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System	2016-513913	11/17/2015	6,228,294	10/20/2017
Automatic Selection of On-Chip Clock in Synchronous Digital Systems	201380065382.X	6/12/2015	ZL201380065382.X	10/27/2017
Processing System With Interspersed Processors With Multi-Layer Interconnect	201380060554.40	5/20/2015	ZL201380060554.4	11/14/2017
System with Interspersed Processors and Configurable Communication Elements	15181012.40	8/13/2015	2,977,911	11/22/2017
System with Interspersed Processors and Configurable Communication Elements			2,977,911	11/22/2017
System with Interspersed Processors and Configurable Communication Elements			2,977,911	11/22/2017
System with Interspersed Processors and Configurable Communication Elements			2,977,911	11/22/2017
A Distributed Architecture for Encoding and Delivering Video Content	2015-517368	12/12/2014	6,247,286	11/24/2017
Real Time Analysis and Control for a Multiprocessor System	2015-541913	5/11/2015	6,290,913	2/16/2018
Multiprocessor Programming Toolkit for Design Reuse	14/047,135	10/7/2013	9,904,542	2/27/2018
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems	201380065071.30	6/12/2015	ZL201380065071.3	3/27/2018
Real Time Analysis and Control for a Multiprocessor System, (Continuation of 5860-02801)	15/276,370	9/26/2016	10,114,739	4/30/2018

Programming A Multi-Processor System (Continuation of 5860-00410)	14/972,815	12/17/2015	9,965,258	5/8/2018
Clock Distribution Network for Multi-Frequency Multi-Processor Systems	201380065370.70	6/12/2015	ZL201380065370.7	5/18/2018
Secondary Interconnection Network Improvements	2015-547381	6/12/2015	6,341,930	5/25/2018
Disabling Communication in a Multiprocessor System	11776050.40	5/14/2013	2,628,090	5/30/2018
Disabling Communication in a Multiprocessor System	602011048853.8		2,628,090	5/30/2018
Disabling Communication in a Multiprocessor System			2,628,090	5/30/2018
Disabling Communication in a Multiprocessor System			2,628,090	5/30/2018
Processing System With Interspersed Processors With Multi-Layer Interconnect (Continuation of 5860-02506)	15/631,925	6/23/2017	9,990,241	6/5/2018
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System (Continuation of 5860-03000)	14/921,281	10/23/2015	9,990,227	6/5/2018
Parallel Execution of Trellis-Based Methods	201510086662.X	2/25/2015	ZL201510086662.X	6/8/2018
Real Time Analysis and Control for a Multiprocessor System	201380065983.00	6/17/2015	ZL201380065983.0	6/19/2018
Secure Boot Sequence for Selectively Disabling Configurable Communication Paths of a Multiprocessor Fabric (Continuation of 5860-01706)	15/099,275	4/14/2016	10,007,806	6/26/2018
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (Continuation of 5860-02101)	15/253,372	8/31/2016	10,007,293	6/26/2018
Multi-Frequency Clock Skew Control for Inter-Chip Communication in Synchronous Digital Systems	2015-548013	6/5/2015	6,389,188	8/24/2018
Memory-Network Processor with Programmable Optimizations	201480039082.90	1/8/2016	ZL201480039082.9	9/5/2018
Multiprocessor Programming Toolkit for Design Reuse	201380067521.30	6/23/2015	ZL201380067521.2	9/18/2018
Processing System With Interspersed Processors DMA-FIFO	2017-67386	3/30/2017	6,412,975	10/5/2018
Path Sort Techniques in a Polar Code Successive Cancellation List Decoder (Continuation of 5860-04703)	15/959,012	4/20/2018	10,110,345	10/23/2018
Processing System With Interspersed Processors With Multi-Layer Interconnect	2015-544057	5/25/2015	6,453,759	12/21/2018
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System	2017-198250	10/12/2017	6,453,971	12/21/2018
Real Time Analysis and Control for a Multiprocessor System, (German validation of of 5860-02804)			2,917,837	1/2/2019

Real Time Analysis and Control for a Multiprocessor System, (French validation of 5860-02804)			2,917,837	1/2/2019
Real Time Analysis and Control for a Multiprocessor System, (UK validation of 5860-02804)			2,917,837	1/2/2019
Processing System with Synchronization Instruction	13785989.80	5/12/2015	2,929,434	1/16/2019
Processing System with Synchronization Instruction			2,929,434	1/16/2019
Processing System with Synchronization Instruction			2,929,434	1/16/2019
Processing System with Synchronization Instruction			2,929,434	1/16/2019
Processing System With Interspersed Processors With Multi-Layer Interconnect (Continuation of 5860-02511)	15/986,701	5/22/2018	10,185,608	1/22/2019
Multiprocessor System with Improved Secondary Interconnection Network (Continuation of 5860-02906)	15/437,343	2/20/2017	10,185,672	1/22/2019
A Distributed Architecture for Encoding and Delivering Video Content	2017-220753	11/16/2017	6,473,213	2/1/2019
Clock Distribution Network for Multi-Frequency Multi-Processor Systems	17159612.50	3/7/2017	3,200,042	2/6/2019
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (Validation of 5860-02107)			3,200,042	2/6/2019
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (Validation of 5860-02107)			3,200,042	2/6/2019
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (Validation of 5860-02107)			3,200,042	2/6/2019
Multiprocessor Fabric Having Configurable Communication that is Selectively Disabled for Secure Processing	201610565613.90	7/18/2016	ZL201610565613.9	6/4/2019
Scrambling Sequence Design for Multi-Mode Block Discrimination on DCI Blind Detection	15/852,632	12/22/2017	10,327,235	6/18/2019
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System (Claiming Priority to PCT/US13/41942)	201380077900.00	12/29/2015	ZL201380077900.X	7/2/2019
Processing System with Synchronization Instruction	201380063373.70	6/5/2015	ZL201380063373.7	7/16/2019
Scrambling Sequence Design for Embedding UE ID into Frozen Bits for DCI Blind Detection	15/852,761	12/22/2017	10,383,106	8/13/2019
Processing System with Synchronization Instruction	2018-63728	3/30/2018	6,574,865	8/23/2019

Secondary Interconnection Network Improvements (validation of 5860-02907),			3,109,769	10/16/2019
Secondary Interconnection Network Improvements (validation of 5860-02907),			3,109,769	10/16/2019
Secondary Interconnection Network Improvements (validation of 5860-02907),			3,109,769	10/16/2019
Secondary Interconnection Network Improvements (Divisional of 5860-02905)	2018-93528	5/16/2018	6,603,363	10/18/2019
A Distributed Architecture for Encoding and Delivering Video Content	201380038883.90	1/21/2015	ZL201380038883.9	11/19/2019
Method and System for Execution of Hardware Description Language (HDL) Programs	5762106.20	6/28/2005	1,766,544	12/4/2019
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			3,279,793	12/4/2019
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			3,279,793	12/4/2019
Dynamic Reconfiguration of Applications on a Multi-Processor Embedded System			3,279,793	12/4/2019
Processing System With Interspersed Processors With Multi-Layer Interconnect (Continuation of 5860-02512)	16/252,904	1/21/2019	10,521,285	12/31/2019
Path Sort Techniques in a Polar Code Successive Cancellation List Decoder (Continuation of 5860-04703)			3,381,128	1/1/2020
Path Sort Techniques in a Polar Code Successive Cancellation List Decoder (Continuation of 5860-04703)			3,381,128	1/1/2020
Path Sort Techniques in a Polar Code Successive Cancellation List Decoder (Continuation of 5860-04703)			3,381,128	1/1/2020
Scrambling Sequence Design for Multi-Mode Block Discrimination on DCI Blind Detection	16/055,380	8/6/2018	10,536,305	1/14/2020
Real Time Analysis and Control for a Multiprocessor System	2018-021127	2/8/2018	6,652,581	1/27/2020
Scrambling Sequence Design for Embedding UE ID into Frozen Bits for DCI Blind Detection	16/459,072	7/1/2019	10,560,932	2/11/2020
Multiprocessor Programming Toolkit for Design Reuse	15/872,421	1/16/2018	10,592,233	3/17/2020
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution	15/972,752	5/7/2018	10,594,438	3/17/2020
Disabling Communication in a Multiprocessor System	18168964.70	4/24/2018	3,432,152	3/18/2020
Disabling Communication in a Multiprocessor System	602011065773.9		3,432,152	3/18/2020
Disabling Communication in a Multiprocessor System			3,432,152	3/18/2020

Disabling Communication in a Multiprocessor System			3,432,152	3/18/2020
Processor Instructions to Accelerate FEC Encoding and Decoding			3,398,053	3/25/2020
Processor Instructions to Accelerate FEC Encoding and Decoding			3,398,053	3/25/2020
Processor Instructions to Accelerate FEC Encoding and Decoding			3,398,053	3/25/2020
Processing System with Interspersed Processors DMA-FIFO (Divisional of 5860-02403)	201710413773.60	6/5/2017	ZL201710413773.6	5/5/2020
A Distributed Architecture for Encoding and Delivering Video Content	2019-10054	1/24/2019	6,703,150	5/11/2020
Secure Boot Sequence for Selectively Disabling Configurable Communication Paths of a Multiprocessor Fabric (Continuation of 5860-01707)	15/996,709	6/4/2018	10,685,143	6/16/2020
Processor Instructions to Accelerate FEC Encoding and Decoding	15/390,910	12/27/2016	10,691,451	6/23/2020
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (Divisional of 5860-02107)	19153565.70	1/24/2019	3,493,017	8/5/2020
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (validation of 5860-02112)			3,493,017	8/5/2020
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (validation of 5860-02112)			3,493,017	8/5/2020
Clock Distribution Network for Multi-Frequency Multi-Processor Systems (validation of 5860-02112)			3,493,017	8/5/2020
A Distributed Architecture for Encoding and Delivering Video Content	13732021.40	1/5/2015	2,859,729	9/16/2020
A Distributed Architecture for Encoding and Delivering Video Content			2,859,729	9/16/2020
A Distributed Architecture for Encoding and Delivering Video Content			2,859,729	9/16/2020
A Distributed Architecture for Encoding and Delivering Video Content			2,859,729	9/16/2020
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution	18733373.70	11/25/2019	3,622,646	10/21/2020
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution			3,622,646	10/21/2020
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution			3,622,646	10/21/2020
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution			3,622,646	10/21/2020
Processing System With Interspersed Processors With Multi-Layer Interconnect (Divisional of 5860-02504)	16196289.90	10/28/2016	3,151,128	11/4/2020

Processing System With Interspersed Processors With Multi-Layer Interconnect (Divisional of 5860-02504)			3,151,128	11/4/2020
Processing System With Interspersed Processors With Multi-Layer Interconnect (Divisional of 5860-02504)			3,151,128	11/4/2020
Processing System With Interspersed Processors With Multi-Layer Interconnect (Divisional of 5860-02504)			3,151,128	11/4/2020
Automatic Selection of On-Chip Clock in Synchronous Digital Systems	2015-548010	6/5/2015	6,801,959	11/30/2020
Multi-Processor Architecture with Improved Log Probability Calculation	107139222	11/5/2018	I714903	1/1/2021
Multiprocessor Programming Toolkit for Design Reuse	13780017.3	6/2/2015	2,917,827	1/6/2021
Multiprocessor Programming Toolkit for Design Reuse	602013075167.6		2,917,827	1/6/2021
Multiprocessor Programming Toolkit for Design Reuse			2,917,827	1/6/2021
Multiprocessor Programming Toolkit for Design Reuse			2,917,827	1/6/2021
Low Latency Video Codec and Transmission with Parallel Processing	107144864.00	12/12/2018	I718452	2/11/2021
Processing System With Interspersed Processors With Multi-Layer Interconnect (Divisional of 5860-02505)	2018-233619	12/13/2018	6,856,612	3/22/2021
3D Display Compute System	12751709.20	3/17/2014	2,745,176	5/5/2021
3D Display Compute System	12751709.20	3/17/2014	2,745,176	5/5/2021
3D Display Compute System	12751709.20	3/17/2014	2,745,176	5/5/2021
3D Display Compute System	12751709.20	3/17/2014	2,745,176	5/5/2021
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution	16/737,021	1/8/2020	11/063,697	7/13/2021
Real Time Analysis and Control for a Multiprocessor System	201810480764.3	5/18/2018	ZL201810480764.3	9/7/2021
Secondary Interconnection Network Improvements	2019-186694	10/10/2019	6,959,310	10/11/2021
Processing System With Interspersed Processors DMA-FIFO (Divisional of 5860-02404)	16196406.90	10/28/2016	3,142,016	10/13/2021
Processing System With Interspersed Processors DMA-FIFO (Divisional of 5860-02404)	602013079669.6	10/28/2016	3,142,016	10/13/2021
Processing System With Interspersed Processors DMA-FIFO (Divisional of 5860-02404)	16196406.90	10/28/2016	3,142,016	10/13/2021

Processing System With Interspersed Processors DMA-FIFO (Divisional of 5860-02404)	16196406.90	10/28/2016	3,142,016	10/13/2021
Memory Management and Path Sort Techniques in a Polar Code Successive Cancellation List Decoder	2018-525737	5/17/2018	6,974,319	11/8/2021
Clock Distribution Network for Multi-Frequency Multi-Processor Systems	201810356704.00	4/20/2018	ZL201810356704.0	11/26/2021
Enhanced Polarization Weighting to Enable Scalability in Polar Code Bit Distribution	107115632.00	5/8/2018	I750372	12/21/2021
Scrambling Sequence Design for Multi-Mode Block Discrimination on DCI Blind Detection	18756134.5	1/30/2020	3,688,908	12/29/2021
Any World View Generation	19784182.8	11/12/2020	3,776,485	1/26/2022
Any World View Generation	19784182.8	11/12/2020	3,776,485	1/26/2022
Any World View Generation	19784182.8	11/12/2020	3,776,485	1/26/2022
Any World View Generation	19784182.8	11/12/2020	3,776,485	1/26/2022
Real Time Analysis and Control for a Multiprocessor System	2020-9082	2/12/2020	7,053,691	4/4/2022
A Distributed Architecture for Encoding and Delivering Video Content	201911002072.90	10/21/2019	ZL201911002072.9	4/12/2022