PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
DONGGUAN CHANGGONG MICROELECTRONICS LTD	01/01/2023

RECEIVING PARTY DATA

Name:	INNOVISION SEMICONDUCTOR INC.
Street Address:	401, 8# BUILDING, INNOVATION SCI&TECH PARK
Internal Address:	SONGSHAN LAKE HIGH TECH DEVELOPMENT ZONE
City:	DONGGUAN
State/Country:	CHINA
Postal Code:	523808

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17339995

CORRESPONDENCE DATA

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Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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ATTORNEY DOCKET NUMBER:	006
NAME OF SUBMITTER:	MARK LUO
SIGNATURE:	/Mark Luo/
DATE SIGNED:	03/13/2023

Total Attachments: 3
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ASSIGNMENT OF INVENTION

This Assignment of Invention (the "**Assignment**") is between DONGGUAN CHANGGONG MICROELECTRONICS LTD., a corporation duly organized in the People's Republic of China and having a place of business at 401, 8# Building, Innovation Sci&Tech Park, SongShan Lake High Tech Development Zone, Dongguan, Guangdong, China 523808 (the "**Assignor**") and INNOVISION SEMICONDUCTOR INC., a corporation duly organized in the People's Republic of China and having a place of business at 401, 8# Building, Innovation Sci&Tech Park, SongShan Lake High Tech Development Zone, Dongguan, Guangdong, China 523808 (the "**Assignee**") and is effective as of the latest date in the signature block below. Assignor and Assignee may be referred to, individually, as a "**Party**" or collectively, as the "**Parties**".

WHEREAS, Assignor has legally changed its operating name to Assignee, and Assignor remains the same legal entity as the Assignee;

WHEREAS, GUANGHUA YE is the inventor of the concepts and technologies known as "SYNCHRONOUS CLOCK GENERATOR CIRCUIT FOR MULTIPHASE DC-DC CONVERTER" under the Patent Application No. 17,339,995 (filed on 06-05-2021) and more specifically described in Exhibit A attached hereto (collectively referred to as the "**Invention**");

WHEREAS, Assignor is the lawful owner of all proprietary rights, including, but not limited to, patents, copyrights, trade secrets, trademarks, and other associated good will, registrations, and rights in the Invention (collectively, the "**Rights**"); and

WHEREAS, Assignee wish to acquire the ownership of the Rights to the Invention.

NOW, THEREFORE for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Parties hereto agree as follows:

Assignor irrevocably assigns to Assignee all Rights, title, interest, and other rights in the Invention including, but not limited to:

(1) all copyrights, trade secrets, trademarks and associated good will and all patents which may be granted on the Invention;
(2) all applications for patents (including divisions, continuations in whole or part or substitute applications) in the United States or any foreign countries whose duty it is to issue such patents;
(3) any reissues and extensions of such patents; and
(4) all priority rights under the International Convention for the Protection of Industrial Property for every member country.

Assignor represents and warrants that: (1) Assignor is the only current legal owner of all Rights, title, interest, and other rights in the Invention; (2) such Rights, title, interest, and other rights in the Invention have not been previously licensed, pledged, assigned, or encumbered in any way, shape, or form to any party other than Assignor; and (3) this Assignment does not infringe on the rights of any other person. Assignor agrees to fully cooperate with Assignee and to execute and deliver all papers, instruments, and assignments as may be necessary to vest all Rights, title, interest, and other rights in the Invention in Assignor. Assignor further agrees to testify in any legal proceedings, sign all lawful papers and applications, and make all rightful oaths and generally do everything possible to aid Assignee to obtain and enforce proper protection for the Invention in all countries.

Each Party acknowledges and represents that each Party has carefully read and fully understands all of the terms and conditions set forth in this Assignment including, without limitation, seeking of independent legal advice with respect to the terms and conditions of this Assignment. Each Party further acknowledges and represents that each Party will be entering into this Assignment freely, knowingly, and without coercion, and based on its own judgment.

Except as otherwise set forth herein, each Party shall bear its own costs and expenses in performing this Assignment. If any provision of this Assignment is held by a court of competent jurisdiction to be contrary to law or public policy the remaining provisions shall remain in full force and effect. No term or provision hereof shall be deemed waived and no breach consented to or excused, unless such waiver, consent or excuse shall be in writing and signed by the Party claimed to have waived or consented. Should either Party consent, waive, or excuse a breach by the other Party, such shall not constitute consent to, waiver of, or excuse of any other different or subsequent breach whether or not of the same kind as the original breach.

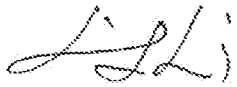
This Assignment is the entire understanding and agreement between the Parties hereto with respect to the subject matter of this Assignment and merges and supersedes all prior communications, understanding and agreements, written or oral, and no amendments shall become effective without written agreement signed by the Parties hereto.

Each signatory below represents and warrants that it is duly authorized to sign, execute, and deliver this Assignment on behalf of the Party it represents:

DONGGUAN CHANGGONG MICROELECTRONICS LTD.
(ASSIGNOR)

Name: XUENING LI

Title:

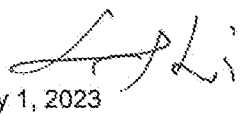
Signature: 

Date: January 1, 2023

INNOVISION SEMICONDUCTOR INC.
(ASSIGNEE)

Name: XUENING LI

Title:

Signature: 

Date: January 1, 2023

EXHIBIT A

INVENTION DESCRIPTION

In general, this disclosure describes an embodiment of an invented synchronous clock generator circuit for multiphase DC-DC converter. Assuming the phase number is N, the proposed synchronous clock generator circuit comprises a front-end buffer, a ramp signal generator, a voltage reference generator circuit, a set of comparators, a set of pulse generators, and a pulse combination circuit. The voltage buffer generates a reference voltage - VREF_B, which is identical to the input reference voltage - VREF but with enhanced driving capability. The voltage reference generator circuit is used to generate equally divided voltage reference, VREF2-VREFN, based on the configured phase number. It comprises a set of identical resistors connected in series between the VREF_B and the ground. Also, there is a pull-down N-MOSFET connected to each node between two adjacent resistors. In this way, by controlling the on/off state of each N-MOSFET, the circuit can generate reference voltage, VREF2-VREFN, that meets the requirement of configured phase number. The ramp signal generator circuit consists of a constant current source, a capacitor, and an N-MOSFET. The constant current source keeps charging the capacitor to generate the ramp-up voltage signal – VRAMP, which is compared to the reference voltage, VREF_B. The output of the comparator is then fed into a 10-nano-second (ns) pulse generator. This 10-ns pulse generator generates a 10-ns width pulse whenever it detects a rising edge from the comparator's output. The output of the pulse generator, CLK_PULSE1, drives the N-MOSFET that is used for resetting the capacitor. In this way, VRAMP becomes a saw-tooth waveform, which ramps between 0V to VREF_B, and the CLK_PULSE1 signal's frequency is the same as the saw-tooth waveform frequency, which is defined as the synchronous loop frequency. Similarly, for the other voltage references VREF2-VREFN, there is a comparator that compares each voltage reference with the VRAMP signal. The outputs of these comparators are connected to 30-ns pulse generators, which generate the clock pulse signals: CLK_PULSE2-CLK_PULSEN, respectively. These clock pulse signals along with the original CLK_PULSE1 signal are all at the same frequency but equally interleaved over one period. Finally, these clock pulse signals are combined into the required synchronous clock signal, SYNC, by a set of "OR" gate circuits. Therefore, the 10-ns pulse can be identified as the master clock pulse, and the 30-ns pulse can be identified as the slave clock pulse. Also, the pulse frequency of the signal SYNC is N times of CLK_PULSE1's frequency. There are two extraordinary features for the proposed synchronous clock generator circuit. First, the synchronous loop frequency is not dependent on the configured number of phases. Therefore, the synchronous clock generator can maintain very stable synchronous loop frequency and equally interleaved phase shift even when the number of phases changes dynamically, which greatly improves the stability of the multiphase DC-DC converter. Second, the master clock signal and the slave clock signal are distinguished by their different pulse width. No additional signal is needed to identify the master clock so that the total number of pins are reduced, and the circuit layout is simplified.