PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT7854308

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
RENESAS DESIGN US INC. (FORMERLY KNOWN AS DIALOG SEMICONDUCTOR US INC. AS SUCCESSOR-IN-INTEREST TO ADESTO TECHNOLOGIES CORPORATION AND ARTEMIS ACQUISITION, LLC)	02/03/2023

RECEIVING PARTY DATA

Name:	GLOBALFOUNDRIES U.S. INC.
Street Address:	400 STONEBREAK ROAD EXTENSION
City:	MALTA
State/Country:	NEW YORK
Postal Code:	12020

PROPERTY NUMBERS Total: 95

Property Type	Number
Patent Number:	8062694
Patent Number:	7215568
Patent Number:	7561460
Patent Number:	7746683
Patent Number:	7372716
Patent Number:	7483294
Patent Number:	8531863
Patent Number:	7277312
Patent Number:	7327603
Patent Number:	7715226
Patent Number:	8115282
Patent Number:	8420481
Patent Number:	8107273
Patent Number:	8369132
Patent Number:	8625331
Patent Number:	8274842
Patent Number:	8498164
Patent Number:	8331128
Patent Number:	9007814

PATENT

REEL: 063118 FRAME: 0352

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Property Type	Number
Patent Number:	9373398
Patent Number:	8675396
Patent Number:	8426839
Patent Number:	8437171
Patent Number:	8947907
Patent Number:	8294488
Patent Number:	9159414
Patent Number:	8320148
Patent Number:	8659926
Patent Number:	8829482
Patent Number:	9401472
Patent Number:	8687403
Patent Number:	9343667
Patent Number:	10446747
Patent Number:	9755142
Patent Number:	8947913
Patent Number:	9177639
Patent Number:	9099175
Patent Number:	9721658
Patent Number:	9570166
Patent Number:	8854873
Patent Number:	8895953
Patent Number:	9070877
Patent Number:	8816314
Patent Number:	8847192
Patent Number:	9047948
Patent Number:	8659954
Patent Number:	8995173
Patent Number:	9165648
Patent Number:	9025396
Patent Number:	9305643
Patent Number:	9099633
Patent Number:	8952351
Patent Number:	8730752
Patent Number:	9368198
Patent Number:	8941089
Patent Number:	9165644
Patent Number:	9734902

Property Type	Number
Patent Number:	9053789
Patent Number:	9147464
Patent Number:	9455036
Patent Number:	8912517
Patent Number:	9627441
Patent Number:	8866122
Patent Number:	9007808
Patent Number:	8953362
Patent Number:	9431101
Patent Number:	9373786
Patent Number:	8995167
Patent Number:	9019745
Patent Number:	9208876
Patent Number:	9412945
Patent Number:	9595671
Patent Number:	9252359
Patent Number:	9818939
Patent Number:	9711719
Patent Number:	9361975
Patent Number:	9336868
Patent Number:	9368206
Patent Number:	9099176
Patent Number:	9391270
Patent Number:	10497868
Patent Number:	9613693
Patent Number:	9530495
Patent Number:	9524777
Patent Number:	10191666
Patent Number:	11056646
Patent Number:	10181496
Patent Number:	10777268
Patent Number:	10984861
Patent Number:	11107535
Application Number:	15650719
Application Number:	17510545
Application Number:	17879904
Application Number:	17601778
Patent Number:	11537754

CORRESPONDENCE DATA

Fax Number: (703)848-2981

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent

using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: aparedes@rcsc-ip.com

Correspondent Name: ANDREW M. CALDERON

Address Line 1: 7918 JONES BRANCH DRIVE, SUITE 500

Address Line 4: MCLEAN, VIRGINIA 22102

NAME OF SUBMITTER:	ANDREW M. CALDERON
SIGNATURE:	/Andrew M. Calderon/
DATE SIGNED:	03/20/2023

Total Attachments: 7

source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page1.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page2.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page3.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page4.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page5.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page6.tif source=685059550_v 1_Project Cyndi - Patent Assignment Agreement (Executed)#page7.tif

PATENT ASSIGNMENT AGREEMENT

This PATENT ASSIGNMENT AGREEMENT ("<u>Patent Assignment</u>"), dated as of February 3, 2023, is entered into by: Renesas Design US Inc. (formerly known as Dialog Semiconductor US Inc. as successor-in-interest to Adesto Technologies Corporation and Artemis Acquisition, LLC), a Delaware corporation ("<u>Assignor</u>"), in favor of GlobalFoundries U.S. Inc., a Delaware corporation ("Assignee").

WHEREAS, pursuant to that certain Asset Purchase Agreement, dated as of January 27, 2023, by and between Assignor and Assignee, Assignor wishes to sell and assign to Assignee, among other assets, certain Assigned Patents of Assignor as defined and detailed below, and has agreed to execute and deliver this Patent Assignment;

NOW, THEREFORE, in consideration of the premises and the mutual covenants and agreements contained herein, and for other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the parties hereto, intending to be legally bound, hereby agree as follows:

- 1. <u>Assignment</u>. Assignor hereby irrevocably sells, conveys, transfers and assigns to Assignee, and Assignee hereby accepts, all of Assignor's right, title and interest in and to the following:
- (a) the issued patents and patent applications set forth on <u>Schedule A</u> hereto and all related patent applications in all countries, including all issuances, divisions, continuations, continuations-in-part, reissues, extensions, reexaminations and renewals thereof, together with all patents issuing therefrom (the "Assigned <u>Patents</u>");
- (b) including specifically, but without limitation, any registrations and applications therefor, any renewals and extensions of the registrations, all rights of priority of Assignor accruing under any of the foregoing provided by applicable law of any jurisdiction, by international treaties and conventions and otherwise throughout the world, now or hereafter in effect, for Assignee's own use and enjoyment, and for the use and enjoyment of Assignee's successors, assigns or other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor if this Patent Assignment had not been made;
- (c) any and all royalties, income, fees, income, payments and other proceeds now or hereafter due or payable with respect to any and all of the foregoing, including, without limitation, all claims for damages by reason of past, present or future infringement or other unauthorized use of the Assigned Patents, with the right to sue for and collect the same for Assignee's own use and enjoyment and for the use and enjoyment of its successors, assigns or other legal representatives; and
- (d) any and all claims and causes of action, with respect to any of the foregoing, whether accruing before, on and/or after the date hereof, including all rights to and claims

for damages, restitution and injunctive and other legal and equitable relief for past, present and future infringement, dilution, misappropriation, violation, misuse, breach or default, with the right but no obligation to sue for such legal and equitable relief and to collect, or otherwise recover, any such damages.

- 2. Recordation and Further Actions. Assignor hereby authorizes the Commissioner for Patents and any other governmental officials of any country, to record and register this Patent Assignment upon request by Assignee, it successors, assigns and legal representatives, or to such nominees as it may designate. Assignor shall take such steps and actions following the date hereof, and provide to Assignee, Assignee's successors, assigns or other legal representatives, reasonable cooperation and assistance, requested by Assignee and at Assignee's sole expense, including the execution of any documents, files, registrations, or other similar items, to more fully and effectively effectuate the purposes of this Patent Assignment and evidence and perfect Assignee's exclusive ownership of the Assigned Patents and to ensure that the Assigned Patents are properly assigned to Assignee, or any assignee or successor thereto.
- 3. <u>Counterparts</u>. This Patent Assignment may be executed in counterparts, each of which shall be deemed an original, but all of which together shall be deemed to be one and the same agreement. A signed copy of this Patent Assignment delivered by facsimile, email or other means of electronic transmission shall be deemed to have the same legal effect as delivery of an original signed copy of this Patent Assignment.
- 4. <u>Successors and Assigns</u>. This Patent Assignment shall be binding upon and shall inure to the benefit of the parties hereto and their respective successors and assigns. This Patent Assignment may not be modified or amended except by an instrument or instruments in writing signed by Assignor and Assignee.
- 5. <u>Governing Law</u>. This Patent Assignment and any claim, controversy, dispute or cause of action (whether in contract, tort or otherwise) based upon, arising out of or relating to this Patent Assignment and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of Delaware, without giving effect to any choice or conflict of law provision or rule (whether of the State of Delaware or any other jurisdiction).

IN WITNESS WHEREOF, the parties have duly executed and delivered this Patent Assignment as of the date first above written.

By:

ASSIGNOR:

RENESAS DESIGN US INC. (formerly known as Dialog Semiconductor US Inc. as successor-in-interest to Adesto Technologies Corporation and Artemis Acquisition, LLC)

DocuSigned by:

Vavin lu

Name: Davin Lee

	Title:	Director and Vice President
Agreed and accepted by:		
ASSIGNEE:		
GLOBALFOUNDRIES U.S. INC.		
By:		
Name:		
Title:		

[Signature Page to Patent Assignment Agreement]

IN WITNESS WHEREOF, the parties have duly executed and delivered this Patent Assignment as of the date first above written.

A	SS	IG	N	O	R:
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RENESAS DESIGN US INC. (formerly known as Dialog Semiconductor US Inc. as successor-in-interest to Adesto Technologies Corporation and Artemis Acquisition, LLC)

By:			
Name:			
Title:			

Agreed and accepted by:

ASSIGNEE:

GLOBALFOUNDRIES U.S. INC.

By: ______

Name: Kevin J. Soukup
Title: Chief Strategy Officer

SCHEDULE A

ASSIGNED PATENTS

Devices, systems, and methods for memory-based vitor-matrix multiplication	STATIC RANDOM ACCESS MEMORIES WITH PROGRAMMABLE IMPEDIANCE ELEMBNTS AND METHODS AND DEVICES INCLUDING THE SAME Provide dividually inclonable frontions IPI FRI made from RRAM arrays.	MEMORY DEVICE HAVING PROGRAMMABLE IMPEDANCE ELEMENTS WITH A COMMON CONDUCTOR FORMED BELOW BIT LINES PROGRAMMABLE IMPEDANCE MEMORY DEVICE AND RELATED METHODS	Write parameter switching in a memory device Memory Device Having Programmable Impedance Elements With A Common Conductor Formed Bellow Bit Lines	NEDS I I'VE SWI ICHINIA MEMILIAN TAYMINA A NEDSI IAN, JAJUCE, AND SMITICH MEMILIAN LELL. Dual program state cycling algorithms for resistive switching memory device	Resistive switching memory having a resistor, diode, and switch memory cell	Memory elements having conductive cap layers and methods therefor METHODS FOR SETTING A RESISTANCE DEPROGRAMMARI ERESISTANCE MEMORY CELLS AND DEVICES INCLUDING THE SAME	MEMORY CELLS WITH VERTICALLY INTEGRATED TUNNEL ACCESS DEVICE AND PROGRAMMABLE INFEDANCE ELEMENT Memory elements having conductive cap layers and methods therefor	Resistive switching memory with diode select	Common plate switching reduction in resistive switching mental reviews	Sensing B as an resistive workning internary devices Sensing B as an resistive workning internary devices	NONVOLATILE MEMORY ELEMENTS HAVING CONDUCTIVE STRUCTURES WITH SEMINAETALS AND/OR SEMICONDUCTORS	NONVOLATILE MERIORY ELEMENTS HAVING CONDUCTIVE STRUCTURES WITH SEMIMIETALS AND/OR SEMICONDUCTORS	Nonvolatile memory with seminetal or semicon ductors el ectrodes	NORVOLATILE MEMORY ELEMENTS HAVING CONDUCTIVE STRUCTURES WITH AUGUST LIBERT STRUCTURES WITH A STRUCTURES WITH A STRUCTURE OF THE MEMORY ELEMENTS HAVING CONDUCTIVES STRUCTURES WITH A STRUCTURE SWIMINE FLAX, SOND/ORS SMINOCONDUCTIVES SWIMINE FLAX, SOND SWIMINE FLAX, SOND SWIMINE FLAX, SWIMIN	Resistive Switching Devices Having a Switching Layer and An Intermediate Electrode Layer and Matchods of Formation Thereof Positive Court Files Devices Having a Switching Layer and An Intermediate Electrode Layer and Matchods of Formation Thereof	restour e smoothing, between thomas a smoothing above in the interface between between the processor of common interface. Resistive dwitching (buyer shortfring (buyer) And An Intermediate (Bettrobe) tayer and Methods of Formation Thereof	Resistive Switching Devices Having a switching Layer And An Intermediate Electrode Layer and Methods of Formation Thereof	Resistive switching Devices Having a Switching Layer And An Intermediate electroic layer and Methods of Formation Thereof	Scorage elements, structures and methods having edgeless features for programmable layer(s) Scorage elements, structures and methods having edgeless features for programmable layer(s) METHODYS OF PARRICATIONS STRUCKURES FEATURES FEATURES FEATURES FEATURES FEATURES FOR PROGRAMMANI E LAYER(s)	Verify pulse delay to improve resistance window	Verify pulsy did and rose typing agrantims Verify pulsy did art or improvementations windows Verify pulsy did art or improvementations windows	Two Terminal Resistive Access Devices and Methods of Formation Thereof	Resistive Devices and when holds of Operation There or Resistive Devices and Methods of Operation There or	SAFEGUARDING DATA THROUGH AN SMIT PROCESS Boutston Distance of Machinel of Discontine Theoret	Resistive Switching Devices Having A Buffer Layer and Methods of Formation Thereof	RESISTIVE SWITCHING MEMORY RESISTIVE SWITCHING MEMORY	Resistive Switching Memory	Resistive Switching Memory	SYSTEM ARCHITECTURE WITH MULTIPLE MEMORY TYPES, INCLUDING PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS SYSTEM ARCHITECTURER WITH DATA TRANSFER PATHS RETWEEN DIFFERENT MEMORY TYPES	Triggered cell annihi lation for resistive switching memory devices	Resistive Devices and Methods of Operation Thereof	Resistive Devices and Methods of Operation Thereof	THE STATE OF THE S	Resistive Devices and Methods of Operation Thereof	Resistive Devices and Methods of Operation Thereof	Resistive switching devices and methods of formation thereof	ORCLITS AND METHODS FOR PLACING PROGRAMMABLE INDEDANCING MEMORY KELDKEN'S IN HIGH INDEDANCE STATES ORCLIT'S AND METHODS FOR PLACING PROGRAMMABLE INDEDANCING MEMORY KELDKEN'S IN HIGH INDEDANCE STATES ORCLIT'S AND METHODS FOR PLACING PROGRAMMABLE INDEDANCING MEMORY KELDKEN'S IN HIGH INDEDANCE STATES	PROGRAMMABLE INVESTMENT BLANKING WITH LATERAL WITH A STRUCK STRUCTURE STRUCTURE.	MEMORY DEVICES AND METHODS HAVING ADAPTABLE READ THRESHOLD LEVELS SOILD IF ETERRA YTE MERHODS YE INFARTON WITH ITERROR IN THRESHOLD LEVELS TO INFORM THE WORLD FOR THE THRESHOLD WITH THRESHOLD LEVELS AND THE SHOULD LEVELS.	Pre-conditioning circuits and methods for programmable impedance elements in memory devices	WINDOWY CELLS, DEVILES AND METHOD WITH DYNAMIC STORAGE LEMMENTS AND PROGRAMMABLE IMPEDANCE SHADOW ELEMENTS RESISTING METHODS STORAGE REGISTER OF THE STORAGE STORAGE STATES AND METHODS LAWLING READ CHREEN IT IMPI TING RESISTING METHODS CHARLING READ CHREEN IT IMPI TING RESISTING METHOD READ CHREEN THE PROGRAMME STATE OF THE PROGRAMME STATE O	CBRAM/ReRAM WITH IMPROVED PROGRAM AND ERASE ALGORITHMS	PROGRAMMABLE WINDOW OF DEPENTING TO GRAMI	CONTACT STRUCTURE AND INCTION FOR VARIABLE INVESTIGATION ACCURATE TO THE REPORT OF STRUCTURE AND INCTION FOR VARIABLE INVESTIGATION ACCURATIONS TO EXPONENTIAL THEORY OF STRUCTURE AND INCTION OF THE STRUCTURE AND INCIDENCE AND IN	MEMIORY ELEMENTS AND METHODS WITH IMPROVED DATA RETENTION AND/OR ENDURANCE	WINDOWS CASE, ANCHI ELI ONGE MAND HET DOUG FOR WINDOWS ELEMENTS OF PRIVING A PRIMING CHANGE IN PRACES IT PROFESSION FOR PROGRAMMABLE MEMBROSY ELEMENTS, DEVICES AND METHODS HAVING PHYSICALLY LOCALIZED STRUCTURE.	READ DPERATIONS AND CIRCUIT'S RISK MIENDRY DEVICES HAVING PROGRAMMABLE ELEMBRITS, INCLUDING PROGRAMMABLE RESISTANCE ELEMBRITS IN THE PROPERTY AND CIRCUIT'S RISK MIENDRY DEVICES ARE AND ARTERIOR FOR MISSINGER PROPERTY AND ARTERIOR OF THE PROPERTY AR	NEMORY DEVICES AND METHODS FOR STORING SINGLE DATA VALUE IN MULTIPLE PROGRAMMABLE RESISTANCE ELEMBNTS	NEMORY DEVICES AND MRCHAUS FRANKE AND AND MRITE OPERATIONS TO MEMORY ELEMENTS HAVING DYNAMIC CHANGE IN PROPERTY	ORCUITS AND METHODS HAVING PROGRAMMARLE IMPEDANCE ELEMENTS MELADRY CRUTCE AND METHODS HAVING DATA VALUE OF ACCUMINATION CHARGE IN MATERIAL DROPESTY	METHODS OF MAKING INTEGRATED CIRCUIT DEVICES HAVING VOLATILE AND NONVOKATILE MEMBER VIX TIDNS METHODS OF MAKING MEMORY DEVICES WITH PROGRAMMABLE IMPEDANCE ELEMENTS AND VERTICALLY FORMED ACCESS DEVICES	CIRCUITS HAVING PROGRAMMABLE IMPEDIANCE ELEMENTS AND VERTICAL ACCESS DEVICES	PROJECT TO ANALOGO DE LEGISTA LEGISTA ANALOGO DE LEGISTA DE L'ANALOGO	PROPRIENTS INTERPRETATIONS DECIDING ALL DE PROPRIENTS AND ACTUANY AND ACTUANY AND ACTUANY AND ACCOUNT THE STREET	VARIABLE IMPEDANCE MEMORY DEVICE STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF LIFE COMMISSION FOR A STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE PROGRAMMABLE INCLUDING PROGRAMMABLE INCLUDING PROGRAMMABLE P	PMC-BASED NON-VOLATILE CAM	PROGRAMINABLE IMPEDANCE ELEMENT CIRCUITS AND METHODS	CURRENT SOURCE CROLITS AND METHODS FOR MASS WRITE AND TESTING OF PROGRAMMMABLE IMPEDANCE ELEMENTS OF OFFICE AND AND METHODS. FOR THE AND THE PROPERTY OF THE P	METHODS AND CIRCUITS FOR TEMPERATURE VARYING WRITE OPERATIONS OF PROGRAMMAMBLE IMPEDANCE ELEMENTS	INTEGRATED CIRCUIT DEVICES AND SYSTEMS HAVING PROGRAMMABLE INPEGRANCE ELEMENTS WITH DIFFERENT RESPONSE TYPES CONDUCTING BRIDGER FANDOM ACCESS MEMORY CREAMAND FEVER STRUCTURES AND FARBICATION METHODS.	PROTOTYPING INTEGRATED DIROUT DEVICES WITH PROGRAMMABLE IMPEDANCE BEINFENTS	Recordiguated memory arrays laying programm able impediance elements and corresponding methods Abburdamon or ser in Avanda I/O are one in ser on open parameter and interpolating in the parameter of the paramet	VARIABLE IMPEDANCE MIEMDRY DEVICE BIASING CIRCUITS AND METHODS	METHODS OF PROGRAMMING AND ERASING PROGRAMMABLE NETALLIZATION CELLS (PMCs) Vailable immediate a manny device bearing similary and seaso and consensoring anathod and circuits	METHODS OF PROGRAMMING AND EASING PROGRAMMAGE IN PERSENTED FAILURATION CELLS (PMCs)	Memory cell device and method of manufacture INTEGRATION PROFILES AND MEMORY DEVICES AND DESCRIPTIONS AND D	INTERPRETATION OF THE PROPERTY	Method for operating a programmable metallization cell and electrical intrutte Interament intuition of the International Control of the American Control of the Control of	Electrical circuit and a method for operating a programmable metallization cell	Wethod for operating an integrated circuit having a resistivity changing memory cell is and method integrated semiconductor memory with arrangement of norwalatile memory cell is, and method	Read, write, and erase circux for programmable memory devices	CBRAM memory cell arrangement and method for programming DBRAM memory cells	NOR and NAND memory arrangement of resistate memory elements CRAAM memory reliablements and method for provenam this CRAAM memory reliab	Resistive memory arrangement	viecuou uzi productiig, tieritory riwning a sosiu eiesci opye maketnai region Reistivo memory arrangement	Making for majorina managar in salah ang militan managari ang managari mana	Memory eyean and process for controlling a memory component to achieve different tinds of memory characteristics on one and the same memory component. United States of America. Registered. 2009-11-28. 2009-11-28.
International Pacent-PCT	United States of America	United States of America United States of America	United States of America Talwan	United States of America	United States of America	Talwan	United States of America United States of America	United States of America	United States of America	Talwan	United States of America	China	Japan	United States of America	China	Taiwan	lapan	United States of America	United States of America United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America China	Taiwan	United States of America	United States of America	United States of America	China	Korea (South)	CHILDRED CONTROL POINT IN	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America United States of America	United States of America		Links of Section of America	United States of America	United States of America United States of America	United States of America	United States of America	United States of America	United States of America United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	United States of America	Germany United States of America	United States of America	United States of America United States of America	United States of America	Germany	United States of America	United States of America	United States of America	I Inited States of America	United States of America
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