PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7996894

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
CYPRESS SEMICONDUCTOR CORPORATION	03/15/2020

RECEIVING PARTY DATA

Name:	INFINEON TECHNOLOGIES LLC
Street Address:	198 CHAMPION COURT
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	17591824

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: julie.taylor@infineon.com
Correspondent Name: INFINEON TECHNOLOGIES LLC
Address Line 1: 198 CHAMPION COURT
Address Line 4: SAN JOSE, CALIFORNIA 95134

NAME OF SUBMITTER:	KIN HUNG LAI
SIGNATURE:	/Kin Hung Lai/
DATE SIGNED:	06/08/2023

Total Attachments: 34
source=Corporateassignment#page1.tif
source=Corporateassignment#page2.tif
source=Corporateassignment#page3.tif
source=Corporateassignment#page4.tif
source=Corporateassignment#page5.tif
source=Corporateassignment#page6.tif
source=Corporateassignment#page7.tif
source=Corporateassignment#page8.tif

source=Corporateassignment#page9.tif
source=Corporateassignment#page10.tif
source=Corporateassignment#page11.tif
source=Corporateassignment#page12.tif
source=Corporateassignment#page13.tif
source=Corporateassignment#page14.tif
source=Corporateassignment#page15.tif
source=Corporateassignment#page16.tif
source=Corporateassignment#page17.tif
source=Corporateassignment#page18.tif
source=Corporateassignment#page19.tif
source=Corporateassignment#page20.tif
source=Corporateassignment#page21.tif
source=Corporateassignment#page22.tif
source=Corporateassignment#page23.tif
source=Corporateassignment#page24.tif
source=Corporateassignment#page25.tif
source=Corporateassignment#page26.tif
source=Corporateassignment#page27.tif
source=Corporateassignment#page28.tif
source=Corporateassignment#page29.tif
source=Corporateassignment#page30.tif
source=Corporateassignment#page31.tif
source=Corporateassignment#page32.tif
source=Corporateassignment#page33.tif
source=Corporateassignment#page34.tif

UNITED STATES OF AMERICA

DECLARATION OF CONSENT FOR THE PURPOSE OF RECORDATION OF ASSIGNMENT WITH THE U.S. PATENT AND TRADEMARK OFFICE

For good and valuable consideration, the receipt of which is hereby acknowledged, Cypress Semiconductor Corporation, a Delaware corporation having a place of business at 198 Champion Court, San Jose, CA 95134 ("**Assignor**"), has assigned, sold and transferred to Infineon Technologies LLC, a Delaware limited liability company having a place of business at 198 Champion Court, San Jose, CA 95134 ("**Assignee**"), on March 15, 2020 and effective March 15, 2020, all rights, title and interest that exist and may exist in the future in and to any of the following (collectively, the "***Patent Rights***"):

(a) the patent applications and patents listed in the attached Appendix I (collectively, the "***Assigned Assets***"), including all rights of priority;

(b) all patents, divisionals, continuations, continuations-in-part, continued prosecution applications, requests for continuing examinations, reissues, reexaminations and extensions thereof and all pending applications therefor, and any other patent or patent application related to such patent or patent application by claim of direct or indirect priority or terminal disclaimer, and all pending applications therefor, and any patents resulting therefrom for all Assigned Assets in (a) above;

(c) all foreign patents, foreign patent applications, and foreign counterparts relating to any item in any of the foregoing categories by claim of direct or indirect priority or terminal disclaimer (a) and (b), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(d) all items in any of the foregoing categories (a) through (c), whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(e) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (d), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(f) all claims and causes of action (whether known or unknown or whether currently pending, filed, or otherwise) for damages, injunctive relief, and any other remedies of any kind, accounting and information, and other secondary claims arising out of the past, current, and future infringement of the Assigned Assets and/or any item in any of the foregoing categories (b) through (e) by third parties which have accrued with Assignor or to which Assignor otherwise holds title; and

(g) all rights to collect royalties and other payments under or on account of any of the Assigned Assets and/or any item in any of the foregoing categories (b) through (f).

Assignor also hereby authorizes the respective patent office or governmental agency to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances which may be granted upon any of the **Assigned Assets** in the name of **Assignee**, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of **Assignee**, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist **Assignee** in obtaining, perfecting, sustaining, and/or enforcing the **Patent Rights**.

The terms and conditions of this assignment will inure to the benefit of **Assignee**, its successors, assigns, and other legal representatives and will be binding upon **Assignor**, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF, each of **Assignor** and **Assignee** has caused its duly authorized representative to execute this declaration.

ASSIGNOR Cypress Semiconductor Corporation:

March 25, 2022

Name: Terence Woodsome
Title: Assistant Secretary
Date

ASSIGNEE Infineon Technologies LLC:

14-Mar-22

Name: Marc Field
Title: Secretary
Date

Appendix 1

Filing Date	Application Number	Internal file number	Title
7/18/2011	90/011,801	1998P60111 US13	MEMORY INTERFACE SYSTEM AND METHOD FOR REDUCING CYCLE TIME OF SEQUENTIAL READ AND WRITE ACCESSES USING SEPARATE ADDRESS AND DATA BUSES
10/16/2019	16/655,091	2016P60039 US02	SYSTEMS, METHODS, AND DEVICES FOR USER CONFIGURABLE WEAR LEVELING OF NON-VOLATILE MEMORY
11/20/2020	16/953,643	2017P60059 US02	EMBEDDED NON-VOLATILE MEMORY DEVICE AND FABRICATION METHOD OF THE SAME
10/12/2020	17/068,492	2017P60068 US03	MEMORY DEVICES, SYSTEMS, AND METHODS FOR UPDATING FIRMWARE WITH SINGLE MEMORY DEVICE
3/19/2020	16/823,528	2019P60071 US01	GENERAL-PURPOSE ANALOG SWITCH WITH A CONTROLLED DIFFERENTIAL EQUALIZATION VOLTAGE-SLOPE LIMIT
6/4/2019	16/431,548	2018P60059 US01	SECURED COMMUNICATION FROM WITHIN NON-VOLATILE MEMORY DEVICE
12/14/2020	17/120,415	2018P60061 US03	NONVOLATILE MEMORY DEVICE WITH REGIONS HAVING SEPARATELY PROGRAMMABLE SECURE ACCESS FEATURES AND RELATED METHODS AND SYSTEMS
10/9/2020	17/066,599	2020P60238 US02	MEMORY DEVICE RESILIENT TO CYBER-ATTACKS AND MALFUNCTION
3/24/2020	16/827,924	2019P60080 US02	SILICON-OXIDE-NITRIDE-OXIDE-SILICON MULTI-LEVEL NON-VOLATILE MEMORY DEVICE AND METHODS OF FABRICATION THEREOF
9/4/2020	17/012,636	2014P60117 US02	BOOTING AN APPLICATION FROM MULTIPLE MEMORIES
6/26/2019	16/453,636	2014P60111 US01	TILTED IMPLANT FOR POLY RESISTORS
6/18/2020	16/905,044	2013P60097 US04	NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS
9/8/2020	17/014,261	2012P60151 US03	SPLIT GATE CHARGE TRAPPING MEMORY CELLS HAVING DIFFERENT SELECT GATE AND MEMORY GATE HEIGHTS
9/30/2020	17/039,603	2012P60156 US05	MEMORY FIRST PROCESS FLOW AND DEVICE
10/9/2018	16/154,907	2012P60143 US01	INTER-LAYER INSULATOR FOR ELECTRONIC DEVICES AND APPARATUS FOR FORMING SAME
2/20/2001	09/790,159	2001P60195 US	METHOD AND CIRCUIT FOR SETUP AND HOLD DETECT PASS-FAIL TEST MODE
4/16/2002	10/124,773	2002P60358 US	HIDING REFRESH IN 1T-SRAM ARCHITECTURE
9/20/2002	10/251,623	2002P60437 US	AUTOMATIC BACKUP AND RETRIEVAL OF DATA BETWEEN VOLATILE AND NON-VOLATILE MEMORIES

2/24/2004	10/785,599	2003P60146 US01	POWER SUPPLY DETECTING INPUT RECEIVER CIRCUIT AND METHOD
6/25/2004	10/877,932	2003P60366 US01	CONFIGURABLE DATA PATH ARCHITECTURE AND CLOCKING SCHEME
4/19/2004	10/827,785	2004P60278 US	CURRENT SOURCE ARCHITECTURE FOR MEMORY DEVICE STANDBY CURRENT REDUCTION
3/17/2004	10/803,011	1984P60002 US71	LATCH CIRCUIT AND METHOD FOR WRITING AND READING VOLATILE AND NON-VOLATILE DATA TO AND FROM THE LATCH
8/26/2004	10/927,583	2004P60362 US	MEMORY ARRAY WITH CURRENT LIMITING DEVICE FOR PREVENTING PARTICLE INDUCED LATCH-UP
6/18/2004	10/871,825	1998P60111 US10	MEMORY INTERFACE SYSTEM AND METHOD FOR REDUCING CYCLE TIME OF SEQUENTIAL READ AND WRITE ACCESSES USING SEPARATE ADDRESS AND DATA BUSES
9/23/2005	11/234,429	1984P60002 US73	ONE TIME PROGRAMMABLE LATCH AND METHOD
5/1/2006	11/415,694	2005P60191 US07	DEVICE AND METHOD FOR SENSING PROGRAMMING STATUS OF NON-VOLATILE MEMORY ELEMENTS
9/27/2005	11/237,378	2005P60562 US	SINGLE LATE-WRITE FOR STANDARD SYNCHRONOUS SRAMS
2/27/2007	11/712,069	2006P60361 US01	SELF VERIFICATION OF NON-VOLATILE MEMORY
9/10/2010	12/879,643	2009P60263 US01	SYSTEM AND METHOD TO COMPENSATE FOR PROCESS AND ENVIRONMENTAL VARIATIONS IN SEMICONDUCTOR DEVICES
2/28/2011	13/037,157	2010P60134 US01	SYSTEM AND METHOD FOR DE-LATCH OF AN INTEGRATED CIRCUIT
7/8/2011	13/179,307	2010P60157 US01	MEMORY DEVICES AND METHODS HAVING MULTIPLE ADDRESS ACCESSES IN SAME CYCLE
7/11/2011	13/180,337	2010P60156 US01	MEMORY DEVICES HAVING EMBEDDED HARDWARE ACCELERATION AND CORRESPONDING METHODS
12/29/2011	13/340,453	2011P60109 US01	DEVICE AND METHOD OF ESTABLISHING SLEEP MODE ARCHITECTURE FOR NVSRAMS
12/29/2011	13/340,439	2011P60129 US	CAPACITOR POWER SOURCE TAMPER PROTECTION AND RELIABILITY TEST
6/28/2012	13/536,661	2012P60109 US01	HIGH RELIABILITY NON-VOLATILE STATIC RANDOM ACCESS MEMORY DEVICES, METHODS AND SYSTEMS
10/13/2014	14/512,647	2012P60109 US02	HIGH RELIABILITY NON-VOLATILE STATIC RANDOM ACCESS MEMORY DEVICES, METHODS AND SYSTEMS
4/29/2012	13/459,206	2012P60106 US01	HIGH SPEED TIME INTERLEAVED SENSE AMPLIFIER CIRCUITS, METHODS AND MEMORY DEVICES INCORPORATING THE SAME

6/29/2012	13/537,877	2012P60114 US	MEMORY CONTROLLER DEVICES, SYSTEMS AND METHODS FOR TRANSLATING MEMORY REQUESTS BETWEEN FIRST AND SECOND FORMATS FOR HIGH RELIABILITY MEMORY DEVICES
12/26/2012	13/727,505	2012P60131 US01	ACCESS METHODS AND CIRCUITS FOR MEMORY DEVICES HAVING MULTIPLE BANKS
4/22/2014	14/258,950	2012P60131 US02	ACCESS METHODS AND CIRCUITS FOR MEMORY DEVICES HAVING MULTIPLE BANKS
9/25/2015	14/866,260	2012P60131 US05	ACCESS METHODS AND CIRCUITS FOR MEMORY DEVICES HAVING MULTIPLE CHANNELS AND MULTIPLE BANKS
12/17/2012	13/717,637	2012P60132 US02	MEMORY DEVICE DATA LATENCY CIRCUITS AND METHODS
3/12/2013	13/795,134	2012P60132 US03	DATA FORWARDING CIRCUITS AND METHODS FOR MEMORY DEVICES WITH WRITE LATENCY
3/12/2013	13/795,036	2013P60093 US02	NONVOLATILE MEMORY CELLS AND METHODS OF MAKING SUCH CELLS
3/24/2014	14/222,904	2013P60134 US01	METHOD OF FABRICATING A FERROELECTRIC CAPACITOR
6/21/2013	13/924,292	2013P60122 US	METHOD MINIMIZING IMPRINT THROUGH PACKAGING OF F-RAM
9/27/2013	14/040,616	2013P60137 US	FERROELECTRIC MEMORIES WITH A STRESS BUFFER
6/12/2014	14/303,014	2013P60133 US01	ELIMINATING SHORTING BETWEEN FERROELECTRIC CAPACITORS AND METAL CONTACTS DURING FERROELECTRIC RANDOM ACCESS MEMORY FABRICATION
12/17/2013	14/109,045	2013P60123 US03	METHODS OF FABRICATING AN F-RAM
3/28/2014	14/228,899	2013P60153 US05	MULTI-CHANNEL, MULTI-BANK MEMORY WITH WIDE DATA INPUT/OUTPUT
3/28/2014	14/229,765	2013P60153 US06	MULTI-CHANNEL PHYSICAL INTERFACES AND METHODS FOR STATIC RANDOM ACCESS MEMORY DEVICES
4/1/2016	15/088,557	2015P60080 US01	HYDROGEN BARRIERS IN A COPPER INTERCONNECT PROCESS
1/19/2018	15/875,594	2014P60102 US02	DAMASCENE OXYGEN BARRIER AND HYDROGEN BARRIER FOR FERROELECTRIC RANDOM-ACCESS MEMORY
8/10/2015	14/822,085	2014P60121 US01	POWER MANAGEMENT SYSTEM FOR HIGH TRAFFIC INTEGRATED CIRCUIT
10/19/2015	14/886,663	2014P60130 US01	10T NON-VOLATILE STATIC RANDOM-ACCESS MEMORY
4/13/2017	15/487,071	2014P60130 US02	10-TRANSISTOR NON-VOLATILE STATIC RANDOM-ACCESS MEMORY USING A SINGLE NON-VOLATILE MEMORY ELEMENT AND METHOD OF OPERATION THEREOF
6/12/2015	14/738,492	2015P60071 US01	METHOD OF FABRICATING AN F-RAM

12/15/2015	14/970,063	2015P60071 US02	FERROELECTRIC RANDOM-ACCESS MEMORY WITH PRE-PATTERNED OXYGEN BARRIER
9/24/2015	14/864,594	2015P60072 US01	NON-VOLATILE STATIC RAM AND METHOD OF OPERATION THEREOF
3/24/2016	15/079,462	2015P60079 US01	MULTI-BIT NON-VOLATILE RANDOM-ACCESS MEMORY CELLS
3/9/2016	15/065,410	2015P60073 US03	METHOD FOR FABRICATING FERROELECTRIC RANDOM-ACCESS MEMORY ON PRE-PATTERNED BOTTOM ELECTRODE AND OXIDATION BARRIER
11/14/2016	15/351,268	2015P60073 US04	FERROELECTRIC RANDOM-ACCESS MEMORY ON PRE-PATTERNED BOTTOM ELECTRODE AND OXIDATION BARRIER
6/10/2016	15/179,070	2016P60032 US01	HYBRID REFERENCE GENERATION FOR FERROELECTRIC RANDOM ACCESS MEMORY
9/28/2016	15/279,194	2016P60033 US01	METHODS AND DEVICES FOR REDUCING PROGRAM DISTURB IN NON-VOLATILE MEMORY CELL ARRAYS
3/28/2017	15/471,418	2016P60033 US03	NON-VOLATILE MEMORY ARRAY WITH MEMORY GATE LINE AND SOURCE LINE SCRAMBLING
4/17/2018	15/954,955	2016P60033 US04	NON-VOLATILE MEMORY ARRAY WITH MEMORY GATE LINE AND SOURCE LINE SCRAMBLING
12/20/2018	16/227,015	2016P60033 US05	NON-VOLATILE MEMORY ARRAY WITH MEMORY GATE LINE AND SOURCE LINE SCRAMBLING
4/25/2017	15/496,993	2016P60042 US01	SUPPRESSION OF PROGRAM DISTURB WITH BIT LINE AND SELECT GATE VOLTAGE REGULATION
1/23/2018	15/877,633	2016P60042 US02	SUPPRESSION OF PROGRAM DISTURB WITH BIT LINE AND SELECT GATE VOLTAGE REGULATION
2/6/2019	16/268,736	2016P60042 US03	SUPPRESSION OF PROGRAM DISTURB WITH BIT LINE AND SELECT GATE VOLTAGE REGULATION
5/6/2020	16/867,828	2016P60042 US04	SUPPRESSION OF PROGRAM DISTURB WITH BIT LINE AND SELECT GATE VOLTAGE REGULATION
12/21/2017	15/850,779	2017P60061 US01	ROW REDUNDANCY WITH DISTRIBUTED SECTORS
3/19/2018	15/925,510	2017P60062 US01	MEMORY GATE DRIVER TECHNOLOGY FOR FLASH MEMORY CELLS
9/29/2016	15/279,974	2016P60034 US01	METHODS AND DEVICES FOR READING DATA FROM NON-VOLATILE MEMORY CELLS
7/11/2017	15/647,166	2016P60034 US02	METHODS AND DEVICES FOR READING DATA FROM NON-VOLATILE MEMORY CELLS
12/22/2016	15/388,892	2016P60039 US01	SYSTEMS, METHODS, AND DEVICES FOR USER CONFIGURABLE WEAR LEVELING OF NON-VOLATILE MEMORY
3/29/2017	15/473,372	2016P60043 US01	SPLIT-GATE FLASH CELL FORMED ON RECESSED SUBSTRATE
10/12/2017	15/730,979	2016P60043 US02	SPLIT-GATE FLASH CELL FORMED ON RECESSED SUBSTRATE
9/25/2017	15/714,912	2017P60055 US01	2T1C FERRO-ELECTRIC RANDOM ACCESS

			MEMORY CELL
8/7/2018	16/056,874	2017P60055 US02	2T1C FERRO-ELECTRIC RANDOM ACCESS MEMORY CELL
12/20/2017	15/848,327	2017P60058 US01	METHOD OF FORMING HIGH-VOLTAGE TRANSISTOR WITH THIN GATE POLY
12/20/2017	15/848,439	2017P60059 US01	EMBEDDED NON-VOLATILE MEMORY DEVICE AND FABRICATION METHOD OF THE SAME
3/28/2018	15/938,840	2017P60069 US01	LOW INRUSH CIRCUIT FOR POWER UP AND DEEP POWER DOWN EXIT
8/24/2018	16/111,521	2018P60057 US01	FERROELECTRIC RANDOM ACCESS MEMORY SENSING SCHEME
2/7/2020	16/784,712	2018P60057 US02	FERROELECTRIC RANDOM ACCESS MEMORY SENSING SCHEME
12/4/2018	16/208,841	2017P60071 US01	NON-VOLATILE MEMORY DEVICE AND METHOD OF BLANK CHECK
6/11/2018	16/005,262	2017P60068 US01	MEMORY DEVICES, SYSTEMS, AND METHODS FOR UPDATING FIRMWARE WITH SINGLE MEMORY DEVICE
1/6/2020	16/735,177	2017P60068 US02	MEMORY DEVICES, SYSTEMS, AND METHODS FOR UPDATING FIRMWARE WITH SINGLE MEMORY DEVICE
3/29/2019	16/369,423	2018P60065 US01	SYSTEMS, METHODS, AND DEVICES FOR FAST WAKEUP OF DC-DC CONVERTERS INCLUDING FEEDBACK REGULATION LOOPS
3/23/2020	16/827,478	2018P60061 US02	NONVOLATILE MEMORY DEVICE WITH REGIONS HAVING SEPARATELY PROGRAMMABLE SECURE ACCESS FEATURES AND RELATED METHODS AND SYSTEMS
3/25/2020	16/829,219	2019P60079 US01	REMOTE MEMORY DIAGNOSTICS
3/25/2020	16/829,838	2020P60238 US01	MEMORY DEVICE RESILIENT TO CYBER-ATTACKS AND MALFUNCTION
3/24/2020	16/827,948	2019P60080 US01	SILICON-OXIDE-NITRIDE-OXIDE-SILICON BASED MULTI-LEVEL NON-VOLATILE MEMORY DEVICE AND METHODS OF OPERATION THEREOF
2/27/2004	10/708,379	2004P60179 US	METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE
11/29/2005	11/164,556	2005P60609 US	SRAM VOLTAGE CONTROL FOR IMPROVED OPERATIONAL MARGINS
11/19/2007	11/985,961	2007P60260 US	CIRCUIT DESIGN
12/3/2007	11/998,948	2007P60296 US	SRAM VOLTAGE CONTROL FOR IMPROVED OPERATIONAL MARGINS
4/30/2001	09/846,119	2001P60148 US	METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE
3/14/2002	10/097,674	2002P60241 US	POLY/SILICIDE STACK AND METHOD OF FORMING THE SAME
6/6/2002	10/163,970	2002P60231 US	IN SITU HARD MASK APPROACH FOR SELF-ALIGNED CONTACT ETCH

2/7/2002	10/072,164	2002P60178 US	DUAL-DAMASCENE PROCESS AND ASSOCIATED FLOATING METAL STRUCTURES
6/26/2002	10/184,336	2002P60269 US	PROTECTION OF A LOW-K DIELECTRIC IN A PASSIVATION LEVEL
9/11/2002	10/241,236	2002P60413 US	LOW-K DIELECTRIC LAYER WITH AIR GAPS
12/6/2002	10/314,381	2002P60554 US	DEUTERIUM INCORPORATED NITRIDE
9/8/2004	10/936,275	2003P60480 US01	METHOD FOR REDUCING SOFT ERROR RATES OF MEMORY CELLS
9/24/2004	10/950,332	2003P60489 US01	OXIDE-NITRIDE STACK GATE DIELECTRIC
12/20/2007	11/961,750	2003P60489 US02	OXIDE-NITRIDE STACK GATE DIELECTRIC
8/26/2004	10/927,365	2003P60474 US01	METHOD OF REDUCING STEP HEIGHT DIFFERENCE BETWEEN DOPED REGIONS OF FIELD OXIDE IN AN INTEGRATED CIRCUIT
3/25/2005	11/089,732	2004P60240 US01	INCREASING SELF-ALIGNED CONTACT AREAS IN INTEGRATED CIRCUITS USING A DISPOSABLE SPACER
6/25/2004	10/877,313	2004P60297 US	MEMORY CELL ARRAY LATCHUP PREVENTION
5/1/2009	12/434,084	2004P60297 US01	MEMORY CELL ARRAY
10/25/2011	13/280,937	2004P60297 US02	MEMORY CELL ARRAY LATCHUP PREVENTION
7/23/2013	13/949,116	2004P60297 US03	MEMORY CELL ARRAY LATCHUP PREVENTION
3/29/2014	14/229,908	2004P60297 US04	MEMORY CELL ARRAY LATCHUP PREVENTION
8/25/2006	11/509,932	1998P60274 US03	SHALLOW TRENCH ISOLATION STRUCTURES AND METHODS FOR FORMING THE SAME
11/14/2006	11/599,926	2005P60605 US01	PROCESS FOR POST CONTACT-ETCH CLEAN
2/27/2007	11/711,382	2006P60364 US01	INTERFACE APPARATUS AND METHODS OF TESTING INTEGRATED CIRCUITS USING THE SAME
5/15/2007	11/803,474	2006P60536 US01	METHOD OF FORMING BORDERLESS CONTACTS
11/2/2006	11/555,905	2006P60314 US	POLYCRYSTALLINE SILICON ACTIVATION RTA
9/24/2007	11/860,245	2006P60662 US01	SEMICONDUCTOR TOPOGRAPHY AND METHOD FOR REDUCING GATE INDUCED DRAIN LEAKAGE (GIDL) IN MOS TRANSISTORS
3/28/2008	12/079,802	2008P60309 US	NON-VOLATILE MEMORY AND METHOD OF OPERATING THE SAME
9/23/2010	12/888,737	2009P60265 US02	NVSRAM WITH INVERTED RECALL
6/18/2013	13/921,056	2009P60265 US03	NVSRAM WITH INVERTED RECALL
4/1/2002	10/114,535	2002P60328 US	FERROELECTRIC MEMORY WITH BIT-PLATE PARALLEL ARCHITECTURE AND OPERATING METHOD THEREOF
3/31/2003	10/404,941	2003P60177 US	BIT-LINE SHIELDING METHOD FOR FERROELECTRIC MEMORIES
11/21/2003	10/719,108	2003P60522 US	IMPRINT-FREE CODING FOR FERROELECTRIC NONVOLATILE COUNTERS
12/14/2006	11/611,053	2003P60522 US01	IMPRINT-FREE CODING FOR FERROELECTRIC NONVOLATILE COUNTERS
11/9/2004	10/984,065	2004P60481 US	CIRCUIT FOR GENERATING A CENTERED REFERENCE VOLTAGE FOR A 1T/1C FERROELECTRIC MEMORY

6/23/2006	11/426,165	2004P60481 US01	CIRCUIT FOR GENERATING A CENTERED REFERENCE VOLTAGE FOR A 1T/1C FERROELECTRIC MEMORY
12/23/2004	11/021,394	2004P60539 US	NON-VOLATILE COUNTER
3/17/2005	11/082,526	2004P60539 US01	COUNTING SCHEME WITH AUTOMATIC POINT-OF-REFERENCE GENERATION
1/20/2012	13/355,145	2011P60082 US01	AUTHENTICATING FERROELECTRIC RANDOM ACCESS MEMORY (F-RAM) DEVICE AND METHOD
11/12/2013	14/077,971	2011P60082 US02	AUTHENTICATING FERROELECTRIC RANDOM ACCESS MEMORY (F-RAM) DEVICE AND METHOD
8/8/2012	13/569,735	2011P60099 US03	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) DEVICE STRUCTURE EMPLOYING REDUCED PROCESSING STEPS
9/13/2013	14/026,118	2011P60099 US08	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) DEVICE STRUCTURE EMPLOYING REDUCED PROCESSING STEPS
8/8/2012	13/569,755	2011P60099 US04	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) WITH SIMULTANEOUS FORMATION OF SIDEWALL FERROELECTRIC CAPACITORS
8/26/2013	14/010,134	2011P60099 US06	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) WITH SIMULTANEOUS FORMATION OF SIDEWALL FERROELECTRIC CAPACITORS
8/8/2012	13/569,785	2011P60099 US05	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) HAVING A FERROELECTRIC CAPACITOR ALIGNED WITH A THREE DIMENSIONAL TRANSISTOR STRUCTURE
8/26/2013	14/010,174	2011P60099 US07	METHOD FOR FABRICATING A DAMASCENE SELF-ALIGNED FERRORELECTRIC RANDOM ACCESS MEMORY (F-RAM) HAVING A FERROELECTRIC CAPACITOR ALIGNED WITH A THREE DIMENSIONAL TRANSISTOR STRUCTURE
5/11/2012	13/470,117	2012P60118 US	ENHANCED HYDROGEN BARRIER ENCAPSULATION METHOD FOR THE CONTROL OF HYDROGEN INDUCED DEGRADATION OF FERROELECTRIC CAPACITORS IN AN F-RAM PROCESS
10/14/2014	14/514,008	2012P60118 US01	ENHANCED HYDROGEN BARRIER ENCAPSULATION METHOD FOR THE CONTROL OF HYDROGEN INDUCED DEGRADATION OF FERROELECTRIC CAPACITORS IN AN F-RAM PROCESS

11/26/2012	13/685,331	2012P60145 US	METHOD FOR IMPROVING DATA RETENTION IN A 2T/2C FERROELECTRIC MEMORY
11/29/1989	07/443,018	1987P60003 US03	NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT
7/10/1989	07/377,168	1987P60003 US02	METHOD FOR READING NON-VOLATLILE FERROELECTRIC CAPACITOR MEMORY CELL
12/22/2006	11/644,819	2006P60461 US	METHOD AND APPARATUS TO PROGRAM BOTH SIDES OF A NON-VOLATILE STATIC RANDOM ACCESS MEMORY
8/24/2011	13/216,546	2006P60457 US01	METHOD AND APPARATUS TO IMPLEMENT A RESET FUNCTION IN A NON-VOLATILE STATIC RANDOM ACCESS MEMORY
12/31/2007	12/006,228	2007P60308 US01	CURRENT CONTROLLED RECALL SCHEMA
8/28/2001	09/941,370	2000P60236 US01	FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF
2/3/2003	10/356,496	2000P60378 US	NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE AND METHOD OF READING OUT DATA
6/5/2003	10/454,630	2000P60595 US	NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND DATA ERASING METHOD
3/7/2002	10/091,767	2001P60243 US01	PASSWORD AND DYNAMIC PROTECTION OF FLASH MEMORY DATA
10/22/2002	10/277,395	2001P60527 US01	SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING
2/3/2003	10/356,495	2002P60212 US	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE PROGRAMMING SECOND DYNAMIC REFERENCE CELL ACCORDING TO THRESHOLD VALUE OF FIRST DYNAMIC REFERENCE CELL
3/21/2003	10/392,912	2002P60271 US	NON-VOLATILE SEMICONDUCTOR MEMORY THAT IS BASED ON A VIRTUAL GROUND METHOD
3/27/2002	10/109,235	2002P60285 US	MEMORY WORDLINE HARD MASK
3/27/2002	10/109,516	2002P60281 US	METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION
8/1/2005	11/195,201	2002P60284 US01	SEMICONDUCTOR MEMORY WITH DATA RETENTION LINER
3/27/2002	10/109,234	2002P60277 US	LINER FOR SEMICONDUCTOR MEMORIES AND MANUFACTURING METHOD THEREFOR
4/8/2002	10/118,732	2002P60336 US	MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION
4/8/2002	10/117,818	2002P60344 US	PRECISION HIGH-K INTERGATE DIELECTRIC LAYER
4/8/2002	10/119,366	2002P60340 US	ERASE METHOD FOR A DUAL BIT MEMORY CELL
4/8/2002	10/119,273	2002P60338 US	REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING
4/8/2002	10/119,391	2002P60333 US	ALGORITHM DYNAMIC REFERENCE PROGRAMMING
3/14/2003	10/387,427	2002P60359 US	NON-VOLATILE SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME

4/19/2002	10/126,207	2002P60131 US	USING A FIRST LINER LAYER AS A SPACER IN A SEMICONDUCTOR DEVICE
4/22/2002	10/128,771	2002P60134 US	SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS
9/26/2003	10/672,093	2002P60134 US01	METHOD OF MANUFACTURING A SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS
4/29/2002	10/136,034	2002P60140 US	SYSTEM FOR CONTROL OF PRE-CHARGE LEVELS IN A MEMORY DEVICE
5/15/2002	10/150,204	2002P60169 US	SELF-ALIGNED POLYSILICON POLISH
5/15/2002	10/150,255	2002P60161 US	METHOD AND SYSTEM FOR SCALING NONVOLATILE MEMORY CELLS
7/3/2002	10/190,002	2002P60316 US	METHOD FOR SEMICONDUCTOR WAFER PLANARIZATION BY ISOLATION MATERIAL GROWTH
7/16/2002	10/197,116	2002P60330 US	SYSTEM FOR USING A DYNAMIC REFERENCE IN A DOUBLE-BIT CELL MEMORY
7/31/2002	10/210,378	2002P60346 US	SYSTEM AND METHOD FOR ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE
8/12/2002	10/217,821	2002P60374 US	SALICIDED GATE FOR VIRTUAL GROUND ARRAYS
8/1/2003	10/631,812	2002P60366 US	NONVOLATILE MEMORY HAVING A TRAP LAYER
8/14/2002	10/217,403	2002P60382 US	REFLOWABLE-DOPED HDP FILM
8/20/2002	10/223,920	2002P60388 US	MEMORY DEVICE AND METHOD OF MAKING
8/22/2002	10/226,912	2002P60391 US	PRECHARGING SCHEME FOR READING A MEMORY CELL
9/2/2003	10/652,035	2002P60410 US	MEMORY CIRCUIT WITH REDUNDANT CONFIGURATION
9/12/2002	10/243,792	2002P60415 US	METHOD AND SYSTEM TO MINIMIZE PAGE PROGRAMMING TIME FOR FLASH MEMORY DEVICES
9/12/2002	10/243,315	2002P60421 US	SYSTEM AND METHOD FOR Y-DECODING IN A FLASH MEMORY DEVICE
9/10/2003	10/658,428	2002P60418 US	SEMICONDUCTOR MEMORY ENABLING CORRECT SUBSTITUTION OF REDUNDANT CELL ARRAY
8/5/2003	10/633,535	2002P60414 US	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE INCLUDING A PLURALITY OF BLOCKS AND A SENSING CIRCUIT PROVIDED IN EACH OF THE BLOCKS FORCOMPARING DATA WITH A REFERENCE SIGNAL HAVING A LOAD IMPOSEDTHEREON
9/16/2002	10/245,146	2002P60426 US	REFERENCE CELL WITH VARIOUS LOAD CIRCUITS COMPENSATING FOR SOURCE SIDE LOADING EFFECTS IN A NON-VOLATILE MEMORY
11/12/2002	10/292,121	2002P60508 US	FABRICATION OF SHALLOW TRENCH ISOLATION STRUCTURES WITH ROUNDED CORNER AND SELF-ALIGNED GATE

5/12/2004	10/844,116	2002P60519 US01	CASCODE AMPLIFIER CIRCUIT FOR GENERATING AND MAINTAINING A FAST, STABLE AND ACCURATE BIT LINE VOLTAGE
11/22/2002	10/302,672	2002P60519 US	CASCODE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BIT LINE VOLTAGE
11/26/2002	10/305,700	2002P60521 US	METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY
11/26/2002	10/305,750	2002P60528 US	METHOD OF PROTECTING A MEMORY ARRAY FROM CHARGE DAMAGE DURING FABRICATION
11/27/2002	10/306,529	2002P60530 US	METHOD FOR FABRICATING NITRIDE MEMORY CELLS USING A FLOATING GATE FABRICATION PROCESS
11/27/2002	10/306,252	2002P60531 US	METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE
11/29/2002	10/307,189	2002P60535 US	MEMORY WITH IMPROVED CHARGE-TRAPPING DIELECTRIC LAYER
12/2/2002	10/307,667	2002P60536 US	SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL
12/5/2002	10/313,454	2002P60545 US	STRUCTURE AND METHOD FOR REDUCING CHARGE LOSS IN A MEMORY CELL
12/5/2002	10/313,444	2002P60546 US	CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS
12/9/2002	10/315,458	2002P60558 US	DISCONTINUOUS NITRIDE STRUCTURE FOR NON-VOLATILE TRANSISTORS
1/14/2003	10/342,585	2003P60148 US	FLASH MEMORY CELL PROGRAMMING METHOD AND SYSTEM
1/15/2003	10/342,549	2003P60154 US	DIELECTRIC MEMORY CELL STRUCTURE WITH COUNTER DOPED CHANNEL REGION
1/29/2003	10/353,558	2003P60178 US	METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY
2/2/2004	10/768,188	2003P60191 US	SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF
10/12/2005	11/247,328	2003P60191 US01	SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF
2/4/2003	10/358,498	2003P60193 US	COMPENSATED OSCILLATOR CIRCUIT FOR CHARGE PUMPS
2/5/2003	10/358,866	2003P60221 US	PERFORMANCE IN FLASH MEMORY DEVICES
2/10/2003	10/361,378	2003P60233 US	SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS
3/5/2003	10/382,726	2003P60349 US	CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION
3/5/2003	10/379,885	2003P60347 US	METHOD OF PROGRAMMING A MEMORY CELL
3/5/2003	10/379,744	2003P60351 US	FAST BANDGAP REFERENCE CIRCUIT FOR USE IN A LOW POWER SUPPLY A/D BOOSTER

3/5/2003	10/382,744	2003P60353 US	METHOD OF FORMING CORE AND PERIPHERY GATES INCLUDING TWO CRITICAL MASKING STEPS TO FORM A HARD MASK IN A CORE REGION THAT INCLUDES A CRITICAL DIMENSION LESS THAN ACHIEVABLE AT A RESOLUTION LIMIT OF LITHOGRAPHY
6/16/2004	10/869,774	2003P60353 US01	SEMICONDUCTOR DEVICE WITH CORE AND PERIPHERY REGIONS
3/5/2003	10/382,731	2003P60343 US	MEMORY ARRAY HAVING SHALLOW BIT LINE WITH SILICIDE CONTACT PORTION AND METHOD OF FORMATION
3/11/2003	10/387,064	2003P60371 US	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE
3/21/2003	10/394,565	2003P60390 US	ALIGNMENT SYSTEM FOR PLANAR CHARGE TRAPPING DIELECTRIC MEMORY CELL LITHOGRAPHY
4/3/2003	10/406,415	2003P60183 US	FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER
4/15/2003	10/413,800	2003P60195 US	METHOD OF PROGRAMMING DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL
4/24/2003	10/422,092	2003P60228 US	METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED END-OF-LIFE READ MARGIN
4/24/2003	10/422,090	2003P60232 US	METHOD OF CONTROLLING PROGRAM THRESHOLD VOLTAGE DISTRIBUTION OF A DUAL CELL MEMORY DEVICE
5/3/2003	10/429,140	2003P60243 US	STRUCTURE AND METHOD FOR A TWO-BIT MEMORY CELL
5/3/2003	10/429,150	2003P60245 US	METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE
5/6/2003	10/431,320	2003P60257 US	NON-VOLATILE MEMORY READ CIRCUIT WITH END OF LIFE SIMULATION
5/6/2003	10/431,065	2003P60259 US	METHOD TO OBTAIN TEMPERATURE INDEPENDENT PROGRAM THRESHOLD VOLTAGE DISTRIBUTION USING TEMPERATURE DEPENDENT VOLTAGE REFERENCE
5/6/2003	10/431,321	2003P60251 US	A METHOD FOR MANUFACTURING A DOUBLE BITLINE IMPLANT
6/6/2003	10/455,310	2003P60305 US	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE
6/20/2003	10/600,065	2003P60342 US	MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME
1/22/2008	12/017,693	2003P60342 US01	MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME

6/27/2003	10/609,159	2003P60350 US	APPARATUS AND METHOD FOR A METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SOURCE SIDE PUNCH-THROUGH PROTECTION IMPLANT
8/12/2013	13/964,958	2003P60350 US01	APPARATUS AND METHOD FOR A METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SOURCE SIDE PUNCH-THROUGH PROTECTION IMPLANT
7/11/2003	10/617,450	2003P60420 US	UNDOPED OXIDE LINER/BPSG FOR IMPROVED DATA RETENTION
6/16/2005	11/154,070	2003P60430 US01	DUAL-LEVEL STACKED FLASH MEMORY CELL WITH A MOSFET STORAGE TRANSISTOR
8/6/2003	10/636,337	2003P60433 US	LOW POWER CHARGE PUMP
8/6/2003	10/636,336	2003P60432 US	STRUCTURE AND METHOD TO REDUCE DRAIN INDUCED BARRIER LOWERING
8/6/2003	10/635,089	2003P60434 US	MEMORY DEVICE AND METHOD OF SIMULTANEOUS FABRICATION OF CORE AND PERIPHERY OF SAME
8/6/2003	10/635,781	2003P60431 US	MEMORY DEVICE HAVING SILICIDED BITLINES AND METHOD OF FORMING THE SAME
8/7/2003	10/635,974	2003P60435 US	MEMORY CIRCUIT FOR PROVIDING WORD LINE REDUNDANCY IN A MEMORY SECTOR
9/3/2003	10/654,739	2003P60450 US	PATTERNING FOR ELONGATED VSS CONTACT ON FLASH MEMORY
10/19/2004	10/968,713	2003P60450 US01	PATTERNING FOR ELONGATED VSS CONTACT FLASH MEMORY
10/1/2003	10/677,073	2003P60495 US	MEMORY DEVICE AND METHOD
10/1/2003	10/677,031	2003P60494 US	MEMORY DEVICE AND METHOD
10/2/2003	10/677,790	2003P60498 US	MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL
10/3/2003	10/678,446	2003P60499 US	EFFICIENT AND ACCURATE SENSING CIRCUIT AND TECHNIQUE FOR LOW VOLTAGE FLASH MEMORY DEVICES
11/5/2003	10/701,780	2003P60515 US	METHOD AND STRUCTURE FOR PROTECTING NROM DEVICES FROM INDUCED CHARGE DAMAGE DURING DEVICE FABRICATION
3/7/2006	11/368,678	2002P60552 US01	SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THE SAME
11/24/2003	10/721,643	2003P60523 US	READING FLASH MEMORY
12/5/2003	10/729,732	2003P60531 US	HARD MASK SPACER FOR SUBLITHOGRAPHIC BITLINE
12/9/2003	10/731,659	2003P60534 US	PROCESS FOR FABRICATION OF NITRIDE LAYER WITH REDUCED HYDROGEN CONTENT IN ONO STRUCTURE IN SEMICONDUCTOR DEVICE
12/16/2003	10/738,301	2003P60537 US	METHOD AND DEVICE FOR PROGRAMMING CELLS IN A MEMORY ARRAY IN A NARROW DISTRIBUTION

3/13/2003	10/387,617	2003P60378 US	CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS
1/14/2004	10/758,173	2004P60117 US	ELECTROSTATIC DISCHARGE PERFORMANCE OF A SILICON STRUCTURE AND EFFICIENT USE OF AREA WITH ELECTROSTATIC DISCHARGE PROTECTIVE DEVICE UNDER THE PAD APPROACH AND ADJUSTMENT OF VIA CONFIGURATION THERETO TO CONTROL DRAIN JUNCTION RESISTANCE
1/16/2004	10/759,855	2004P60122 US	FLEXIBLE CASCODE AMPLIFIER CIRCUIT WITH HIGH GAIN FOR FLASH MEMORY CELLS
1/20/2004	10/762,071	2004P60128 US	METHOD FOR ERASING A MEMORY SECTOR IN VIRTUAL GROUND ARCHITECTURE WITH REDUCED LEAKAGE CURRENT
1/22/2004	10/762,445	2004P60132 US	STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL
2/2/2004	10/770,260	2004P60139 US	FLASH MEMORY CELL WITH UV PROTECTIVE LAYER
2/2/2004	10/770,673	2004P60142 US	BITLINE HARD MASK SPACER FLOW FOR MEMORY CELL SCALING
2/2/2004	10/770,245	2004P60141 US	DISPOSABLE HARD MASK FOR MEMORY BITLINE SCALING
2/18/2005	11/061,119	2004P60161 US	CURRENT-VOLTAGE CONVERTER CIRCUIT AND ITS CONTROL METHOD
2/18/2005	11/061,365	2004P60171 US	SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANT METHOD
2/18/2005	11/061,307	2004P60163 US	SEMICONDUCTOR MEMORY STORAGE DEVICE AND A REDUNDANCY CONTROL METHOD THEREFOR
3/25/2005	11/090,716	2004P60224 US	SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATA INTO THE SEMICONDUCTOR DEVICE
4/8/2004	10/821,312	2004P60260 US	NARROW WIDE SPACER
4/13/2004	10/823,970	2004P60269 US	SEMICONDUCTOR DEVICE HAVING A PAD METAL LAYER AND A LOWER METAL LAYER THAT ARE ELECTRICALLY COUPLED, WHEREAS APERTURES ARE FORMED IN THE LOWER METAL LAYER BELOW A CENTER AREA OF THE PAD METAL LAYER
4/28/2004	10/835,341	2004P60104 US	METHOD FOR PROVIDING SHORT CHANNEL EFFECT CONTROL USING A SILICIDE VSS LINE
5/4/2004	10/838,962	2004P60110 US	METHOD FOR MINIMIZING FALSE DETECTION OF STATES IN FLASH MEMORY DEVICES
5/4/2004	10/839,562	2004P60107 US	POSITIVE GATE STRESS DURING ERASE TO IMPROVE RETENTION IN MULTI-LEVEL, NON-VOLATILE FLASH MEMORY
5/4/2004	10/839,561	2004P60109 US	METHOD AND APPARATUS FOR ELIMINATING WORD LINE BENDING BY SOURCE SIDE IMPLANTATION

5/5/2004	10/839,614	2004P60114 US	METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES
5/11/2005	11/126,739	2005P60207 US	CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
5/11/2004	10/843,289	2004P60123 US	BITLINE IMPLANT UTILIZING DUAL POLY
6/3/2004	10/860,450	2004P60217 US	METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES
1/27/2006	11/340,916	2004P60217 US01	METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES
6/4/2004	10/861,581	2004P60221 US	APPARATUS AND METHOD FOR SOURCE SIDE IMPLANTATION AFTER SPACER FORMATION TO REDUCE SHORT CHANNEL EFFECTS IN METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS
6/4/2004	10/861,575	2004P60219 US	METHOD AND SYSTEM FOR IMPROVING THE TOPOGRAPHY OF A MEMORY ARRAY
6/7/2004	10/862,636	2004P60223 US	LDC IMPLANT FOR MIRRORBIT TO IMPROVE VT ROLL-OFF AND FORM SHARPER JUNCTION
6/14/2005	11/152,547	2004P60250 US	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
6/16/2004	10/869,286	2004P60265 US	ALIGNMENT MARKS WITH SALICIDED SPACERS BETWEEN BITLINES FOR ALIGNMENT SIGNAL IMPROVEMENT
6/23/2005	11/165,008	2004P60293 US	SEMICONDUCTOR DEVICE AND SOURCE VOLTAGE CONTROL METHOD
7/20/2004	10/896,292	2004P60320 US	APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS
8/6/2008	12/187,276	2004P60320 US01	APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS
7/20/2004	10/896,299	2004P60317 US	METHOD FOR PROGRAMMING DUAL BIT MEMORY DEVICES TO REDUCE COMPLEMENTARY BIT DISTURBANCE
8/2/2004	10/909,693	2004P60352 US	FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE
8/11/2004	10/916,167	2004P60354 US	METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS AND LITHOGRAPHY MASKS
8/13/2004	10/917,562	2004P60356 US	USING THIN UNDOPED TEOS WITH BPTEOS ILD OR BPTEOS ILD ALONE TO IMPROVE CHARGE LOSS AND CONTACT RESISTANCE IN MULTI BIT MEMORY DEVICES
8/30/2005	11/215,850	2004P60380 US	NON-VOLATILE MEMORY DEVICE, AND CONTROL METHOD THEREFOR

9/22/2004	10/945,914	2004P60406 US	METHODS AND SYSTEMS FOR REDUCING ERASE TIMES IN FLASH MEMORY DEVICES
10/26/2005	11/259,874	2004P60450 US	NON-VOLATILE MEMORY DEVICE
11/1/2004	10/976,816	2004P60467 US	SYSTEM AND METHOD FOR PROTECTING SEMICONDUCTOR DEVICES
11/2/2004	10/979,516	2004P60474 US	METHOD OF MAKING A MEMORY CELL
11/5/2004	10/982,296	2004P60479 US	MULTI BIT PROGRAM ALGORITHM
11/30/2005	11/291,318	2004P60505 US	SEMICONDUCTOR DEVICE, FABRICATING METHOD THEREOF, AND PHOTOMASK
11/30/2005	11/290,001	2004P60496 US	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
11/30/2005	11/291,342	2004P60498 US	SEMICONDUCTOR MEMORY AND METHOD OF FABRICATING THE SAME
12/1/2004	11/001,940	2004P60507 US	METHOD, SYSTEM, AND CIRCUIT FOR PERFORMING A MEMORY RELATED OPERATION
12/2/2004	11/003,208	2004P60511 US	METHOD FOR ACHIEVING INCREASED CONTROL OVER INTERCONNECT LINE THICKNESS ACROSS A WAFER AND BETWEEN WAFERS
12/7/2004	11/006,034	2004P60517 US	INPUT OF TEST CONDITIONS AND OUTPUT GENERATION FOR BUILT-IN SELF TEST
5/11/2005	11/126,330	2004P60524 US	SEMICONDUCTOR MEMORY DEVICE
4/23/2008	12/108,256	2004P60524 US01	SEMICONDUCTOR MEMORY DEVICE HAVING NON-VOLATILE MEMORY CIRCUITS IN SINGLE CHIP
12/28/2004	11/024,257	2004P60557 US	SENSE AMPLIFIERS WITH HIGH VOLTAGE SWING
11/15/2007	11/985,427	2004P60557 US01	SENSE AMPLIFIERS WITH HIGH VOLTAGE SWING
12/21/2005	11/317,083	2004P60555 US	FABRICATION METHOD FOR A SEMICONDUCTOR DEVICE
12/28/2004	11/023,914	2004P60558 US	CURRENT SENSING ARCHITECTURE FOR HIGH BITLINE VOLTAGE, RAIL TO RAIL OUTPUT SWING AND VCC NOISE CANCELLATION
1/27/2006	11/341,029	2005P60212 US	METHOD AND APPARATUS FOR ADDRESS ALLOTTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE
8/27/2008	12/199,684	2005P60212 US01	METHOD AND APPARATUS FOR ADDRESS ALLOTTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE
10/12/2010	12/903,065	2005P60212 US02	METHOD AND APPARATUS FOR ADDRESS ALLOTTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE
7/1/2008	12/166,293	2005P60221 US01	CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICES
1/25/2006	11/339,352	2006P60298 US	STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICE
2/7/2005	11/052,688	2005P60251 US	MEMORY ELEMENT USING ACTIVE LAYER OF BLENDED MATERIALS

2/23/2005	11/062,641	2005P60295 US	SYSTEM AND METHOD FOR ERASING A MEMORY CELL
3/8/2005	11/076,252	2005P60345 US	DECODER FOR MEMORY DEVICE
3/8/2005	11/075,999	2005P60347 US	METHOD FOR CONTAINING A SILICIDED GATE WITHIN A SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY
4/30/2010	12/770,805	2005P60347 US01	METHOD FOR CONTAINING A SILICIDED GATE WITHIN A SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY
3/16/2006	11/378,444	2005P60354 US	MEMORY DEVICE AND CONTROL METHOD THEREFOR
3/23/2005	11/087,944	2005P60361 US	CURRENT SENSING CIRCUIT WITH A CURRENT-COMPENSATED DRAIN VOLTAGE REGULATION
3/25/2005	11/089,708	2005P60377 US	MEMORY DEVICE WITH IMPROVED DATA RETENTION
3/29/2005	11/091,982	2005P60388 US	QUAD BIT USING HOT-HOLE ERASE FOR CBD CONTROL
4/4/2005	11/099,339	2005P60446 US	NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION
4/27/2006	11/414,082	2005P60498 US	SEMICONDUCTOR DEVICE WITH REDUCED TRANSISTOR BREAKDOWN VOLTAGE FOR PREVENTING SUBSTRATE JUNCTION CURRENTS
4/27/2005	11/116,571	2005P60502 US	MULTI-CHIP MODULE AND METHOD OF MANUFACTURE
6/15/2005	11/152,375	2005P60280 US	JUNCTION LEAKAGE SUPPRESSION IN MEMORY DEVICES
3/29/2011	13/074,836	2005P60280 US01	JUNCTION LEAKAGE SUPPRESSION IN MEMORY DEVICES
6/24/2005	11/165,329	2005P60313 US	MEMORY DEVICE WITH BURIED BIT LINE STRUCTURE
6/28/2006	11/478,537	2005P60320 US	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR
12/21/2010	12/974,754	2005P60320 US01	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR
7/30/2009	12/512,741	2005P60318 US01	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
11/15/2013	14/081,987	2005P60318 US09	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
10/15/2010	12/905,716	2005P60318 US05	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
3/6/2012	13/413,527	2005P60318 US07	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
6/28/2006	11/478,554	2005P60318 US	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR
7/30/2009	12/512,638	2005P60318 US02	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME

10/11/2010	12/901,990	2005P60318 US04	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
9/11/2012	13/610,368	2005P60318 US08	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
6/18/2010	12/819,071	2005P60318 US03	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
10/5/2011	13/253,634	2005P60318 US06	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
12/8/2011	13/314,932	2006P60581 US01	CAPACITIVE ELEMENT USING MOS TRANSISTORS
6/30/2006	11/479,373	2006P60581 US	METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
12/8/2011	13/315,060	2006P60581 US02	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE
7/1/2005	11/173,930	2005P60378 US	POWER INTERCONNECT STRUCTURE FOR BALANCED BITLINE CAPACITANCE IN A MEMORY ARRAY
7/6/2005	11/174,560	2005P60389 US	PROGRAMMING A MEMORY DEVICE
7/27/2005	11/189,874	2005P60420 US	SYSTEM AND METHOD FOR IMPROVING RELIABILITY IN A SEMICONDUCTOR DEVICE
7/27/2006	11/495,116	2005P60413 US	FLASH MEMORY DEVICE COMPRISING BIT-LINE CONTACT REGION WITH DUMMY LAYER BETWEEN ADJACENT CONTACT HOLES
12/12/2011	13/323,538	2005P60413 US01	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR
8/1/2005	11/193,391	2005P60442 US	METHODS AND SYSTEMS FOR REDUCING THE THRESHOLD VOLTAGE DISTRIBUTION FOLLOWING A MEMORY CELL ERASE
10/6/2009	12/574,427	2005P60456 US01	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
8/8/2006	11/501,449	2005P60456 US	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
10/6/2009	12/574,413	2005P60456 US02	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
6/7/2011	13/155,278	2005P60456 US03	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
2/19/2013	13/771,043	2005P60456 US04	SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME
8/29/2005	11/212,850	2005P60499 US	FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE
10/31/2007	11/931,992	2005P60499 US01	FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE
8/18/2009	12/543,404	2005P60515 US01	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR
8/30/2006	11/513,693	2005P60515 US	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR

9/20/2005	11/229,527	2005P60552 US	HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH DENSITY DATA STORAGE
9/20/2005	11/229,529	2005P60549 US	FLASH MEMORY PROGRAMMING WITH DATA DEPENDENT CONTROL OF SOURCE LINES
10/4/2005	11/242,773	2005P60574 US	RELIABLE AND SCALABLE VIRTUAL GROUND MEMORY ARRAY FORMED WITH REDUCED THERMAL CYCLE
10/14/2005	11/250,913	2005P60575 US	VOLTAGE SUPPLY CIRCUIT FOR MEMORY ARRAY PROGRAMMING
10/31/2005	11/262,651	2005P60591 US	MEMORY ARRAY
2/22/2006	11/358,206	2005P60592 US	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE PERFORMING ERASE OPERATION THAT CREATES NARROW THRESHOLD DISTRIBUTION
12/7/2006	11/636,111	2005P60617 US	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR
2/23/2005	11/062,629	2005P60299 US	SYSTEM AND METHOD FOR GATE FORMATION IN A SEMICONDUCTOR DEVICE
1/18/2006	11/333,208	2006P60293 US	CONTROLLING THE LATCHUP EFFECT
12/15/2014	14/570,801	2006P60293 US01	CONTROLLING THE LATCHUP EFFECT
1/20/2006	11/336,464	2006P60297 US	FAST RAIL-TO-RAIL VOLTAGE COMPARATOR AND METHOD FOR RAIL-TO-RAIL VOLTAGE COMPARISON
2/5/2007	11/702,845	2006P60315 US01	DUAL STORAGE NODE MEMORY
9/20/2013	14/033,170	2006P60315 US02	DUAL STORAGE NODE MEMORY
2/5/2007	11/702,846	2006P60317 US01	FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS
4/16/2014	14/254,237	2006P60317 US02	FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS
12/15/2006	11/639,666	2006P60320 US01	METHOD FOR FABRICATING MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES
2/9/2006	11/350,556	2006P60326 US	SWITCHABLE MEMORY DIODES BASED ON FERROELECTRIC/CONJUGATED POLYMER HETEROSTRUCTURES AND/OR THEIR COMPOSITES
12/9/2011	13/316,137	2006P60326 US01	SWITCHABLE MEMORY DIODES BASED ON FERROELECTRIC/CONJUGATED POLYMER HETEROSTRUCTURES AND/OR THEIR COMPOSITES
2/27/2007	11/712,299	2006P60362 US	SEMICONDUCTOR DEVICE HAVING LOWER LEAKAGE CURRENT BETWEEN SEMICONDUCTOR SUBSTRATE AND BIT LINES
12/14/2011	13/326,012	2006P60362 US01	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING LOWER LEAKAGE CURRENT BETWEEN SEMICONDUCTOR SUBSTRATE AND BIT LINES
3/9/2006	11/371,023	2006P60376 US	OXYGEN ELIMINATION FOR DEVICE PROCESSING
3/16/2006	11/378,464	2006P60393 US	METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

4/5/2006	11/399,130	2006P60452 US	METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES
4/5/2006	11/398,415	2006P60455 US	FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT
9/11/2009	12/557,721	2006P60455 US01	FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT
9/13/2010	12/880,541	2006P60528 US02	METHOD FOR FORMING BIT LINES FOR SEMICONDUCTOR DEVICES
3/14/2008	12/048,549	2006P60528 US01	METHOD FOR FORMING BIT LINES FOR SEMICONDUCTOR DEVICES
5/3/2006	11/416,551	2006P60534 US	METHOD FOR DETERMINING WORDLINE CRITICAL DIMENSION IN A MEMORY ARRAY AND RELATED STRUCTURE
9/11/2006	11/518,207	2006P60540 US	NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE, ERASE METHOD FOR SAME, AND TEST METHOD FOR SAME
6/12/2006	11/423,638	2006P60564 US	METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE
12/5/2007	11/950,811	2006P60564 US01	METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE
8/2/2006	11/497,597	2006P60611 US	RAMP GATE ERASE FOR DUAL BIT FLASH MEMORY
10/3/2006	11/538,408	2006P60271 US	METHOD AND APPARATUS FOR SECTOR ERASE OPERATION IN A FLASH MEMORY ARRAY
10/11/2007	11/974,295	2006P60277 US	IMPROVED ORNAND FLASH MEMORY AND METHOD FOR CONTROLLING THE SAME
10/21/2013	14/059,077	2006P60296 US01	CONTACTS FOR SEMICONDUCTOR DEVICES
12/3/2019	16/701,496	2006P60296 US02	CONTACTS FOR SEMICONDUCTOR DEVICES
12/6/2006	11/634,777	2006P60358 US	BARRIER REGION UNDERLYING SOURCE/DRAIN REGIONS FOR DUAL-BIT MEMORY DEVICES
12/6/2006	11/634,776	2006P60356 US	METHOD TO PROVIDE A HIGHER REFERENCE VOLTAGE AT A LOWER POWER SUPPLY IN FLASH MEMORY DEVICES
12/7/2006	11/608,032	2006P60360 US	MEMORY DEVICE PROTECTION LAYER
11/20/2007	11/986,331	2007P60270 US	NONVOLATILE STORAGE DEVICE AND CONTROL METHOD THEREOF
11/20/2007	11/986,509	2007P60267 US	HIGH SPEED CASCODE CIRCUIT WITH LOW POWER CONSUMPTION
12/29/2009	12/648,984	2007P60267 US01	NONVOLATILE MEMORY DEVICE
12/18/2006	11/612,413	2006P60388 US	DUAL-BIT MEMORY DEVICE HAVING TRENCH ISOLATION MATERIAL DISPOSED NEAR BIT LINE CONTACT AREAS
12/19/2006	11/612,992	2006P60392 US	METHOD AND APPARATUS FOR MULTI-CHIP PACKAGING

3/9/2010	12/720,547	2006P60392 US01	METHOD AND APPARATUS FOR MULTI-CHIP PACKAGING
12/19/2006	11/612,863	2006P60398 US	ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS
7/6/2010	12/831,085	2006P60398 US01	ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS
12/20/2006	11/613,383	2006P60408 US	FLASH MEMORY DEVICE WITH EXTERNAL HIGH VOLTAGE SUPPLY
3/16/2007	11/724,775	2006P60410 US01	USING THICK SPACER FOR BITLINE IMPLANT THEN REMOVE
3/16/2007	11/724,726	2006P60426 US01	USING IMPLANTED POLY-1 TO IMPROVE CHARGING PROTECTION IN DUAL-POLY PROCESS
12/20/2006	11/613,513	2006P60418 US	SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION
7/20/2010	12/840,165	2006P60418 US01	SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION
12/20/2006	11/614,048	2006P60420 US	METHODS FOR FABRICATING A SPLIT CHARGE STORAGE NODE SEMICONDUCTOR MEMORY
12/22/2006	11/615,365	2006P60475 US	METHOD OF FORMING SPACED-APART CHARGE TRAPPING STACKS
1/29/2010	12/696,409	2006P60475 US01	METHOD OF FORMING SPACED-APART CHARGE TRAPPING STACKS
12/22/2006	11/615,489	2006P60478 US	FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME
6/18/2013	13/920,742	2006P60478 US01	FLASH MEMORY DEVICES AND METHODS FOR FABRICATING SAME
12/22/2006	11/615,280	2006P60483 US	NEGATIVE WORDLINE BIAS FOR REDUCTION OF LEAKAGE CURRENT DURING FLASH MEMORY OPERATION
12/26/2006	11/646,157	2006P60492 US	DEEP BITLINE IMPLANT TO AVOID PROGRAM DISTURB
12/26/2006	11/645,475	2006P60496 US	THIN OXIDE DUMMY TILING AS CHARGE PROTECTION
12/27/2006	11/616,544	2006P60517 US	LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE
12/16/2010	12/970,675	2006P60517 US01	LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE
12/16/2010	12/970,687	2006P60517 US02	LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE
12/21/2007	12/004,919	2006P60500 US	SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME, AND METHOD OF MANUFACTURING THE SAME
1/24/2011	13/012,664	2006P60500 US01	SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME, AND METHOD OF MANUFACTURING THE SAME

3/21/2014	14/222,399	2006P60500 US02	SYSTEM WITH MEMORY HAVING VOLTAGE APPLYING UNIT
12/20/2007	12/004,969	2006P60488 US	METHODS AND STRUCTURES FOR DISCHARGING PLASMA FORMED DURING THE FABRICATION OF SEMICONDUCTOR DEVICE
12/21/2007	11/963,400	2006P60491 US	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
12/27/2006	11/616,718	2006P60502 US	DUAL-BIT MEMORY DEVICE HAVING ISOLATION MATERIAL DISPOSED UNDERNEATH A BIT LINE SHARED BY ADJACENT DUAL-BIT MEMORY CELLS
9/10/2012	13/608,698	2006P60517 US03	LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE
1/11/2007	11/652,785	2007P60238 US	A SHALLOW BIPOLAR JUNCTION TRANSISTOR
1/19/2007	11/625,150	2007P60246 US	FULLY ASSOCIATIVE BANKING FOR MEMORY
2/1/2008	12/012,388	2008P60270 US	FLIP-CHIP PACKAGE COVERED WITH TAPE
2/1/2008	12/012,390	2007P60252 US	PROGRAM AND ERASE DISABLING CONTROL OF WPCAM BY DOUBLE CONTROLS
3/21/2011	13/052,486	2007P60252 US01	SEMICONDUCTOR DEVICE WITH DOUBLE PROGRAM PROHIBITION CONTROL
2/5/2008	12/026,417	2007P60262 US	SEMICONDUCTOR DEVICE AND METHOD FOR ADJUSTING REFERENCE LEVELS OF REFERENCE CELLS
8/30/2010	12/871,693	2007P60262 US01	SEMICONDUCTOR DEVICE AND METHOD FOR ADJUSTING REFERENCE LEVELS OF REFERENCE CELLS
3/16/2007	11/687,436	2007P60298 US	DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY
3/16/2007	11/687,487	2007P60295 US	STATE CHANGE SENSING
3/16/2007	11/687,492	2007P60294 US	HIGH ACCURACY ADAPTIVE PROGRAMMING
3/28/2008	12/058,471	2007P60330 US	NON-VOLATILE MEMORY DEVICE, NON-VOLATILE MEMORY SYSTEM AND CONTROL METHOD FOR THE NON-VOLATILE MEMORY DEVICE IN WHICH DRIVING ABILITY OF A SELECTOR TRANSISTOR IS VARIED
4/24/2008	12/109,239	2007P60376 US	NONVOLATILE STORAGE DEVICE AND BIAS CONTROL METHOD THEREOF
5/23/2008	12/126,686	2007P60428 US	MULTIPLE PROGRAMMING OF SPARE MEMORY REGION FOR NONVOLATILE MEMORY
6/5/2008	12/133,689	2007P60462 US	ULTRAVIOLET BLOCKING STRUCTURE AND METHOD FOR SEMICONDUCTOR DEVICE
5/30/2008	12/130,583	2007P60464 US	SEMICONDUCTOR DEVICE AND CONTROLLING METHOD FOR THE SAME
6/25/2007	11/821,653	2007P60473 US	METHOD OF CONSTRUCTING A STACKED-DIE SEMICONDUCTOR STRUCTURE
6/25/2007	11/767,623	2007P60474 US	PROCESS APPLYING DIE ATTACH FILM TO SINGULATED DIE

7/1/2008	12/166,288	2007P60477 US	SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING A SEMICONDUCTOR DEVICE
7/21/2008	12/176,997	2007P60481 US	SYNCHRONOUS MEMORY DEVICES AND CONTROL METHODS FOR PERFORMING BURST WRITE OPERATIONS
7/25/2008	12/180,306	2007P60484 US	LATERAL CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR WORDLINE
2/19/2016	15/048,886	2007P60484 US01	LATERAL CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR WORDLINE
7/21/2008	12/177,039	2007P60485 US	NONVOLATILE MEMORY DEVICE HAVING A PLURALITY OF MEMORY BLOCKS
9/9/2010	12/878,656	2007P60485 US01	NONVOLATILE MEMORY DEVICE HAVING A PLURALITY OF MEMORY BLOCKS
7/31/2008	12/183,756	2007P60489 US	SELF-ALIGNED CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR DEVICE
4/26/2011	13/094,744	2007P60489 US01	SELF-ALIGNED CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR DEVICE
8/8/2007	11/835,538	2007P60494 US	USE OF A POLYMER SPACER AND SI TRENCH IN A BITLINE JUNCTION OF A FLASH MEMORY CELL TO IMPROVE TPD CHARACTERISTICS
6/30/2010	12/827,069	2007P60494 US01	USE OF A POLYMER SPACER AND SI TRENCH IN A BITLINE JUNCTION OF A FLASH MEMORY CELL TO IMPROVE TPD CHARACTERISTICS
8/8/2007	11/835,542	2007P60493 US	ORO AND ORPRO WITH BIT LINE TRENCH TO SUPPRESS TRANSPORT PROGRAM DISTURB
7/26/2011	13/190,565	2007P60493 US01	ORO AND ORPRO WITH BIT LINE TRENCH TO SUPPRESS TRANSPORT PROGRAM DISTURB
8/20/2008	12/195,307	2007P60506 US	PLASMA TREATED METAL SILICIDE LAYER FORMATION
8/20/2007	11/841,468	2007P60508 US	CMOS LOGIC COMPATIBLE NON-VOLATILE MEMORY CELL STRUCTURE, OPERATION, AND ARRAY CONFIGURATION
8/28/2007	11/895,901	2007P60513 US	METHOD AND STRUCTURE OF MINIMIZING MOLD BLEEDING ON A SUBSTRATE SURFACE OF A SEMICONDUCTOR PACKAGE
9/19/2008	12/234,337	2007P60525 US	SEMICONDUCTOR DEVICE INCLUDING A PRESSURE-CONTACT SECTION
10/17/2007	11/874,076	2007P60546 US	FAST SINGLE PHASE PROGRAM ALGORITHM FOR QUADBIT
9/19/2012	13/622,796	2012P60134 US	SEMICONDUCTOR MEMORY DEVICE FEATURING SELECTIVE DATA STORAGE IN A STACKED MEMORY CELL STRUCTURE
10/25/2007	11/924,169	2007P60558 US	SPLIT CHARGE STORAGE NODE OUTER SPACER PROCESS
12/29/2010	12/980,716	2007P60558 US01	SPLIT CHARGE STORAGE NODE OUTER SPACER PROCESS

10/26/2007	11/924,823	2007P60560 US	SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK
12/22/2009	12/644,457	2007P60560 US01	SELECTIVE SILICIDE FORMATION USING RESIST ETCH BACK
10/30/2007	11/929,097	2007P60568 US	CONTROL OF TEMPERATURE SLOPE FOR BAND GAP REFERENCE VOLTAGE IN A MEMORY DEVICE
10/30/2007	11/928,865	2007P60566 US	NON-VOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELLS AND MULTI-LEVEL CELLS WITHIN THE SAME MEMORY
10/30/2007	11/928,434	2007P60565 US	ERROR CORRECTION CODING IN FLASH MEMORY DEVICES
10/30/2007	11/929,761	2007P60567 US	MEMORY ARRAY OF PAIRS OF NONVOLATILE MEMORY CELLS USING FOWLER-NORDHEIM PROGRAMMING AND ERASING
11/5/2007	11/935,049	2007P60237 US	DECODING SYSTEM CAPABLE OF REDUCING SECTOR SELECT AREA OVERHEAD FOR FLASH MEMORY
11/6/2007	11/935,717	2007P60245 US	CONTROLLED BIT LINE DISCHARGE FOR CHANNEL ERASES IN NONVOLATILE MEMORY
11/27/2007	11/945,316	2007P60279 US	SPI AUTO-BOOT MODE
11/29/2007	11/947,424	2007P60293 US	WEAVABLE FIBER PHOTOVOLTAIC COLLECTORS
12/5/2007	11/951,262	2007P60311 US	CIRCUIT PRE-CHARGE TO SENSE A MEMORY LINE
12/13/2007	11/956,032	2007P60344 US	PROGRAMMING IN MEMORY DEVICES USING SOURCE BITLINE VOLTAGE BIAS
12/17/2007	11/957,737	2007P60362 US	SI TRENCH BETWEEN BITLINE HDP FOR BVDSS IMPROVEMENT
12/20/2007	11/961,772	2007P60382 US	EXTENDING FLASH MEMORY DATA RETENSION VIA REWRITE REFRESH
12/21/2007	11/963,508	2007P60425 US	CONTROLLING AC DISTURBANCE WHILE PROGRAMMING
8/8/2012	13/569,442	2007P60425 US03	CONTROLLING AC DISTURBANCE WHILE PROGRAMMING
12/30/2009	12/650,118	2007P60425 US01	CONTROLLING AC DISTURBANCE WHILE PROGRAMMING
6/9/2011	13/156,763	2007P60425 US02	CONTROLLING AC DISTURBANCE WHILE PROGRAMMING
12/21/2007	11/963,200	2007P60413 US	DATA COMMIT ON MULTICYCLE PASS COMPLETE WITHOUT ERROR
12/21/2007	11/963,078	2007P60410 US	SYSTEM AND METHOD FOR OPTIMIZED ERROR CORRECTION IN FLASH MEMORY ARRAYS
1/4/2008	12/006,744	2008P60226 US	TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS
2/22/2010	12/710,153	2008P60226 US01	TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS

5/13/2011	13/107,724	2008P60226 US02	TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS
5/25/2012	13/481,582	2008P60226 US03	TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS
1/10/2008	11/972,312	2008P60236 US	NON-VOLATILE MEMORY DEVICE AND METHODS OF USING
1/9/2008	11/971,331	2008P60234 US	LOW-H PLASMA TREATMENT WITH N2 ANNEAL FOR ELECTRONIC MEMORY DEVICES
2/13/2008	12/030,485	2008P60282 US	MEMORY DEVICE AND METHOD THEREOF
2/14/2008	12/031,458	2008P60283 US	METHOD OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING FEATURES WITHIN A MASK AND A SELECTIVE REMOVAL PROCESS
2/20/2008	12/034,316	2008P60290 US	DECODING SYSTEM CAPABLE OF CHARGING PROTECTION FOR FLASH MEMORY DEVICES
3/14/2008	12/048,474	2008P60300 US	USING LPDDR1 BUS AS TRANSPORT LAYER TO COMMUNICATE TO FLASH
3/27/2008	12/057,203	2008P60307 US	BITLINE VOLTAGE DRIVER
7/23/2010	12/842,409	2008P60307 US01	BITLINE VOLTAGE DRIVER
3/31/2008	12/059,816	2008P60313 US	FLASH MEMORY AND OPERATING SYSTEM KERNEL
4/16/2008	12/082,988	2008P60324 US	METHOD OF IMPROVING ADHESION OF DIELECTRIC CAP TO COPPER
8/6/2018	16/056,183	2017P60053 US01	METHOD OF REDUCING CHARGE LOSS IN NON-VOLATILE MEMORIES
6/5/2017	15/614,271	2017P60053 US	METHOD OF REDUCING CHARGE LOSS IN NON-VOLATILE MEMORIES
5/5/2008	12/114,966	2008P60341 US	BITCELL CURRENT SENSE DEVICE AND METHOD THEREOF
12/8/2014	14/562,789	2014P60131 US	METHODS, CIRCUITS, DEVICES, SYSTEMS AND MACHINE EXECUTABLE CODE FOR READING FROM A NON-VOLATILE MEMORY ARRAY
5/18/2018	15/984,071	2014P60129 US01	BLOCK MAPPING SYSTEMS AND METHODS FOR STORAGE DEVICE
5/28/2008	12/127,919	2008P60356 US	ADDRESS CACHING STORED TRANSLATION
6/6/2008	12/134,905	2008P60362 US	SENSE AMPLIFIER WITH CAPACITANCE-COUPLED DIFFERENTIAL SENSE AMPLIFIER
10/20/2014	14/518,560	2014P60129 US	OVERLAID ERASE BLOCK MAPPING
10/17/2014	14/517,201	2014P60128 US	SIMULTANEOUS PROGRAMMING OF MANY BITS IN FLASH MEMORY
8/28/2014	14/472,043	2014P60124 US	TEST CONTROL CIRCUIT, SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR TESTING THE SAME
8/13/2014	14/458,542	2014P60122 US	INTEGRATION OF SEMICONDUCTOR MEMORY CELLS AND LOGIC CELLS
6/29/2018	16/023,546	2014P60120 US02	SPLIT-GATE SEMICONDUCTOR DEVICE WITH L-SHAPED GATE
2/15/2017	15/433,848	2014P60120 US01	SPLIT-GATE SEMICONDUCTOR DEVICE WITH L-SHAPED GATE

8/4/2014	14/450,727	2014P60120 US	SPLIT-GATE SEMICONDUCTOR DEVICE WITH L-SHAPED GATE
6/15/2018	16/010,142	2014P60117 US01	BOOTING AN APPLICATION FROM MULTIPLE MEMORIES
6/7/2011	13/154,616	2008P60362 US01	DETERMINING A LOGIC STATE BASED ON CURRENTS RECEIVED BY A SENSE AMPLIFER
6/30/2014	14/319,079	2014P60117 US	BOOTING AN APPLICATION FROM MULTIPLE MEMORIES
5/22/2014	14/284,812	2014P60113 US	METHODS, CIRCUITS, DEVICES AND SYSTEMS FOR INTEGRATED CIRCUIT VOLTAGE LEVEL SHIFTING
5/27/2009	12/472,735	2008P60364 US03	IMAGING DEVICE HAVING A RADIATION DETECTING STRUCTURE DISPOSED AT A SEMICONDUCTOR SUBSTRATE WITH A THERMALIZING MATERIAL AND A FIRST RADIATION-REACTIVE MATERIAL SENSITIVE TO NEUTRON RADIATION (AS AMENDED)
6/1/2018	15/995,926	2014P60112 US01	METHODS, CIRCUITS, DEVICES, AND SYSTEMS FOR SENSING AN NVM CELL
7/24/2012	13/556,819	2008P60364 US05	IMAGING DEVICE HAVING A RADIATION DETECTING STRUCTURE SENSITIVE TO NEUTRON RADIATION
7/28/2010	12/844,888	2008P60364 US04	SYSTEM AND METHOD FOR DETECTING PARTICLES WITH A SEMICONDUCTOR DEVICE
3/12/2014	14/207,303	2013P60142 US02	BURIED TRENCH ISOLATION IN INTEGRATED CIRCUITS
3/5/2013	13/786,216	2008P60364 US06	A CHARGE STORAGE DEVICE FOR DETECTING ALPHA PARTICLES
3/6/2014	14/199,837	2014P60109 US	MEMORY ACCESS BASES ON ERASE CYCLE TIME
10/12/2017	15/730,952	2014P60108 US01	MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ
2/24/2014	14/188,048	2014P60108 US	MEMORY SUBSYSTEM WITH WRAPPED TO CONTINUOUS READ
8/11/2008	12/189,746	2008P60393 US	MULTI-LEVEL STORAGE ALGORITHM TO EMPHASIZE DISTURB CONDITIONS
8/15/2008	12/228,691	2008P60394 US	METHOD OF MEASURING FLASH MEMORY CELL CURRENT
9/2/2008	12/231,369	2008P60413 US	METHOD FOR ACHIEVING VERY SMALL FEATURE SIZE IN SEMICONDUCTOR DEVICE BY UNDERTAKING SILICIDE SIDEWALL GROWTH AND ETCHING
12/19/2018	16/226,216	2014P60100 US02	MULTI-LAYER INTER-GATE DIELECTRIC STRUCTURE AND METHOD OF MANUFACTURING THEREOF
5/26/2017	15/606,255	2014P60100 US01	MULTI-LAYER INTER-GATE DIELECTRIC STRUCTURE AND METHOD OF MANUFACTURING THEREOF
12/30/2013	14/143,317	2013P60168 US	FORMATION OF GATE SIDEWALL STRUCTURE
12/20/2013	14/136,358	2013P60167 US	GATE FORMATION MEMORY BY PLANARIZATION

9/17/2008	12/284,002	2008P60418 US	ELECTRICALLY PROGRAMMABLE AND ERASABLE MEMORY DEVICE AND METHOD OF FABRICATION THEREOF
12/20/2013	14/135,863	2013P60166 US	CT-NOR DIFFERENTIAL BITLINE SENSING ARCHITECTURE
12/18/2013	14/132,422	2013P60164 US	INCREASING LITHOGRAPHIC DEPTH OF FOCUS WINDOW USING WAFER TOPOGRAPHY
11/27/2013	14/092,554	2013P60158 US	AUTO RESUME OF IRREGULAR ERASE STOPPAGE OF A MEMORY SECTOR
11/7/2013	14/073,914	2013P60157 US	METHODS CIRCUITS APPARATUSES AND SYSTEMS FOR SENSING A LOGICAL STATE OF A NON-VOLATILE MEMORY CELL AND NON-VOLATILE MEMORY DEVICES PRODUCED ACCORDINGLY
11/6/2013	14/073,031	2013P60156 US	METHODS, CIRCUITS, SYSTEMS AND COMPUTER EXECUTABLE INSTRUCTION SETS FOR PROVIDING ERROR CORRECTION OF STORED DATA AND DATA STORAGE DEVICES UTILIZING SAME
1/13/2014	14/153,900	2008P60418 US01	ELECTRICALLY PROGRAMMABLE AND ERASEABLE MEMORY DEVICE
10/17/2013	14/056,547	2013P60151 US	MULTIPLE PHASE-SHIFT PHOTOMASK AND SEMICONDUCTOR MANUFACTURING METHOD
10/16/2013	14/054,880	2013P60149 US	MEMORY PROGRAM UPON SYSTEM FAILURE
9/22/2008	12/234,737	2008P60429 US	FLASH MIRROR BIT ARCHITECTURE USING SINGLE PROGRAM AND ERASE ENTITY AS LOGICAL CELL
9/22/2008	12/234,738	2008P60430 US	SECTOR CONFIGURE REGISTERS FOR A FLASH DEVICE GENERATING MULTIPLE VIRTUAL GROUND DECODING SCHEMES
10/15/2018	16/160,008	2013P60148 US02	METHOD FOR PROVIDING READ DATA FLOW CONTROL OR ERROR REPORTING USING A READ DATA STROBE
9/22/2008	12/234,740	2008P60431 US	QUAD+BIT STORAGE IN TRAP BASED FLASH DESIGN USING SINGLE PROGRAM AND ERASE ENTITY AS LOGICAL CELL
9/21/2016	15/271,527	2013P60148 US01	METHOD FOR PROVIDING READ DATA FLOW CONTROL OR ERROR REPORTING USING A READ DATA STROBE
9/22/2008	12/234,733	2008P60432 US	HIGH VT STATE USED AS ERASE CONDITION IN TRAP BASED NOR FLASH CELL DESIGN
10/15/2013	14/054,265	2013P60148 US	METHOD FOR PROVIDING READ DATA FLOW CONTROL OR ERROR REPORTING USING A READ DATA STROBE
10/11/2013	14/051,859	2013P60147 US	ION IMPLANTATION-ASSISTED ETCH-BACK PROCESS FOR IMPROVING SPACER SHAPE AND SPACER WIDTH CONTROL
10/11/2013	14/051,828	2013P60146 US	SPACER FORMATION WITH STRAIGHT SIDEWALL

9/22/2008	12/234,734	2008P60433 US	EEPROM EMULATION IN FLASH DEVICE
10/10/2013	14/050,490	2013P60145 US	MULTI-PASS SOFT PROGRAMMING
11/3/2017	15/802,721	2013P60142 US05	SELF-ALIGNED TRENCH ISOLATION IN INTEGRATED CIRCUITS
6/24/2016	15/191,882	2013P60142 US04	SELF-ALIGNED TRENCH ISOLATION IN INTEGRATED CIRCUITS
10/8/2013	14/048,863	2013P60142 US01	SELF-ALIGNED TRENCH ISOLATION IN INTEGRATED CIRCUITS
11/2/2015	14/929,428	2013P60143 US01	POWER SUPPLY INCLUDING REGULATING TRANSISTOR FOR PROVIDING CURRENT TO A LOAD AND NON-VOLATILE MEMORY DEVICES PRODUCED ACCORDINGLY
10/8/2013	14/048,076	2013P60143 US	METHODS CIRCUITS APPARATUSES AND SYSTEMS FOR PROVIDING CURRENT TO A NON-VOLATILE MEMORY ARRAY AND NON-VOLATILE MEMORY DEVICES PRODUCED ACCORDINGLY
9/22/2008	12/234,736	2008P60434 US	DYNAMIC ERASE STATE IN FLASH DEVICE
6/13/2013	13/917,141	2013P60121 US	SCREENING FOR REFERENCE CELLS IN A MEMORY
6/10/2013	13/913,909	2013P60120 US	PROGRAMMABLE LATENCY COUNT TO ACHIEVE HIGHER MEMORY BANDWIDTH
4/22/2013	13/867,618	2013P60112 US	CHARGE-TRAP NOR WITH SILICON-RICH NITRIDE AS A CHARGE TRAP LAYER
4/18/2013	13/865,714	2013P60111 US	DIE SEAL LAYOUT FOR VFTL DUAL DAMASCENE IN A SEMICONDUCTOR DEVICE
4/4/2013	13/856,816	2013P60109 US	ERASE VERIFICATION CIRCUITRY FOR SIMULTANEOUSLY AND CONSECUTIVELY VERIFYING A PLURALITY OF ODD AND EVEN-NUMBERED FLASH MEMORY TRANSISTORS AND METHOD THEREOF
4/3/2013	13/856,313	2013P60108 US	MODIFIED LOCAL SEGMENTED SELF-BOOSTING OF MEMORY CELL CHANNELS
7/14/2009	12/502,592	2008P60435 US	MEMORY, MEMORY OPERATING METHOD, AND MEMORY SYSTEM
10/10/2008	12/249,261	2008P60448 US	SYSTEM AND METHOD FOR MULTI-LAYER GLOBAL BITLINES
3/8/2013	13/790,979	2013P60105 US	PIPELINING IN A MEMORY
2/18/2013	13/769,398	2013P60101 US	MEMORY DEVICE WITH SOURCE-SIDE SENSING
10/21/2008	12/255,622	2008P60454 US	APPARATUS AND METHOD FOR GENERATING WIDE-RANGE REGULATED SUPPLY VOLTAGES FOR A FLASH MEMORY
2/7/2013	13/761,217	2013P60099 US	NON-VOLATILE MEMORY DEVICE WITH AN EPLI COMPARATOR
10/24/2008	12/258,067	2007P60556 US	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
4/13/2017	15/487,141	2013P60098 US01	MANUFACTURING OF FET DEVICES HAVING LIGHTLY DOPED DRAIN AND SOURCE REGIONS

10/30/2008	12/262,123	2008P60456 US	APPARATUS AND METHOD FOR PLACEMENT OF BOOSTING CELL WITH ADAPTIVE BOOSTER SCHEME
4/17/2017	15/489,695	2013P60097 US03	NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS
1/26/2016	15/006,288	2013P60097 US02	NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS
9/30/2014	14/501,536	2013P60097 US01	NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS
1/30/2013	13/753,676	2013P60097 US	NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS
1/9/2013	13/737,321	2013P60092 US	PROGRAMMABLE AND FLEXIBLE REFERENCE CELL SELECTION METHOD FOR MEMORY DEVICES
11/6/2008	12/266,512	2008P60460 US	FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS
4/19/2016	15/133,026	2013P60090 US01	BURIED HARD MASK FOR EMBEDDED SEMICONDUCTOR DEVICE PATTERNING
1/7/2013	13/735,156	2013P60090 US	BURIED HARD MASK FOR EMBEDDED SEMICONDUCTOR DEVICE PATTERNING
2/25/2013	13/776,337	2008P60460 US01	FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS
12/28/2012	13/729,153	2012P60160 US	DESIGN FOR TEST (DFT) READ SPEED THROUGH TRANSITION DETECTOR IN BUILT-IN SELF-TEST (BIST) SORT
2/24/2016	15/052,709	2012P60159 US01	MEMORY DEVICE WITH INTERNAL COMBINATION LOGIC
12/21/2012	13/725,415	2012P60159 US	MEMORY DEVICE WITH INTERNAL COMBINATION LOGIC
2/25/2013	13/776,310	2008P60460 US02	FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS
4/10/2018	15/949,328	2012P60158 US01	CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF FABRICATING SAME
12/14/2012	13/715,185	2012P60158 US	CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF FABRICATING SAME
11/17/2008	12/313,134	2008P60466 US	HIGH ULTRAVIOLET LIGHT ABSORBANCE SILICON OXYNITRIDE FILM FOR IMPROVED FLASH MEMORY DEVICE PERFORMANCE
12/14/2012	13/715,705	2012P60152 US	PROCESS CHARGING PROTECTION FOR SPLIT GATE CHARGE TRAPPING FLASH
2/10/2017	15/430,157	2012P60151 US02	SPLIT GATE CHARGE TRAPPING MEMORY CELLS HAVING DIFFERENT SELECT GATE AND MEMORY GATE HEIGHTS
6/17/2015	14/742,201	2012P60151 US01	USE DISPOSABLE GATE CAP TO FORM TRANSISTORS, AND SPLIT GATE CHARGE TRAPPING MEMORY CELLS

11/18/2008	12/273,289	2008P60468 US	ELECTROPLATING APPARATUS AND METHOD WITH UNIFORMITY IMPROVEMENT
3/3/2016	15/060,249	2012P60150 US01	THREE DIMENSIONAL CAPACITOR
12/16/2015	14/971,531	2012P60149 US01	CHARGE TRAPPING SPLIT GATE EMBEDDED FLASH MEMORY AND ASSOCIATED METHODS
11/24/2008	12/276,604	2008P60472 US	MULTI-PHASE PROGRAMMING OF MULTI-LEVEL MEMORY
11/17/2009	12/620,172	2008P60232 US	SEMICONDUCTOR MEMORY AND METHOD AND SYSTEM FOR ACTUATING SEMICONDUCTOR MEMORY
7/19/2019	16/517,393	2012P60156 US04	MEMORY FIRST PROCESS FLOW AND DEVICE
6/15/2018	16/009,543	2012P60156 US03	MEMORY FIRST PROCESS FLOW AND DEVICE
12/5/2008	12/329,475	2008P60243 US	MEMORY EMPLOYING REDUNDANT CELL ARRAY OF MULTI-BIT CELLS
9/29/2016	15/281,010	2012P60156 US02	MEMORY FIRST PROCESS FLOW AND DEVICE
6/13/2016	15/181,138	2012P60156 US01	MEMORY FIRST PROCESS FLOW AND DEVICE
12/14/2012	13/715,577	2012P60156 US	MEMORY FIRST PROCESS FLOW AND DEVICE
9/12/2014	14/484,417	2012P60153 US01	INTEGRATED CIRCUITS WITH NON-VOLATILE MEMORY AND METHODS FOR MANUFACTURE
12/14/2012	13/715,565	2012P60153 US	INTEGRATED CIRCUITS WITH NON-VOLATILE MEMORY AND METHODS FOR MANUFACTURE
11/19/2012	13/680,507	2012P60141 US	DATA REFRESH IN NON-VOLATILE MEMORY
12/9/2008	12/316,042	2007P60467 US01	DIE OFFSET DIE TO DIE BONDING
11/2/2015	14/930,484	2012P60135 US01	SUPPLY POWER DEPENDENT CONTROLLABLE WRITE THROUGHPUT FOR MEMORY APPLICATIONS
12/9/2008	12/316,041	2007P60467 US02	DIE OFFSET DIE TO BONDING
12/9/2008	12/330,928	2008P60247 US	DETERMINISTIC-BASED PROGRAMMING IN MEMORY
12/12/2008	12/334,221	2007P60336 US	ELECTRONIC CIRCTUI
12/17/2008	12/337,396	2007P60359 US	STACKED SEMICONDUCTOR DEVICES AND A METHOD FOR FABRICATING THE SAME
12/19/2008	12/340,288	2008P60364 US01	RADIATION DETECTING ELECTRONIC DEVICE AND METHODS OF OPERATING
10/4/2012	13/644,895	2012P60135 US	SUPPLY POWER DEPENDENT CONTROLLABLE WRITE THROUGHPUT FOR MEMORY APPLICATIONS
8/3/2012	13/566,187	2012P60129 US	POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP
7/31/2012	13/563,206	2012P60128 US	BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY
7/10/2012	13/545,469	2012P60123 US	LEAKAGE REDUCING WRITELINE CHARGE PROTECTION CIRCUIT
12/22/2008	12/341,886	2007P60379 US	TIME REDUCTION OF ADDRESS SETUP/HOLD TIME FOR SEMICONDUCTOR MEMORY
6/1/2012	13/486,972	2012P60120 US	METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY ADAPTIVE ALGORITHM
5/15/2012	13/471,854	2012P60119 US	SOFT ERROR RESISTANT CIRCUITRY

4/2/2012	13/437,324	2012P60113 US	ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS
1/10/2011	12/987,466	2007P60379 US01	TIME REDUCTION OF ADDRESS SETUP/HOLD TIME FOR SEMICONDUCTOR MEMORY
3/30/2012	13/435,445	2012P60112 US	APPARATUS AND METHOD FOR A REDUCED PIN COUNT (RPC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL
2/17/2012	13/399,537	2012P60103 US	REDUNDANCY LOADING EFFICIENCY
12/22/2008	12/342,008	2008P60268 US	HTO OFFSET AND BL TRENCH PROCESS FOR MEMORY DEVICE TO IMPROVE DEVICE PERFORMANCE
3/23/2011	13/069,710	2008P60268 US01	HTO OFFSET AND BL TRENCH PROCESS FOR MEMORY DEVICE TO IMPROVE DEVICE PERFORMANCE
1/25/2012	13/357,842	2012P60100 US	CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES
12/22/2008	12/342,016	2008P60269 US	HTO OFFSET FOR LONG LEFFECTIVE, BETTER DEVICE PERFORMANCE
12/7/2011	13/313,699	2011P60120 US	HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM
12/17/2013	14/109,157	2008P60269 US01	HTO OFFSET FOR LONG LEFFECTIVE, BETTER DEVICE PERFORMANCE
7/18/2011	13/185,390	2011P60097 US	METHOD AND MANUFACTURE FOR EMBEDDED FLASH TO ACHIEVE HIGH QUALITY SPACERS FOR CORE AND HIGH VOLTAGE DEVICES AND LOW TEMPERATURE SPACERS FOR HIGH PERFORMANCE LOGIC DEVICES
6/30/2016	15/198,235	2011P60096 US03	METHOD AND APPARATUS FOR STAGGERED START-UP OF A PREDEFINED, RANDOM, OR DYNAMIC NUMBER OF FLASH MEMORY DEVICES
5/19/2015	14/716,719	2011P60096 US02	METHOD AND APPARATUS FOR STAGGERED START-UP OF A PREDEFINED, RANDOM, OR DYNAMIC NUMBER OF FLASH MEMORY DEVICES
12/6/2013	14/099,340	2011P60096 US01	METHOD AND APPARATUS FOR STAGGERED START-UP OF A PREDEFINED, RANDOM OR DYNAMIC NUMBER OF FLASH MEMORY DEVICES
6/16/2011	13/162,520	2011P60096 US	METHOD AND APPARATUS FOR STAGGERED START-UP OF A PREDEFINED, RANDOM, OR DYNAMIC NUMBER OF FLASH MEMORY DEVICES
4/29/2011	13/098,389	2011P60090 US	APPARATUS AND METHOD FOR EXTERNAL CHARGE PUMP ON FLASH MEMORY MODULE
4/29/2011	13/098,378	2011P60092 US	METHOD AND APPARATUS FOR TEMPERATURE COMPENSATION FOR PROGRAMMING AND ERASE DISTRIBUTIONS IN A FLASH MEMORY
12/22/2008	12/342,011	2008P60265 US	HTO OFFSET SPACERS AND DIP OFF PROCESS TO DEFINE JUNCTION

12/30/2008	12/346,699	2008P60279 US	METHOD AND APPARATUS FOR PERFORMING SEMICONDUCTOR MEMORY OPERATIONS
4/29/2011	13/098,364	2011P60091 US	METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY WRITE ALGORITHM FOR FAST BITS
1/21/2011	13/011,706	2011P60080 US	SYSTEM AND METHOD FOR ADDRESSING THRESHOLD VOLTAGE SHIFTS OF MEMORY CELLS IN AN ELECTRONIC PRODUCT
1/21/2010	12/691,633	2010P60119 US	HIGH SPEED MEMORY HAVING A PROGRAMMABLE READ PREAMBLE
6/10/2011	13/158,179	2010P60169 US	NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND DATA WRITE METHOD FOR THE SAME
9/10/2010	12/880,018	2010P60166 US	APPARATUS AND METHOD FOR DATA CAPTURE USING A READ PREAMBLE
2/5/2009	12/366,519	2009P60196 US	FRACTURED ERASE SYSTEM AND METHOD
9/10/2010	12/879,992	2010P60165 US	APPARATUS AND METHOD FOR READ PREAMBLE DISABLE
2/24/2015	14/630,238	2009P60196 US01	FRACTURED ERASE SYSTEM AND METHOD
2/10/2009	12/368,835	2009P60198 US	SYSTEMS AND METHODS FOR LOCATING ERROR BITS IN ENCODED DATA
9/10/2010	12/880,021	2010P60164 US	APPARATUS, METHOD, AND MANUFACTURE FOR USING A READ PREAMBLE TO OPTIMIZE DATA CAPTURE
2/23/2009	12/390,550	2009P60200 US	ADJACENT WORDLINE DISTURB REDUCTION USING BORON/INDIUM IMPLANT
8/10/2010	12/853,856	2010P60160 US	STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK
5/19/2009	12/468,615	2009P60241 US	RADIATION DETECTING DEVICE AND METHOD OF OPERATING
9/13/2012	13/613,448	2012P60133 US	RADIATION DETECTING DEVICE AND METHOD OF OPERATING
5/27/2009	12/473,037	2009P60244 US	IMPROVEMENT IN CHARGE RETENTION FOR FLASH MEMORY BY MANIPULATING THE PROGRAM DATA METHODOLOGY
6/29/2009	12/494,114	2009P60248 US	MEMORY EMPLOYING INDEPENDENT DYNAMIC REFERENCE AREAS
7/14/2009	12/502,891	2006P60351 US01	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
8/31/2012	13/600,527	2010P60155 US01	HIGH READ SPEED MEMORY WITH GATE ISOLATION
6/28/2010	12/824,352	2010P60155 US	HIGH READ SPEED MEMORY WITH GATE ISOLATION
9/21/2015	14/860,035	2010P60140 US02	DATA WRITING METHOD AND SYSTEM
1/7/2014	14/149,484	2010P60140 US01	DATA WRITING METHOD AND SYSTEM
8/4/2010	12/850,470	2009P60253 US	SEMICONDUCTOR MEMORY, SYSTEM, AND METHOD OF CONTROLLING SEMICONDUCTOR MEMORY
3/23/2011	13/070,186	2010P60140 US	DATA WRITING METHOD AND SYSTEM

12/18/2009	12/642,162	2009P60274 US	HIGH READ SPEED ELECTRONIC MEMORY WITH SERIAL ARRAY TRANSISTORS
12/23/2009	12/646,279	2009P60275 US	READ PREAMBLE FOR DATA CAPTURE OPTIMIZATION
2/3/2011	13/020,636	2010P60138 US	SEMICONDUCTOR MEMORY
12/23/2009	12/646,291	2009P60276 US	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
11/5/2012	13/668,935	2009P60276 US02	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
3/28/2014	14/228,384	2009P60276US03	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
1/24/2013	13/749,246	2010P60138 US01	SEMICONDUCTOR MEMORY READ AND WRITE ACCESS
3/3/2011	13/039,839	2010P60132 US	DATA-PROCESSING METHOD, PROGRAM, AND SYSTEM
3/23/2010	12/729,905	2009P60276 US01	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
2/7/2011	13/022,410	2010P60124 US	SEMICONDUCTOR MEMORY INCLUDING PROGRAM CIRCUIT OF NONVOLATILE MEMORY CELLS AND SYSTEM
2/5/2010	12/701,391	2010P60120 US	METHOD AND SYSTEM FOR AUTOMATED GENERATION OF MASKS FOR SPACER FORMATION FROM A DESIRED FINAL WAFER PATTERN
1/20/2010	12/690,590	2010P60118 US	FIELD PROGRAMMABLE REDUNDANT MEMORY FOR ELECTRONIC DEVICES
4/12/2019	16/383,078	2009P60276 US04	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
3/5/2020	16/810,241	2009P60276 US05	VARIABLE READ LATENCY ON A SERIAL MEMORY BUS
1/7/2010	12/683,732	2010P60116 US	MEMORY DEVICE
10/17/2014	14/517,470	2009P60278 US01	LINE-EDGE ROUGHNESS IMPROVEMENT FOR SMALL PITCHES