PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT8228696

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
WELLS FARGO CAPITAL FINANCE, LLC, AS SUCCESSOR BY MERGER TO WACHOVIA CAPITAL FINANCE CORPORATION (WESTERN)	09/29/2023

RECEIVING PARTY DATA

Name:	NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR OPERATING COMPANY
Street Address:	4321 JAMBOREE ROAD
City:	NEWPORT BEACH
State/Country:	CALIFORNIA
Postal Code:	92660

PROPERTY NUMBERS Total: 178

Property Type	Number
Patent Number:	4698417
Patent Number:	4749662
Patent Number:	4694565
Patent Number:	4697328
Patent Number:	4879583
Patent Number:	5043787
Patent Number:	5047828
Patent Number:	4947225
Patent Number:	5935397
Patent Number:	6119368
Patent Number:	6187672
Patent Number:	6071809
Patent Number:	6239026
Patent Number:	6143593
Patent Number:	6255192
Patent Number:	6245663
Patent Number:	6211561
Patent Number:	6417094
Patent Number:	6339000

Property Type	Number
Patent Number:	6180976
Patent Number:	6251568
Patent Number:	6291361
Patent Number:	6787911
Patent Number:	6271127
Patent Number:	6924196
Patent Number:	6445073
Patent Number:	6225681
Patent Number:	6261918
Patent Number:	6233178
Patent Number:	6383821
Patent Number:	6284623
Patent Number:	6280794
Patent Number:	6475895
Patent Number:	6198170
Patent Number:	6251796
Patent Number:	6329290
Patent Number:	6479194
Patent Number:	6380078
Patent Number:	6411492
Patent Number:	6444136
Patent Number:	6490032
Patent Number:	6514825
Patent Number:	6630710
Patent Number:	6309922
Patent Number:	6417755
Patent Number:	6410975
Patent Number:	6396122
Patent Number:	6365479
Patent Number:	6514886
Patent Number:	6534406
Patent Number:	6328848
Patent Number:	6444591
Patent Number:	6486532
Patent Number:	6620732
Patent Number:	6638819
Patent Number:	6740985
Patent Number:	6430028

Property Type	Number
Patent Number:	6534372
Patent Number:	6836400
Patent Number:	6387770
Patent Number:	6506659
Patent Number:	6534802
Patent Number:	6746928
Patent Number:	6444535
Patent Number:	6459104
Patent Number:	6798065
Patent Number:	6509623
Patent Number:	6653679
Patent Number:	6559022
Patent Number:	6602793
Patent Number:	6597022
Patent Number:	6617619
Patent Number:	6639256
Patent Number:	6759674
Patent Number:	6943414
Patent Number:	6586307
Patent Number:	6580104
Patent Number:	6475849
Patent Number:	6583494
Patent Number:	6586297
Patent Number:	6683366
Patent Number:	6589850
Patent Number:	6838352
Patent Number:	6597057
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Patent Number:	6830967
Patent Number:	6765243
Patent Number:	6747523
Patent Number:	6759729
Patent Number:	6787879
Patent Number:	6830982
Patent Number:	6893931
Patent Number:	6867477
Patent Number:	6716558

Property Type	Number
Patent Number:	6673688
Patent Number:	6680235
Patent Number:	6716711
Patent Number:	6781214
Patent Number:	6830625
Patent Number:	6727716
Patent Number:	6919272
Patent Number:	6818520
Patent Number:	6764913
Patent Number:	6770541
Patent Number:	6797580
Patent Number:	6812107
Patent Number:	6774411
Patent Number:	6680521
Patent Number:	6933085
Patent Number:	6797578
Patent Number:	6861308
Patent Number:	6809353
Patent Number:	6867440
Patent Number:	6894328
Patent Number:	6777777
Patent Number:	6627539
Application Number:	09754806
Application Number:	10321877
Application Number:	10054438
Application Number:	09833953
Application Number:	10915797
Application Number:	10434961
Application Number:	10888406
Application Number:	10442449
Application Number:	11175720
Application Number:	10995769
Application Number:	10371307
Application Number:	10865153
Application Number:	10892015
Application Number:	11112194
Application Number:	11198425
Application Number:	10842943

Property Type	Number
Application Number:	10850187
Application Number:	10712067
Application Number:	10952256
Application Number:	06544914
Application Number:	07062007
Application Number:	07068383
Application Number:	06456183
Application Number:	06621773
Application Number:	10826507
Application Number:	10758494
Application Number:	11084391
Application Number:	10970645
Application Number:	11018164
Application Number:	11086168
Application Number:	10997638
Application Number:	10997534
Application Number:	11525457
Application Number:	11121360
Application Number:	11146537
Application Number:	60848973
Application Number:	11641500
Application Number:	11542088
Application Number:	11641296
Application Number:	11641504
Application Number:	11641376
Application Number:	11641925
Application Number:	60276277
Application Number:	10843190
Application Number:	10936927
Application Number:	10865634
Application Number:	10313583
Application Number:	10870900
Application Number:	06397052
Application Number:	06397050
Application Number:	06397646
Application Number:	06355445
Application Number:	06531529
Application Number:	09686323

Property Type	Number
Application Number:	09665422
Application Number:	09590462
Application Number:	11003572
Application Number:	09575055
Application Number:	10995762
Application Number:	10190297
Patent Number:	4639142

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	ROBERT J GOODELL
SIGNATURE:	/Robert J. Goodell/
DATE SIGNED:	10/18/2023

Total Attachments: 12
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RELEASE OF SECURITY INTERESTS IN PATENTS

THIS RELEASE OF SECURITY INTERESTS IN PATENTS (this "Release"), dated as of September 29, 2023, is executed by **WELLS FARGO CAPITAL FINANCE, LLC**, a Delaware limited liability company, in its capacity as successor by merger to Wachovia Capital Finance Corporation (Western), a California corporation ("Grantee"), in favor of **NEWPORT FAB, LLC** (d/b/a Jazz Semiconductor Operating Company), a Delaware limited liability company ("Grantor"). All capitalized terms used in this Release and not otherwise defined herein, shall have the respective meanings given to such terms in the Patent Security Agreement (as defined below).

RECITALS

A. WHEREAS, Grantor has pursuant to that certain Patent Security Agreement dated January 6, 2006, recorded in the United States Patent and Trademark Office (the "USPTO") on January 20, 2006 at Reel 017223, Frame 0083, as amended by that certain First Amendment to Patent Security Agreement dated February 28, 2007, recorded in the USPTO on April 4, 2007 at Reel 019111, Frame 0295 (as the same may be amended, amended and restated, restated, supplemented, modified or otherwise in effect prior to the date hereof, the "Patent Security Agreement") granted to Grantee a security interest in and to all of Grantor's right, title and interest in and to (a) the Patents as set forth on Exhibit A; (b) all registrations of the Patents in any State of the United States, any political subdivision thereof and any other country or jurisdiction; (c) all patents, patent rights, applications, recordings and registrations for the protection of inventions and designs hereafter acquired by, granted to, or filed by Grantor, whether based upon, derived from or variations of any invention or designs disclosed in the Patents or otherwise; (d) all extensions, renewals, reissues, divisions, continuations and continuations-in-part of the Patents and Future Patents; (e) all rights to sue for past, present and future infringements of the Patents and Future Patents; (f) all proceeds, including without limitation, license royalties and proceeds of infringement suits, based on the Patents and Future Patents; (g) all licenses and other agreements and all fees, rents, royalties, proceeds or monies thereunder, relating to the Patents and Future Patents and the use thereof; and (h) all trademarks, trademark registrations, trademark registration applications, inventions, drawings, designs, blueprints, surveys, reports, manuals, operating standards, formulae, processes, compounds, methods, know-how, and trade secrets relating to the manufacture of Grantor's products under, utilizing, or in connection with the Patents and Future Patents and all goodwill connected with, symbolized by or related to the foregoing. All of the foregoing items set forth in clauses (a) through (h) are hereinafter referred to collectively as the "Released Collateral"; and

B. WHEREAS, Grantee wishes to terminate and release, without representation or warranty, its security interest in and to the Released Collateral as provided in this Release.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Grantee hereby terminates and releases, without representation or warranty, its security interest in and to the Released Collateral and terminates the Patent Security Agreement. Grantee acknowledges that this Release may be filed along with any other necessary documentation with the USPTO or any other governmental office to evidence the release granted herein at the sole expense of Grantor. Grantee authorizes Grantor and its designees to record this Release with the USPTO and other applicable registry at the sole expense of Grantor and agrees to provide Grantor with any information and additional authorization necessary to effect the release of the security interest in the Released Collateral.

This Release may be executed by means of (a) an electronic signature that complies with the federal Electronic Signatures in Global and National Commerce Act, state enactments of the Uniform Electronic Transactions Act, or any other relevant and applicable electronic signatures law; (b) an original manual signature; or (c) a faxed, scanned, or photocopied manual signature. Each electronic signature or

faxed, scanned, or photocopied manual signature shall for all purposes have the same validity, legal effect, and admissibility in evidence as an original manual signature.

[Signature page follows]

IN WITNESS WHEREOF, Grantee has executed this Release of Security Interests in Patents as of the date first set forth above.

GRANTEE:

WELLS FARGO CAPITAL FINANCE, LLC, a Delaware limited liability company

By: _____
Name: Brian Keller
Title: Authorized Signatory

[Signature Page to Release of Security Interest in Patents]

Exhibit A

See attached.

List of Patents

Title	Patent No.	Filing Date	Issue Date
Production of Oxy-Metallo-Organic Polymer	4,698,417	02/24/1986	10/06/1987
Diffused Field CMOS-Bulk Process	4,749,662	03/03/1986	06/07/1988
Method of Making Hardened CMOS Sub-micron Field Effect Transistors	4,694,565	04/28/1986	09/22/1987
Method of Making Hardened NMOS Sub-micron Field Effect Transistors	4,697,328	04/28/1986	10/06/1987
Diffused Field CMOS-Bulk Process and CMOS Transistors	4,879,583	10/07/1987	11/07/1989
Extremely Small Area NPN Lateral Transistor	5,043,787	06/24/1987	08/27/1991
PNP Type Lateral Transistor with Minimal Substrate Operation Interference	5,047,828	06/24/1987	09/10/1991
Sub-Micron Devices with Method for Forming Sub-Micron Contacts	4,947,225	07/15/1987	08/07/1990
Physical Vapor Deposition Chamber	5,935,397	04/30/1998	08/10/1999
Apparatus for Reducing Cool Chamber Particles	6,119,368	04/30/1998	09/19/2000
Interconnect with Low Dielectric Constant Insulators for Semiconductor Integrated Circuit Manufacturing	6,187,672	09/22/1998	02/13/2001
Methods for Forming High-Performing Dual-Damascene Interconnect Structures	6,071,809	09/25/1998	06/06/2000
Nitride Etch Stop for Poisoned Unlanded Vias	6,239,026	09/28/1998	05/29/2001
Elevated Channel MOSFET	6,143,593	09/29/1998	11/07/2000
Improved Methods for Barrier Layer Formation	6,255,192	09/29/1998	07/03/2001
IC Interconnect Structures and Methods for Making Same	6,245,663	09/30/1998	06/12/2001
Interconnect Structure and Method Employing Air Gaps Between Metal Lines and Between Metal Layers	6,211,561	11/16/1998	04/03/2001
Dual-Damascene Interconnect Structures and Methods of Fabricating Same	6,417,094	12/31/1998	07/09/2002
Methods for Fabricating Interpoly Dielectrics in Non-Volatile Stacked-Gate Memory Structures	6,339,000	09/25/1998	01/15/2002
Thin-Film Capacitors and Methods for Forming the Same	6,180,976	02/02/1999	01/30/2001
Methods and Apparatus for Stripping PhotoResist and Polymer Layers from a Semiconductor Stack in a Non-Corrosive Environment	6,251,568	02/09/1999	06/26/2001
Methods and Apparatus for High-Resolution In-Situ Plasma Etching of Inorganic and Metal Films	6,291,361	03/24/1999	09/18/2001
Interconnect with Low Dielectric Constant Insulators for Semiconductor Integrated Circuit Manufacturing	6,787,911	05/24/1999	09/07/2004

Title	Patent No.	Filing Date	Issue Date
Method for Dual Damascene Process Using Electron Beam and Ion Implantation Cure Methods for Low Dielectric Constant Materials	6,271,127	06/10/1999	08/07/2001
Anti-Reflective Coating and Process Using an Anti-Reflective Coating	6,924,196	08/06/1999	08/02/2005
Damascene Metallization Process and Structure	6,445,073	01/02/1998	09/03/2002
Microelectronic Interconnect Structures and Methods for Forming the Same	6,225,681	09/07/1999	05/01/2001
Method for Creating and Preserving Alignment Marks for Aligning Mask Layers in Integrated Circuit Manufacture	6,261,918	10/01/1999	07/17/2001
Method and Apparatus for Pre-conditioning Flash Memory Devices	6,233,178	10/14/1999	05/15/2001
Semiconductor Device and Process	6,383,821	10/29/1999	05/07/2002
Method of Fabricating Semiconductor Devices Using Shallow Trench Isolation With Reduced Narrow Channel Effect	6,284,623	10/25/1999	09/04/2001
Dielectric Material Suitable for Microelectronic Circuits and Method of Forming Same	6,280,794	11/01/1999	08/28/2001
Semiconductor Device Having a Passivation Layer and Method for its Fabrication	6,475,895	08/06/1999	11/05/2002
Bonding Pad and Support Structure and Method for Their Fabrication	6,198,170	12/16/1999	03/06/2001
Method for Fabrication of Ceramic Tantalum Nitride and Improved Structures Based Thereon	6,251,796	02/24/2000	06/26/2001
Method for Fabrication and Structure for High Aspect Ration Vias	6,329,290	02/24/2000	12/11/2001
Transparent Phase Shift Mask For Fabrication of Small Feature Sizes	6,479,194	02/07/2000	11/12/2002
Method for Fabrication of Damascene Interconnects and Related Structures	6,380,078	05/11/2000	04/30/2002
Structure and Method for Fabrication of an Improved Capacitor	6,411,492	05/24/2000	06/25/2002
Fabrication of Improved Low-K Dielectric Structures	6,444,136	04/25/2000	09/03/2002
Method and Apparatus for Improving a Dark Field Inspection Environment	6,490,032	05/31/2000	12/03/2002
Technique for Reducing 1/F Noise in MOSFETs	6,514,825	06/28/2000	02/04/2003
Elevated Channel MOSFET; Semiconductor Device (e.g., MOSFET) Having a Channel Above the Surface of the Water Containing a Well and a Junction. The Elevated Channel May Be Selectively Epitaxially Grown and Enables Higher Mobility, Enabling a Higher Current Flow At	6,630,710	07/14/2000	10/07/2003
Method for Fabrication of On-chip Inductors and Related Structure	6,309,922	07/28/2000	10/30/2001

Title	Patent No.	Filing Date	Issue Date
Method for Fabrication of High Inductance Inductors and Related Structure	6,417,755	08/25/2000	07/09/2002
Bipolar Transistor with Reduced Base Resistance	6,410,975	09/01/2000	06/25/2002
Method for Fabricating On-Chip Inductors and Related Structure	6,396,122	09/08/2000	05/28/2002
Method for Independent Control of Polycrystalline Silicon-Germanium In a Silicon-Germanium HBT and Related Structure	6,365,479	09/22/2000	04/02/2002
Method for Elimination of Contaminants Prior to Epitaxy	6,514,886	09/22/2000	02/04/2003
Method for Increasing Inductance of On-chip Inductors and Related Structure	6,534,406	02/22/2000	03/18/2003
Apparatus for High-Resolution In-Situ Plasma Etching of Inorganic and Metal Films	6,328,848	09/27/2000	12/11/2001
Method for Reducing Contamination Prior to Epitaxial Growth and Related Structure; Forming Etch Stop Layer on Surface of Wafer, Fabricating Cap Layer on Etch Stop Layer, Selectively Etching Cap Layer Without Etching Etch Stop Layer, Removing Etch Stop Layer, Cleaning Surface of Wafer, Epitaxially Growing Semiconductor	6,444,591	09/30/2000	09/03/2002
Structure for Reduction of Base and Emitter Resistance and Related Method	6,486,532	09/30/2000	11/26/2002
Method for Controlling Critical Dimension in a Polycrystalline Silicon Emitter and Related Structure	6,620,732	11/17/2000	09/16/2003
Method for Fabricating Interfacial Oxide in a Transistor and Related Structure	6,638,819	11/17/2000	10/28/2003
Structure for Bonding Pad and Method for Its Fabrication	6,740,985	11/20/2000	05/25/2004
Method for Fabrication of an MIM Capacitor and Related Structure	6,430,028	11/22/2000	08/06/2002
Method for Fabricating a Self-Aligned Emitter in a Bipolar Transistor	6,534,372	11/22/2000	03/18/2003
Structures Based on Ceramic Tantalum Nitride	6,836,400	01/12/2001	12/28/2004
Thin-Film Capacitors and Methods for Forming the Same	6,387,770	01/30/2001	05/14/2002
High Performance Bipolar Transistor	6,506,659	03/17/2001	01/14/2003
Method for Reducing Base to Collector Capacitance and Related Structure	6,534,802	05/07/2001	03/18/2003
Method for Opening a Semiconductor Region for Fabricating an HBT	6,746,928	05/08/2001	06/08/2004
Method to Reduce Emitter to Base Capacitance and Related Structure; Creating Notch in Dielectric Layer Below Emitter Region Reduces Overlap Area of Capacitor That Forms Between Emitter Region and Base Region, Which Translates to Reduction in Emitter to Base Capacitance	6,444,535	05/09/2001	09/03/2002
Method for Fabricating Lateral PNP Heterojunction Bipolar Transistor and Related Structure	6,459,104	05/10/2001	10/01/2002

Title	Patent No.	Filing Date	Issue Date
Method and Apparatus for High Resolution In-Situ Plasma Etching of Inorganic and Metal Films	6,798,065	09/19/2001	09/28/2004
Microelectronic Air-Gap Structures and Methods of Forming the Same	6,509,623	09/28/2001	01/21/2003
Reduced 1/F Noise in MOSFETs	6,653,679	12/11/2001	11/25/2003
Method for Independent Control of PolyCrystalline Silicon-Germanium in an HBT	6,559,022	01/22/2002	05/06/2003
Pre-Clean Chamber	6,602,793	02/03/2002	08/05/2003
Method for Controlling Critical Dimension in an HBT Emitter and Related Structure	6,597,022	02/04/2002	07/22/2003
Structure for a Selective Epitaxial HBT Emitter	6,617,619	02/04/2002	09/09/2003
Structure for Eliminating Collector-Base Band Gap Discontinuity in an HBT	6,639,256	02/02/2002	10/28/2003
Band Gap Compensated HBT	6,759,674	02/04/2002	07/06/2004
Method for Fabricating a Metal Resistor in an IC Chip and Related Structure	6,943,414	02/08/2002	09/13/2005
Method for Controlling an Emitter Window Opening in an HBT and Related Structure	6,586,307	02/14/2002	07/01/2003
Elimination of Contaminants Prior to Epitaxy and Related Structure	6,580,104	04/01/2002	06/17/2003
Method for Reducing Base Resistance in a Bipolar Transistor	6,475,849	04/26/2002	11/05/2002
Reduced Base Resistance in a Bipolar Transistor	6,583,494	04/26/2002	06/24/2003
Method for Integrating a Metastable Base into a High-Performance HBT and Related Structure	6,586,297	06/01/2002	07/01/2003
Bipolar Transistor and Related Structure; Electrical and Electronic Apparatus Comprising Heterojunctions Having Spacers and Antireflective Coatings Used for High Speed Frequency Response and Amplification	6,683,366	06/04/2002	01/27/2004
Method and System for Fabricating a Bipolar Transistor and Related Structure	6,589,850	07/04/2002	07/08/2003
Damanscene Trench Capacitor for Mixed-Signal/RF IC Applications	6,838,352	07/05/2002	01/04/2005
Epitaxial Growth in a Silicon-Germanium Semiconductor Device with Reduced Contamination	6,597,057	07/10/2002	07/22/2003
Electrostatic Discharge Clamp	6,927,957	07/18/2002	08/09/2005
Method for Fabricating a Self-Aligned Bipolar Transistor and Related Structure	6,784,467	08/13/2002	08/31/2004
Method for Forming CMOS Transistor Spacers in a BiCMOS	6,830,967	10/02/2002	12/14/2004
HBT Having A Controlled Emitter Window Opening	6,765,243	10/04/2002	07/20/2004
BiFET Voltage Controlled Oscillator	6,747,523	12/16/2002	06/08/2004
Temperature Insensitive Resistor in an IC Chip	6,759,729	10/16/2002	07/06/2004
Interfacial Oxide in a Transistor	6,787,879	11/06/2002	09/07/2004

Title	Patent No.	Filing Date	Issue Date
Method for Reducing Extrinsic Base Resistance and Improving Manufacturability in an NPN Transistor	6,830,982	11/07/2002	12/14/2004
Reducing Extrinsic Base Resistance in an NPN Transistor	6,893,931	11/07/2002	05/17/2005
High Gain Bipolar Transistor	6,867,477	11/07/2002	03/15/2005
Transparent Phase Shift Mask for Fabrication of Small Feature Sizes	6,716,558	11/08/2002	04/06/2004
Method for Eliminating Collector-Base Band Gap in an HBT	6,673,688	11/02/2002	01/06/2004
Method for Fabricating a Selective Epitaxial HBT Emitter	6,680,235	02/04/2002	01/20/2004
Method for Fabricating a Self-Aligned Emitter in a Bipolar Transistor	6,716,711	12/02/2002	04/06/2004
Metastable Base in a High-Performance	6,781,214	12/06/2002	08/24/2004
System for Fabricating a Bipolar Transistor	6,830,625	12/07/2002	12/14/2004
Probe Card and Probe Needle for High Frequency Testing	6,727,716	12/16/2002	04/27/2004
Method for Patterning Densely Packed Metal Segments in a Semiconductor Die and Related Structure	6,919,272	02/01/2003	07/19/2005
Method for Controlling Critical Dimension in an HBT	6,818,520	02/10/2003	11/16/2004
Method for Controlling an Emitter Window Opening in an HBT and Related Structure	6,764,913	02/19/2003	07/20/2004
Method for Hard Mask Removal for Deep Trench Isolation and Related Structure	6,770,541	02/20/2003	08/03/2004
Method for Fabricating a Bipolar Transistor in a BiCMOS Process and Related Structure	6,797,580	02/21/2003	09/28/2004
Method for Improved Alignment Tolerance in a Bipolar Transistor	6,812,107	02/26/2003	11/02/2004
Bipolar Transistor With Reduced Emitter to Base	6,774,411	03/06/2003	08/10/2004
High Density Composite MIM Capacitor with Reduced Voltage Dependence in Semiconductor Dies	6,680,521	04/09/2003	01/20/2004
Transparent Phase Shift Mask for Fabricating of Small Feature Sizes	6,933,085	05/02/2003	08/23/2005
Method for Fabrication of Emitter of a Transistor and Related Structure	6,797,578	05/13/2003	09/28/2004
Method for Fabrication of SIGE Layer Having Small Poly Grains and Related Structure	6,861,308	05/13/2003	03/01/2005
Method for Fabricating a Self-Aligned Bipolar Transistor with Planarizing Layer and Related Structure	6,809,353	05/21/2003	10/26/2004
Self-Aligned Bipolar Transistor Without Spacers and Method for Fabricating Same	6,867,440	05/21/2003	03/15/2005
Self-Aligned Bipolar Transistor Having Recessed Spacers and Method for Fabricating Same	6,894,328	05/21/2003	05/17/2005
High Density Composite MIM Capacitor With Flexible Routing in Semiconductor Dies	6,777,777	05/28/2003	08/17/2004
Method of Forming Dual-Damascene Interconnect Structures Employing Low-K Dielectric Materials	6,627,539	09/09/1998	09/30/2003

List of Patents

Title	Patent No.	Filing Date	Issue Date
On-Chip Inductors	09/754,806 7,173,318		2/6/2007
Polycrystalline Silicon Emitter Having an Accurately Controlled Critical Dimension	10/321,877 6,965,132		11/15/2005
Independent Control of Polycrystalline Silicon-Germanium in an HBTand Related Structure	10/054,438 7,183,627		2/27/2007
Low Cost Fabrication Of High Resistivity Resistors	09/833,953	4/11/2001	Pending
SIGE Layer Having Small Poly Grains	10/915,797 7,132,700		11/7/2006
Technique for Reducing Contaminants in Fabrication of Semiconductor Wafers	10/434,961 7,064,073		6/20/2006
Transistor Emitter Having Alternating Undoped and Doped Layers	10/888,406 7,078,744		7/18/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Having Increased Manufacturability and Related Structure	10/442,449 6,979,626		12/27/2005
Fabricating a Self-Aligned Bipolar Transistor Having Increased Manufacturability	11/175,720	7/6/2005	Pending
Self-Aligned Bipolar Transistor Having Increased Manufacturability	10/995,769 7,064,415		6/20/2006
Method for Forming Deep Trench Isolation and Related Structure	10/371,307 7,015,115		3/21/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Having Recessed Spacers	10/865,153 7,033,898		4/25/2006
Bipolar Transistor Fabricated in a BiCMOS Process	10/892,015	7/14/2004	Pending
Densely Packed Metal Segments Patterned in a Semiconductor Die	11/112,194	4/22/2005	Pending
Deep N Wells in Triple Well Structures	11/198,425	8/5/2005	Pending
Deep Trench Isolation Region with Reduced-Size Cavities in Overlying Field Oxide	10/842,943 6,995,449		2/7/2006
High Density Composite MIM Capacitor with Flexible Routing in Semiconductor Dies	10/850,187 7,078,310		7/18/2006
Method for Fabricating a High Density Composite MIM Capacitor with Reduced Voltage Dependence in Semiconductor Dies	10/712,067 7,041,569		5/9/2006
Method for Fabricating a Self-Aligned Bipolar Transistor Without Spacers	10/952,256	9/28/2004	Pending
Small Area High Value Resistor with Greatly Reduced Parasitic Capacitance	06/544,914 4,497,685		2/5/1985
Lateral Transistor Separated from Substrate by Intersecting Slots Filled with Substrate Oxide for Minimal Interference Therefrom	07/062,007 5,031,014		7/9/1991
Complementary NPN and PNP Lateral Transistors Separated from Substrate by Intersecting Slots Filled with Substrate Oxide for Minimal Interference Ther	07/068,383 5,097,316		3/17/1992
Reactive Ion Etching of Molybdenum Silicide and N+ Polysilicon	06/456,183 4,444,617		4/24/1984
Two-Level Transistor Structures and Method Utilizing Minimal Area Therefor	06/621,773 4,593,453		6/10/1986
Composite Ground Shield for Passive Components in a Semiconductor Die	10/826,507 7,154,161		12/26/2006

Title	Patent No.	Filing Date	Issue Date
Circuit for Detecting Arcing in an Etch Tool During Wafer Processing	10/758,494 7,063,988		6/20/2006
Integration of SIGE NPN and Vertical PNP Devices on a Substrate	11/084,391	3/17/2005	Pending
Method for Opto-Electronic Integration on a SOI Substrate and Related Structure	10/970,645	10/20/2004	Pending
SOI Substrate for Integration of Opto-Electronics with SiGe BiCMOS	11/018,164	12/20/2004	Pending
Method for Effective BiCMOS Process Integration	11/086,168	3/21/2005	Pending
Method for Fabricating a MIM Capacitor Having Increased Capacitance Density and Related Structure	10/997,638	11/23/2005	Pending
Method and Structure for Integration of Phosphorus Emitter in an NPN Devise in a BiCMOS Process	10/997,534	11/23/2004	Pending
Integration of Phosphorus Emitter in an NPN Devise in a BiCMOS Process	11/525,457	9/21/2006	Pending
Method for Fabricating a MIM Capacitor High-K Dielectric for Increased Capacitance Density and Related Structure	11/121,360	5/3/2005	Pending
Selective and Non-Selective Epitaxy for Base Integration in a BiCMOS process and related structure	11/146,537	6/6/2005	Pending
Method For Fabricating A Backside Through-Wafer Via In A Processed Wafer And Related Structure	60/848,973	10/2/2006	Pending
Method For Fabricating A Frontside Through-Wafer Via In A Processed Wafer And Related Structure	11/641,500	12/18/2006	Pending
Structure and Method for Encapsulating Microelectronic Devices	11/542,088	10/2/2006	Pending
Method For Fabricating A Substrate-Insulated Frontside Through-Wafer Via In A Processed Wafer And Related Structures	11/641,296	12/18/2006	Pending
Frontside Through-Wafer Vias For Semiconductor Device Region Isolation	11/641,504	12/18/2006	Pending
Method For Preventing Backside Metallization Separation In A Semiconductor Die And Related Structure	11/641,376	12/18/2006	Pending
Method For Fabricating A Top Conductive Layer In A Semiconductor Die And Related Structure	11/641,925	12/18/2006	Pending
Metal Resistor	60/276,277	3/15/2001	Pending
Composite Series Resistor Having Reduced Temperature Sensitivity in an IC Chip	10/843,190 7,078,786		7/18/2006
CMOS Transistor Spacers Formed in a BiCMOS Process	10/936,927 6,992,338		1/31/2006
NPN Transistor Having Reduced Extrinsic Base Resistance and Improved Manufacturability	10/865,634 7,064,361		6/20/2006
An Efficiently Fabricated Bipolar Transistor	10/313,583 6,972,442		12/6/2005
Method for Fabricating a Self-Aligned Bipolar Transistor	10/870,900 7,041,564		5/9/2006
Process for and structure of high density VLSI circuits, having self-aligned gates and contacts for FET devices and conducting lines	06/397,052 4,506,437		3/26/1985
Process for and structure of high density VLSI circuits, having self-aligned gates and contacts for FET devices and conducting lines	06/397,050 4,477,962		7/17/1984

Title	Patent No.	Filing Date	Issue Date
High rate resist polymerization apparatus	06/397,646 4,459,937		7/17/1984
Ion etching process with minimized redeposition	06/355,445 4,396,479		8/2/1983
Method for making a reliable ohmic contact between two layers of integrated circuit metallizations	06/531,529 4,507,852		4/2/1985
Dimension monitoring technique for semiconductor fabrication	484,666 4,639,142		1/27/1987
Method of Fabricating an Interconnect Structure Employing Air Gaps Between Metal Lines and Between Metal Layers	09/686,323 7,056,822		6/6/2006
Damascene Interconnect Structure and Fabrication Method Having Air Gaps Between Metal Lines and Metal Layers	09/665,422 6,984,577		1/10/2006
Double Implant High Performance Varactor and Method for Manufacturing Same	09/590,462 6,995,068		2/7/2006
NPN Transistor Having Reduced Extrinsic Base Resistance and Improved Manufacturability	11/003,572	12/2/2004	Pending
Method for Selective Fabrication of High Capacitance Density Areas in a Low Dielectric Constant Material and related Structure	09/575,055 7,049,246		5/23/2006
Selective Fabrication of High Capacitance Density Areas in a Low Dielectric Constant Material	10/995,762 7,109,125		9/19/2006
Method for Controlling an Emitter Window Opening in an HBT and Related Structure	6,586,307		7/1/2003
Damascene Trench Capacitor for Mixed-Signal/RF IC Applications	6,838,352		1/4/2005
Fabrication of High-Density Capacitors for Mixed Signal/RF Circuits	10/190,297 7,060,557		6/13/2006