PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT8287909

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	PATENT COLLATERAL AGREEMENT - DDTL

CONVEYING PARTY DATA

Name	Execution Date
WESTERN DIGITAL TECHNOLOGIES, INC.	11/17/2023

RECEIVING PARTY DATA

Name:	JPMORGAN CHASE BANK, N.A.
Street Address:	10 SOUTH DEARBORN
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60603

PROPERTY NUMBERS Total: 569

Property Type	Number
Application Number:	18346327
Application Number:	18346329
Application Number:	18346362
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Application Number:	18493379
Application Number:	18493036
Application Number:	18383638
Patent Number:	11756932

CORRESPONDENCE DATA

Fax Number: (800)914-4240

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 800-713-0755
Email: Michael.Violet@wolterskluwer.com
Correspondent Name: CT CORPORATION
Address Line 1: 4400 EASTON COMMONS WAY
Address Line 2: SUITE 125
Address Line 4: COLUMBUS, OHIO 43219

NAME OF SUBMITTER:	SOPHIE BOLT
SIGNATURE:	/Sophie Bolt/
DATE SIGNED:	11/21/2023

Total Attachments: 18
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Form **PTO-1595** (Rev. 6-18)
OMB No. 0651-0027 (exp. 06/30/2021)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

Western Digital Technologies, Inc.

Additional name(s) of conveying party(ies) attached? ☐ Yes ■ No

2. Name and address of receiving party(ies)

Name: JPMORGAN CHASE BANK, N.A.
Internal Address:
Street Address: 10 South Dearborn
City: Chicago
State: IL
Country: USA Zip: 60603

Additional name(s) & address(es) attached? ☐ Yes ■ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) November 17, 2023

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
■ Other Patent Collateral Agreement - DDTL

4. Application or patent number(s): ☐ This document serves as an Oath/Declaration (37 CFR 1.63).

A. Patent Application No.(s)

See Schedule I

B. Patent No.(s)

See Schedule I

Additional numbers attached? ■ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Sophie Bolt
Internal Address: Cahill Gordon & Reindel LLP
Street Address: 32 Old Slip
City: New York
State: NY Zip: 10005
Phone Number: (212) 701-3365
Docket Number:
Email Address: sbolt@cahill.com

6. Total number of applications and patents involved: 569

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number
Authorized User Name

9. Signature: Sophie Bolt

Digitally signed by: Sophie Bolt
DN: CN = Sophie Bolt email = sbolt@cahill.com C = US O = Cahill LLP OU = IP
Date: 2023.11.20 16:36:29 -05'00'

Signature

November 20, 2023
Date

Sophie Bolt
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 18

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Patent Collateral Agreement

This November 17, 2023, Western Digital Technologies, Inc. ("*Debtor*") with its principal place of business and mailing address at 5601 Great Oaks Parkway, San Jose, CA 95119, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the "*Agent*"), with its mailing address at 10 South Dearborn, Chicago, IL 60603, acting as collateral agent hereunder for the Secured Parties as defined in the Security Agreement, dated as of June 20, 2023, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the "*Se- curity Agreement*") for the benefit of the Secured Parties, a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, "*Patent Collateral*"):

(i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on Schedule A hereto (the "*Patents*"); and

(ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

WESTERN DIGITAL TECHNOLOGIES, INC.,
as Debtor

By DocuSigned by: _____
4109E8803D2348...

Name: Michael Ray
Title: Executive Vice President, Chief Legal Officer and Secretary

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By: _____

Name: Timothy D. Lee

Title: Executive Director

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
1	MOUNTING OF CAPACITORS ON PRINTED CIRCUIT BOARDS FOR NON-VOLATILE MEMORY DEVICES	18/346,327
2	FOLDERING ORDERING SCHEME FOR IMPROVED THROUGHPUT IN NON-VOLATILE MEMORY	18/346,329
3	ADAPTIVE WORD LINE STRESS FOR LEAK DETECTION IN NON-VOLATILE MEMORY	18/346,362
4	NON-VOLATILE MEMORY WITH LAYOUT ADAPTIVE PROBLEMATIC WORD LINE DETECTION	18/346,367
5	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING DISCRETE CHARGE STORAGE ELEMENTS AND METHODS OF MAKING THEREOF	18/347,371
6	SEMICONDUCTOR DEVICE INCLUDING METAL INTERCONNECT STRUCTURES THAT CONTAIN SELECTIVELY-GROWN DIELECTRIC SPACERS AND METHODS FOR FORMING THE SAME	18/347,404
7	Data Storage Device and Method for Intelligent Block Allocation	18/218,271
8	Read Collision Avoidance in Sequential Mixed Workloads	18/348,314
9	Hold-Up Capacitor Failure Handling in Data Storage Devices	18/348,316
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23	Zone-Based Garbage Collection in ZNS SSDs	18/349,088
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54	Data Storage Device and Method for Reducing Read Disturbs When Reading Redundantly-Stored Data	18/220,951
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58	Folding Zone Management Optimization in Storage Device	18/352,156
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64	Data Storage Device and Method for Using Zones of Memory in a Read Scrub Operation	18/222,044
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106	DE-FRAGMENTATION ACCELERATION USING OVERLAP TABLE	18/355,097
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141	MEMORY DEVICE AND METHOD OF ASSEMBLING SAME	18/356,838
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143	HARD DISK DRIVE SLIDER SPLIT PAD CONFIGURATION	18/225,084
144	FAST LOOK NEIGHBOR AHEAD FOR DATA RECOVERY	18/224,839
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149	System and Method for Flexible Emergency Power Fail Management for Multiple Persistent Memory Regions	18/224,835
150	Data Storage Device and Method for Logical Range Lock	18/224,856
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175	Method to Enhance Spin Torque Layer Performance in a Spintronic Device	18/226,114
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182	TEMPERATURE DEPENDENT REFRESH READ RATE	18/358,463
183	ESTIMATING PEAK SOURCE CURRENT USING MEMORY DIE SUBSTRATE TEMPERATURE DETECTION	18/358,763
184	POST-PROGRAM ERASE IN 3D NAND	18/358,635
185	DATA INTEGRITY CHECK IN NON-VOLATILE STORAGE	18/358,605
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187	NON-VOLATILE MEMORY WITH INTELLIGENT ERASE TESTING TO AVOID NEIGHBOR PLANE DISTURB	18/358,651
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190	Data Storage Device with Balanced Background Operations and Method Therefor	18/225,789
191	Data Storage Device and Method for Improving Asynchronous Independent Plane Read (AIPR) Utilization	18/225,771
192	Data Storage Device and Method for Optimized Refresh	18/225,766
193	HIGH VOLTAGE FIELD EFFECT TRANSISTORS WITH DIFFERENT SIDEWALL SPACER CONFIGURATIONS AND METHOD OF MAKING THE SAME	18/358,633
194	HIGH VOLTAGE FIELD EFFECT TRANSISTORS WITH DIFFERENT SIDEWALL SPACER CONFIGURATIONS AND METHOD OF MAKING THE SAME	18/358,653
195	CROSS-POINT OVONIC FRUSTUM MEMORY DEVICE AND METHOD OF MAKING THE SAME	18/358,768
196	Two-Dimensional Magnetic Recording Read Head with TaOx Layer for Flat Middle Shield Topography and Method of Forming Thereof	18/226,609
197	Middle Shields Two-Dimensional Magnetic Recording Read Heads	18/226,615
198	CENTER STRUCTURE HAVING ATTACHMENT SUPPORT FOR AN ACTUATOR IN A MULTI-ACTUATOR HARD DISK DRIVE	18/226,584
199	TDMR SOT Read Heads Having Recessed Topological Insulator Materials	18/226,625
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210	PROCESSING COMMANDS IN A SEQUENTIAL WRITE REQUIRED ZONE MODEL	18/359,028
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214	BYPASS BUFFER FOR WORN OUT CODEWORDS	18/359,251
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217	ERROR HANDLING DURING A MEMORY COMPACTION PROCESS	18/359,637
218	THERMALLY CONDUCTIVE SPACER	18/359,645
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221	Data Storage Device and Method for Host-Controlled Data Compression	18/226,449
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225	Enhanced End To End Protection In Key Value Storage Devices	18/359,167
226	DISTRIBUTED TEMPERATURE SENSING SCHEME TO SUPPRESS PEAK ICC IN NON-VOLATILE MEMORIES	18/359,025
227	FULL SEQUENCE PROGRAM FOR EDGE WORD LINE QUAD-LEVEL MEMORY CELLS	18/227,175
228	RAMP SUPPORT FOR A MAGNETIC STORAGE DEVICE	18/360,582
229	MEMORY CONTROLLER WITH COMMON REQUEST BUFFER	18/360,535
230	SYSTEM AND METHOD FOR VALID WINDOW MAXIMIZATION IN TOGGLE MODE LINK USING SYSTEMATIC SKEW ADDITION TO COMPENSATE FOR SSO AND CROSSTALK	18/360,674
231	CURRENT SOURCE FOR READ OF PROGRAMMABLE RESISTANCE MEMORY CELLS	18/360,119
232	MULTI-STEP READ PASS VOLTAGE DISCHARGE FOR ICC REDUCTION	18/360,084
233	ERASE SATURATION MITIGATION IN NON-VOLATILE MEMORY	18/360,075
234	MEMORY CONTROLLER SUPPORT FOR MIXED READ	18/360,096
235	PRINTED CIRCUIT BOARD FOR A REFLOW PROFILING PROCESS	18/360,094
236	BOND WIRE HAVING A RECYCLED THERMOPLASTIC CORE WITH CONDUCTIVE FILLERS	18/360,361
237	MULTI-PLANE HIGH DENSITY CONNECTOR	18/360,167
238	SEMICONDUCTOR DIE STACKING ARCHITECTURE AND CONNECTION METHOD THEREFORE	18/360,555
239	SUSPENSION ARM AND SLIDER CONTACT FOR MAGNETIC STORAGE DEVICE	18/360,594
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241	DYNAMIC BITSCAN FOR NON-VOLATILE MEMORY	18/360,487
242	EVOLVING BAD BLOCK DETECTION IN NON-VOLATILE MEMORY	18/360,520
243	Read Sensor With Ordered Heusler Alloy Free Layer and Semiconductor Barrier Layer	18/227,537
244	System and Method for Measuring Thermal Performance of Substrates used in Semiconductor Device Assembly	18/361,129
245	Semiconductor Device Package with Coupled Substrates	18/361,118
246	Dual Circuit Isolation of Writer to Reader Crosstalk for SGV Modules	18/227,510
247	Tape Head Assembly with Single Beam, Actuator and Spring Adaptor	18/227,520
248	Identification and Retrieval of Recently-Used Files at an External Storage Device	18/361,537
249	Offset Edge of Servo Heads Relative to Data Heads for Signal-to-Noise Ratio Optimization in a Tape Head Module	18/227,513
250	Semiconductor Device Package with Die Stackup and Interposer	18/361,168
251	SPIN-ORBIT TORQUE (SOT) WRITER WITH TOPOLOGICAL INSULATOR MATERIALS	18/361,631
252	Multi-Chip Package with Detachable Chips	18/361,147
253	BINARY READ-BASED FAST ALGORITHM FOR OPTIMAL READ LEVEL ACQUISITION	18/227,581
254	Irregular Jumbo Block Size Unification	18/361,642
255	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD OF MAKING THEREOF USING ION IMPLANTED ETCH STOP LAYER ON A SACRIFICIAL FILL MATERIAL	18/361,594
256	THREE-DIMENSIONAL MEMORY DEVICE WITH THROUGH-STACK CONTACT VIA STRUCTURES AND METHOD OF MAKING THE SAME	18/361,629
257	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING PERIPHERAL CIRCUIT WITH FIN AND PLANAR FIELD EFFECT TRANSISTORS AND METHOD OF MAKING THEREOF	18/361,550
258	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING OVERLYING THIN FILM TRANSISTOR CONTROL CIRCUIT AND METHOD OF MAKING THEREOF	18/361,575
259	ELECTRICALLY COUPLING PRINTED CIRCUIT BOARDS USING A SNAP-FIT CONNECTOR	18/361,037
260	ELECTROLYTIC CAPACITORS HAVING ENCLOSURES THAT ENABLE THE CAPACITORS TO BE SURFACE MOUNTED TO A SUBSTRATE	18/361,061
261	DYNAMICALLY DETERMINING A MEMORY BLOCK THRESHOLD FOR INITIATING A GARBAGE COLLECTION PROCESS	18/361,093
262	SINGLE PACKAGE DATA STORAGE DEVICE	18/361,081
263	SNAP FIT BRACKET FOR ELECTROLYTIC CAPACITORS	18/361,072
264	Removable Memory Card with Efficient Card Lock Mechanism, XY Ratios, and Pads Layout	18/227,499
265	Data Storage Device and Method for Providing External-Interrupt-Based Customized Behavior	18/227,483
266	RECORD AND PLAYBACK COMMANDS FOR STORAGE DEVICES	18/361,531
267	Data Storage Device and Method for Time-Pooled Hot Data Relocation	18/227,466

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268	ADAPTIVE ERASE PULSE TO IMPROVE MEMORY CELL ENDURANCE AND ERASE TIME IN NON-VOLATILE MEMORY	18/360,992
269	NON-VOLATILE MEMORY WITH ADJUSTABLE RAMP RATE	18/361,840
270	NON-VOLATILE MEMORY WITH SUB-BLOCK PROGRAMMING	18/361,842
271	NON-VOLATILE MEMORY WITH DECLINE STATE OPERATION	18/361,841
272	NON-VOLATILE MEMORY WITH NEIGHBOR PLANE PROGRAM DISTURB AVOIDANCE	18/361,843
273	NON-VOLATILE MEMORY WITH MULTIPLE DATA RESOLUTIONS	18/361,839
274	SOT Reader with Recessed SOT Topological Insulator Material	18/228,529
275	Dynamic DC Field Compensator for MAMR Recording Head	18/228,523
276	Data Receiver Design in DDR Memory Interfaces	18/362,388
277	Produce Thinner DTS and Adjustable Capacitance for TDMR Heads	18/228,517
278	APPARATUS AND METHOD FOR COUPLING TO AN ELECTRICAL INTERFACE OF A CIRCUIT BOARD	18/228,054
279	RECONFIGURABLE LINES IN DIFFERENT SUB-BLOCK MODES IN A NAND MEMORY DEVICE	18/228,156
280	UNSELECT WORD LINE SWITCH BIAS SCHEME FOR NON-VOLATILE MEMORY APPARATUS	18/228,088
281	AUTOMATIC XOR DATA PROGRAMMING BY MEMORY DIE FOR UNCORRECTABLE PAGE FAILURE RECOVERY	18/362,197
282	THREE-DIMENSIONAL MEMORY DEVICE WITH LATERALLY SEPARATED SOURCE SELECT ELECTRODES AND METHODS OF FORMING THE SAME	18/362,805
283	POSITIVE SENSING IN LOW POWER OPERATION MODE IN A MEMORY DEVICE	18/228,406
284	LOCAL EXTENSION OF HEAD OVERCOAT WITH A NEAR-FIELD TRANSDUCER EXTENDING TOWARD THE MEDIA-FACING SURFACE	18/362,852
285	METHOD AND APPARATUS FOR SUBSTRATE AND SPACER SEPARATION	18/228,080
286	INSULATION LAYER FOR A SEMICONDUCTOR PACKAGE	18/362,128
287	VERTICALLY MOUNTABLE SNAP FIT BRACKET FOR ELECTROLYTIC CAPACITORS	18/362,157
288	NON-VOLATILE MEMORY WITH CONCURRENT PROGRAMMING	18/362,526
289	TESTING PADDLE FOR SEMICONDUCTOR DEVICE CHARACTERIZATION	18/362,140
290	NON-VOLATILE MEMORY WITH HIGH PERFORMANCE READ	18/362,509
291	POWER-EFFICIENT UNMATCHED DOUT ARCHITECTURE WITH DVW TRAINING	63/516,697
292	HDD head having same gap verify and system for using same	18/229,078
293	DISK HUB FOR RETAINING AND ROTATING MAGNETIC RECORDING MEDIA DURING FILM THICKNESS MEASUREMENT	18/228,835
294	Current Distal to Media Facing Surface	18/229,081
295	DFL Read Head with SiOx Cap Layer on AlOx Refill Layers	18/229,096
296	ASYMMETRIC VREADK TO REDUCE NEIGHBORING WORD LINE INTERFERENCE IN A MEMORY DEVICE	18/228,795
297	WORD LINE DEPENDENT WORD LINE SWITCH DESIGN AND PROGRAMMING TECHNIQUES	18/229,019
298	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING A BIT-LINE-BIAS VERTICAL TRANSISTOR BLOCK AND METHODS OF OPERATING THE SAME	18/363,518
299	HARD DISK DRIVE IDLE SWEEP FOR THERMAL ASPERITY AVOIDANCE	18/229,144
300	CROSS-POINT MAGNETORESISTIVE MEMORY ARRAY CONTAINING CARBON-BASED LAYER AND METHOD OF MAKING THE SAME	18/363,542
301	READ ACCESS MANAGEMENT OF HOST PERFORMANCE BOOSTER (HPB) REGIONS BY A STORAGE DEVICE	18/228,799
302	READ ONLY MODE HANDLING IN STORAGE DEVICES	18/228,806
303	Multi-host bandwidth management considering external and internal traffic	18/363,131
304	SHALLOW ERASE FOR ERASE POOL MANAGEMENT	18/363,470
305	STORAGE DEVICE POOL MANAGEMENT BASED ON OVER-PROVISIONING	18/229,295
306	STORAGE DEVICE POOL MANAGEMENT BASED ON STORAGE DEVICE QUEUE USAGE	18/229,311
307	ADAPTIVE SINGLE-SIDE ERASE TO IMPROVE CELL RELIABILITY	18/229,390
308	NEAR-FIELD TRANSDUCER (NFT) DESIGNS FOR IMPROVED PERFORMANCE OF HEAT-ASSISTED MAGNETIC RECORDING (HAMR)	18/364,413
309	HYBRID ERASE FOR DATA RETENTION THRESHOLD VOLTAGE MARGIN IMPROVEMENT	18/229,257
310	PROGRAM VERIFY WORD LINE RAMPING DELAY FOR LOWER CURRENT CONSUMPTION MODE	18/229,294
311	PRE-SOLDER BUMP PREVENTIVE OVERCOATING	18/229,589
312	MEMORY DEVICE INCLUDING HAFNIUM OR ZIRCONIUM OXIDE CONTAINING BLOCKING DIELECTRIC AND TUNGSTEN NITRIDE BARRIER AND METHODS OF FORMING THE SAME	18/229,489

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313	Integrated Die Ejector for Die Attach Ejector Devices	18/364,685
314	FLUORINATED MEDIA LUBRICANTS WITH REDUCED HYDROCARBON FRACTION FOR DATA STORAGE DEVICES	18/229,777
315	DATA STORAGE DEVICE BACKUP	18/365,017
316	Film and Method for BiSbX (012) Texture for SOT Devices	18/229,772
317	High Capacity Captive Tape Drive	18/229,774
318	SMART EARLY PROGRAM TERMINATION ALGORITHM FOR NEIGHBOR PLANE DISTURB COUNTERMEASURE	18/229,978
319	Near-Field Transducer For Heat Assisted Magnetic Recording Comprising Of Thermally Stable Material Layer	18/229,779
320	Higher Areal Density Non-Local Spin Orbit Torque (SOT) Writer with Topological Insulator Materials	18/229,785
321	DYNAMIC THROTTLING OF INPUT/OUTPUT QUEUES IN A DATA STORAGE DEVICE ARRAY	18/364,723
322	PREDICTIVE ADJUSTMENT OF MULTI-CAMERA SURVEILLANCE VIDEO DATA CAPTURE	18/364,740
323	Phase-Coherent In-Line VCSEL Array with Slider Trailing Mount for HAMR	18/230,018
324	READ POWER SAVINGS BY TEMPORARILY DISABLING BITLINE VOLTAGE	18/229,705
325	OPTIMIZED READ CURRENT CONSUMPTION BASED ON LOWER PAGE READ INFORMATION FOR NON-VOLATILE MEMORY APPARATUS	18/229,748
326	AUTOMATIC BIT LINE VOLTAGE AND BIT LINE VOLTAGE TEMPERATURE COMPENSATION ADJUSTMENT FOR NON-VOLATILE MEMORY APPARATUS CURRENT CONSUMPTION REDUCTION	18/229,782
327	SYSTEMS AND METHODS TO AVOID OVER PROGRAMMING AT INFREQUENT SMART VERIFY ACQUISITION FOR HIGH-PERFORMANCE 3D NAND	18/229,873
328	ENABLING SIGNIFICANT SCALING OF WORDLINE SWITCH WITH WORDLINE DEPENDENT NEGATIVE BITLINE VOLTAGE	18/230,078
329	Continuous Frequency Servo in a Data Storage Device	18/364,759
330	Magnetic Control of Molecule Translocation Speed Through a Nanopore	18/364,506
331	Methods for Improving Track Density in Dual-Reel Removable Tape Devices and Fixed Tape Devices	18/229,775
332	Data Read Synchronization from Phase Modulated Synchronization Fields in a Data Storage Device	18/364,772
333	Tape Heads Having Tiered Servo Readers	18/230,048
334	USING DATA STORAGE DEVICE OPERATIONAL PROFILES FOR INTERFACE-BASED PERFORMANCE LEVELING	18/364,785
335	MULTIPATH INITIATOR FOR DATA STORAGE DEVICE ARRAYS	18/365,025
336	SOLID-STATE DRIVE SECURE DATA WIPING FOR REUSE AND RECYCLING	18/230,145
337	PREDICTIVE ADJUSTMENT OF MULTI-CAMERA SURVEILLANCE VIDEO DATA CAPTURE USING GRAPH MAPS	18/364,730
338	DATA STORAGE DEVICE WITH KEY-VALUE DELETE MANAGEMENT FOR MULTI-HOST NAMESPACES	18/365,033
339	Skipping Completion for Repeat LBAs Based Upon LBA Tracking	18/364,735
340	ACCESS-CONTROLLED DELIVERY OF CONTENT TO NETWORK ATTACHED STORAGE	18/230,610
341	ROTATIONAL DIPPING OF STORAGE DISK MEDIA	18/365,955
342	AROMATIC AND AROMATIC-LIKE CONTAINING MEDIA LUBRICANTS FOR DATA STORAGE DEVICES	18/230,584
343	METHOD AND DISK CARRIER FOR USE IN POLISHING GLASS SUBSTRATE DISKS	18/230,541
344	PLANE AND BLOCK LOCATION DEPENDENT VOLTAGE BIASES IN NAND MEMORY	18/230,336
345	LOWER VREAD FOR ERASED WORD LINES IN POST-WRITE DUMMY READS	18/230,379
346	MAGNETIC RECORDING MEDIA WITH DEAD MAGNETIC LAYER	18/230,559
347	CHANNEL PRE-CHARGE PROCESS FOR MEMORY DEVICES	18/230,371
348	OPEN BLOCK DETECTION METHOD USING FOR FIRST AND SECOND TIME PERIOD READ TIME VALLEY FOR NON-VOLATILE MEMORY APPARATUS	18/230,270
349	COMPUTATIONAL STORAGE DEVICE WITH COMPUTATION PRECISION-DEFINED FIXED POINT DATA GROUPING AND STORAGE MANAGEMENT	18/230,576
350	STORAGE POWER REDUCTION IN BATTERY-OPERATED DEVICES	18/230,586
351	APPARATUS AND METHODS FOR INCREASING CROSS BIT LINE PITCH IN NON-VOLATILE MEMORY CONTROL CIRCUITS	18/365,394
352	Simultaneous Lower Tail Verify With Upper Tail Verify	18/365,894
353	Semiconductor Device Package with Die Stackup and Connection Platform	18/366,396

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354	ABORTED OPERATION DETECTION FOR NONVOLATILE MEMORY WITH NON-UNIFORM ERASE	18/366,213
355	STOP READ GO SETTINGS FOR LOW SUSPEND LATENCY APPLICATIONS	18/230,832
356	ANALOG BITSCAN TECHNIQUES IN A MEMORY DEVICE	18/230,972
357	Data Storage Device and Method for Identifying a Failing Area of Memory Based on a Cluster of Bit Errors	18/230,982
358	Programmable Telemetry and Alerts for Storage Devices	18/366,381
359	NON-VOLATILE MEMORY WITH SUB-BLOCK MODE AND FULL BLOCK MODE	18/366,572
360	PRIVACY-PRESERVING DISTRIBUTED COMPUTING	18/231,706
361	EVALUATING CONVOLUTIONS USING ENCRYPTED DATA	18/231,716
362	HOST INDEPENDENT FORMATTING OF STORAGE DEVICES	18/446,383
363	MEMORY PREFETCH BASED ON MACHINE LEARNING	18/231,730
364	RAISEABLE PROFILE-BASED ACCESS FOR MEDIA CONTENT	18/446,442
365	STORAGE DEVICES HAVING MULTI-CHANNEL CAPACITIVE SENSORS FOR DETECTING GESTURE BASED COMMANDS	18/231,718
366	IN SITU DATA REFRESH WITHOUT ERASE/PROGRAM CYCLES	18/231,395
367	ERASE TECHNIQUES USING ANALOG BITSCAN IN A MEMORY DEVICE	18/231,629
368	STATE-DEPENDENT FAIL BIT COUNT CRITERIA FOR MEMORY APPARATUS PROGRAM PERFORMANCE GAIN	18/231,368
369	Buffer Layers And Interlayers That Promote BiSbx (012) Alloy Orientation For SOT And MRAM Devices	18/232,256
370	DATA STORAGE DEVICE HAVING DUAL ACTUATORS AND METHOD FOR EMERGENCY POWER OFF RETRACT (EPOR) OF DUAL ACTUATORS	18/446,637
371	VCM PWM TO LINEAR MODE TRANSITION OFFSET OPTIMIZATION TO IMPROVE PES	18/446,612
372	DATA STORAGE DEVICE WITH MAPPING AND MITIGATION OF LASER MODE HOP EFFECTS IN HEAT-ASSISTED MAGNETIC RECORDING (HAMR)	18/232,041
373	DATA STORAGE DEVICE READ/WRITE CHANNEL WITH DIRECT RADIAL POSITION DEMODULATION IN ASYNCHRONOUS POSITION ERROR SIGNAL DEMODULATION	18/232,113
374	DATA STORAGE DEVICE WITH ADJACENT TRACK INTERFERENCE-AWARE SERVO TRAJECTORIES	18/232,073
375	DATA STORAGE DEVICE WITH ENHANCED MANAGEMENT OF LASER PRE-BIAS AND LOGIC BLOCK ADDRESSING IN HEAT-ASSISTED MAGNETIC RECORDING	18/232,128
376	ENERGY-ASSISTED MAGNETIC RECORDING DATA STORAGE DEVICE WITH OPPORTUNISTIC BOOSTED LASER PRE-BIASING	18/232,145
377	DATA STORAGE DEVICE WITH RAPID IN-FIELD REPEATABLE RUNOUT NOISE REMOVAL CALIBRATION	18/232,031
378	DATA STORAGE DEVICE CONFIGURED FOR USE WITH A GENERATIVE-ADVERSARIAL-NETWORK (GAN)	18/232,105
379	DATA STORAGE DEVICE CONFIGURED FOR USE WITH A GENERATIVE-ADVERSARIAL-NETWORK (GAN)	18/232,155
380	DATA STORAGE DEVICE WITH WRITE PROTECTION AND GUARANTEED RAPID WRITE VERIFICATION IN ENERGY-ASSISTED RECORDING (EAR)	18/232,003
381	DATA STORAGE DEVICE WITH LASER PRE-BIAS OPTIMIZATION USING DISK THERMAL-MAGNETIC RESPONSE MAPPING IN HEAT-ASSISTED MAGNETIC RECORDING	18/232,009
382	DATA STORAGE DEVICE WITH INTELLIGENT WRITE PROTECTION FOR ENERGY ANOMALIES IN ENERGY-ASSISTED MAGNETIC RECORDING	18/231,905
383	PROACTIVE CACHING OF DATA FOR ACCELERATOR CORES IN A STORAGE DEVICE	18/232,040
384	Protocol For Solid State Drive With High Quality Of Service	18/232,060
385	ENERGY-ASSISTED MAGNETIC RECORDING DATA STORAGE DEVICE WITH ASSISTIVE ENERGY PRE-HEATING FOR WRITING SERVO PATTERNS	18/231,991
386	DATA STORAGE DEVICE WITH ACCELERATED POST-EMERGENCY-POWER-OFF RECOVERY PROCESS	18/231,891
387	PROGRAMMING TECHNIQUES THAT UTILIZE ANALOG BITSCAN IN A MEMORY DEVICE	18/232,117
388	DISAGGREGATED MEMORY MANAGEMENT	18/232,224
389	HOST-INDEPENDENT FORMAT OPERATION OF USB-BASED STORAGE DEVICES	18/232,305
390	HOST-INDEPENDENT DISK OPTIMIZATION AND DATA OPERATIONS FOR USB-BASED STORAGE DEVICES	18/232,310
391	FIVE LEVEL CELL PROGRAM ALGORITHM WITH APPENDED BIT LEVEL ERASE FOR ADDITIONAL THRESHOLD VOLTAGE BUDGET	18/232,010

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392	Translation and Data Management In Storage Devices	18/447,556
393	PREHEATING LASER DIODES WITH REVERSE BIAS FOR HAMR DISK DRIVES	18/447,401
394	STORAGE OF CONTROL DATA INFORMATION	18/447,774
395	SYSTEM CONTROLLED RF SIGNAL SOURCE ARCHITECTURE WITH TRANSDUCER NEAR POLE-TIP FOR MICROWAVE ASSISTED MAGNETIC RECORDING	18/447,419
396	MULTIPLE-ACTUATOR HDD ASSEMBLY UTILIZING MULTIPLE-PREAMP ARCHITECTURE WITH SINGLE POINT TERMINATION	18/447,440
397	Devices, Methods, and Computer-Readable Media to Back-up Parity Information	18/448,116
398	Devices, Methods, and Computer-Readable Media to Store Backed-up Parity Information	18/448,118
399	Devices, Methods, And Computer Readable Media For Control Page Flush Handling	18/447,941
400	DATA STORAGE DEVICE WITH ADAPTIVE CONTROL OF CURRENT BALANCER TO REDUCE POWER CONSUMPTION	18/447,501
401	SMART CARD WITH BUS INTERFACE RECEPTACLE PRINTED AS PART OF PCB	18/232,494
402	DATA STORAGE DEVICE WITH ADAPTIVE CONTROL OF CURRENT BALANCER TO MITIGATE ROTATIONAL VIBRATION (RV) NOISE	18/447,959
403	MAINTAINING CONSISTENT LOCATION FOR SPINDLE INTERRUPTS WHEN SPINDLE MOTOR SWITCHES MODES	18/448,007
404	MANAGING LASER DIODE CAVITY THERMAL TRANSIENTS IN HAMR DISK DRIVES	18/447,989
405	Access control system and a data storage device	18/447,723
406	ENHANCING SPIN UP AND SPIN DOWN TIMES FOR DATA STORAGE DEVICES	18/447,976
407	DATA STORAGE DEVICE WITH LASER WRITE BIAS OPTIMIZATION USING DISK THERMAL-MAGNETIC RESPONSE MAPPING IN HEAT-ASSISTED MAGNETIC RECORDING	18/232,458
408	MEASURING LASER DIODE TEMPERATURE AND PREDICTING MODE HOPS USING LASER DIODE RESISTANCE	18/447,517
409	STEADY STATE LASER DIODE FINGERPRINT MEASUREMENT AND COMPENSATION	18/447,552
410	SINGLE BLOCK MODE BLOCK HANDLING FOR SINGLE-SIDE GIDL ERASE	18/232,538
411	VPASS AUTO LAYER COMPENSATION IN A MEMORY DEVICE	18/232,609
412	GROUND REFERENCED BANDGAP CIRCUIT IN A NEGATIVELY BIASED SUBSTRATE CMOS INTEGRATED CIRCUIT	18/447,562
413	METHOD AND DEVICE FOR SECURE DATA TRANSFER AND STORAGE	18/447,770
414	METHOD AND DEVICE FOR FACILITATING SECURE DATA TRANSFER AND STORAGE	18/447,781
415	DISAGGREGATED MEMORY MANAGEMENT FOR VIRTUAL MACHINES	18/232,780
416	STORAGE-FREE MESSAGE AUTHENTICATORS FOR ERROR-CORRECTING-CODES	18/447,868
417	DYNAMIC MODE SELECTION FOR HYBRID SINGLE-LEVEL CELL AND MULTI-LEVEL CELL DATA STORAGE DEVICES	18/447,738
418	PRIORITY BASED THERMAL MANAGEMENT FOR DATA STORAGE DEVICE ENCLOSURES	18/232,642
419	Write Aggregation Based on NAND Wear Level	18/447,806
420	Address Translation Service for Host Queues	18/447,813
421	Exposed Physical Partitions in Solid-State Storage Devices	18/448,398
422	TEMPERATURE BASED BLOCK READ	18/448,393
423	STREAM TEMPERATURE INTERLEAVE MONITOR	18/448,406
424	DATA STORAGE DEVICE CONFIGURED FOR USE WITH A GENERATIVE-ADVERSARIAL-NETWORK (GAN)	18/233,125
425	Capacitor Health Check For Data Storage Devices	18/448,274
426	Dynamic Garbage Collection Operations	18/448,261
427	THERMAL MANAGEMENT IN DATA STORAGE DEVICE	18/448,656
428	SERVER THERMAL MANAGEMENT	18/448,633
429	SELECTABLE PERFORMANCE-BASED PARTITIONING	18/448,905
430	PACKAGED MEMORY DEVICE WITH OVERHANG SUPPORT STRUCTURE	18/448,296
431	ENERGY-ASSISTED MAGNETIC RECORDING DATA STORAGE DEVICE WITH AVERAGED MEASUREMENT MITIGATION OF ENERGY COMPONENT PROTRUSION	18/232,917
432	SELECTABLE PERFORMANCE BOOST FOR STORAGE DEVICES	18/448,887
433	DATA TRANSMISSION SCHEDULING FOR DISAGGREGATED MEMORY SYSTEMS	18/233,223
434	SEMICONDUCTOR CHIP WITH VARYING THICKNESS PROFILE	18/449,452
435	MAGNETIC RECORDING APPARATUS COMPRISING DISK WITH REDUCED THICKNESS AND REDUCED DISK FLATNESS	18/233,497

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436	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING A METAL OXIDE ETCH STOP LAYER AND METHODS FOR FORMING THE SAME	18/233,697
437	Computational SSD Supporting Rapid File Semantic Search	18/449,116
438	SEGREGATING LARGE DATA BLOCKS FOR DATA STORAGE SYSTEM	18/449,428
439	Error Correction Methods for Computational SSD Supporting Rapid File Semantic Search	18/449,165
440	MACHINE LEARNING DEFECT MANAGEMENT IN STORAGE DEVICES	18/449,278
441	MACHINE LEARNING DEFECT MANAGEMENT IN STORAGE DEVICES	18/449,480
442	THREE-DIMENSIONAL MEMORY DEVICE WITH LAYER CONTACT VIA STRUCTURES LOCATED IN A MEMORY ARRAY REGION AND METHODS OF FORMING THE SAME	18/233,759
443	EARLY DETECTION OF ROOM TEMPERATURE DATA RETENTION PHENOMENA	18/449,491
444	ASYMMETRIC PASS VOLTAGE SCHEME FOR NON-VOLATILE MEMORY APPARATUS SIZE REDUCTION	18/233,640
445	SELECTIVE WIRE COATING DURING WIRE BONDING	18/449,502
446	DUAL FREE LAYER READ HEAD HAVING RECESSED SIDEWALL INSULATOR LAYER AND METHOD OF MAKING THEREOF	18/233,800
447	HEAT HARVESTING IN DATA STORAGE DEVICES	18/449,483
448	ACCESS CONTROL FOR CLOUD-SHARED FILES FROM A STORAGE DEVICE	18/449,646
449	EXPOSED METAL LOOP TO DETECT CORROSION IN A DATA STORAGE DEVICE	18/449,299
450	HEAT ASSISTED MAGNETIC RECORDING (HAMR) WRITE HEAD WITH ENHANCED STABILITY AND METHODS FOR MAKING THE SAME	18/234,248
451	SECURELY ERASING DATA ON INOPERATIVE STORAGE DEVICE	18/233,981
452	MANAGING DATA DESCRIPTOR READS DURING COMMAND PROCESSING IN A STORAGE DEVICE	18/233,970
453	PROGRAMMING TECHNIQUES THAT UTILIZE ANALOG BITSCAN IN A MEMORY DEVICE	18/234,094
454	THREE-DIMENSIONAL MEMORY DEVICES INCLUDING SELF-ALIGNED CHANNEL CAP STRUCTURES AND METHODS FOR FORMING THE SAME	18/450,095
455	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING INCLINED WORD LINE CONTACT STRIPS AND METHODS OF FORMING THE SAME	18/450,115
456	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING TRENCH BRIDGE STRUCTURES HAVING DIFFERENT VOLUMES AND METHODS OF FORMING THE SAME	18/450,150
457	ENERGY EFFICIENT FAST READ IN A MEMORY DEVICE	18/234,185
458	MEMORY DEVICE WITH MULTIPLE PLANE FUNCTIONALITIES	18/234,993
459	PHOTOLITHOGRAPHY METHOD USING CASTELLATION SHAPED ASSIST FEATURES TO FORM A LINE-AND-SPACE PATTERN AND PHOTOMASK CONTAINING THE ASSIST FEATURES	18/451,206
460	SMART VERIFY ALGORITHM FOR IMPROVING RELIABILITY FOR ULTRA HIGH-PERFORMANCE 3D NAND	18/235,099
461	APPARATUS AND METHODS FOR ERASING FOR NON-VOLATILE MEMORY	18/452,500
462	THERMAL RECOVERY IN MULTI-PROTOCOL DEVICES	18/235,956
463	ERROR HANDLING IN KEY-VALUE SOLID STATE DRIVES	18/235,963
464	FREE SPACE MANAGEMENT IN STORAGE DEVICES HAVING NON-UNIFORM-SIZED MEMORY BLOCKS	18/235,975
465	THREE-DIMENSIONAL MEMORY DEVICE WITH SOURCE CONTACT LAYER HAVING HORIZONTALLY AND VERTICALLY EXTENDING PORTIONS AND METHODS OF FORMING THE SAME	18/452,737
466	BONDED MEMORY MRAM ARRAYS SHARING A COMMON DRIVER CIRCUIT AND METHODS OF MAKING THE SAME	18/453,555
467	ERROR HANDLING IN ASYMMETRIC SUB-BLOCKS	18/237,041
468	METHOD FOR OPTIMIZING LOGICAL-TO-PHYSICAL TABLE UPDATES FOR FIXED GRANULARITY LOGICAL-TO-PHYSICAL TABLES	18/237,301
469	RECLAIM PACKAGE CACHE FOR THERMAL THROTTLING	18/237,096
470	EFFICIENT USAGE OF REDUNDANT COLUMNS IN FLASH MEMORY	18/237,033
471	NON-VOLATILE MEMORY BITMAP FOR GARBAGE COLLECTION	18/454,253
472	STAGED HIGH-DENSITY BACKPLANE FOR ELECTRONIC MODULES	18/237,556
473	THREE-DIMENSIONAL MEMORY DEVICE WITH THROUGH-STACK CONTACT VIA STRUCTURES AND METHOD OF MAKING THE SAME	18/455,988
474	PHY Lanes Disabling For Power Efficiency	18/455,958
475	INTERPOSER FOR TROUBLESHOOTING A BALL GRID ARRAY (BGA) DEVICE AND COUPLING THE BGA DEVICE TO A PRINTED CIRCUIT BOARD WITH LIMITED HEAT EXPOSURE	18/238,952

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476	DYNAMICALLY DETERMINING A RATIO OF MEMORY BLOCKS TO INCLUDE IN A GARBAGE COLLECTION PROCESS	18/456,856
477	UNSINGULATED SEMICONDUCTOR PACKAGE	18/456,906
478	Data Storage Device and Method for Inferring a Read Threshold Using a Time Tag Determination	18/239,302
479	STAIRLESS THREE-DIMENSIONAL MEMORY DEVICE WITH LAYER CONTACT VIA STRUCTURES LOCATED ABOVE SUPPORT PILLAR STRUCTURES AND METHODS OF FORMING THE SAME	18/457,883
480	Training Ensemble Models To Improve Performance In The Presence Of Unreliable Base Classifiers	18/459,320
481	Multi-Layer NFT for HAMR with a Thermal Shunt Connecting the Metal Layers	18/241,164
482	TEMPERATURE CONTROL OF A LASER DIODE BY APPLYING REVERSE BIAS IN A DATA STORAGE DEVICE CONFIGURED FOR HEAT-ASSISTED MAGNETIC RECORDING	18/460,376
483	THREE-DIMENSIONAL MEMORY DEVICE WITH PILLAR SHAPED TRENCH BRIDGE STRUCTURES AND METHODS OF FORMING THE SAME	18/459,938
484	DATA STORAGE DEVICE AND METHOD FOR PREDICTING FUTURE READ THRESHOLDS	18/242,061
485	CREDIT ALLOCATION FOR ENABLING ACCESS TO HARDWARE RESOURCES OF A COMPUTING DEVICE	18/461,089
486	MEMORY TESTING FLOW SET UP WITH COMPUTATIONAL INTELLIGENCE	18/461,237
487	DFL TDMR Middle Shield Throat height control for improved stability	18/243,053
488	HMB random and sequential access coherency approach	18/461,777
489	OPTIMIZED ERRATIC PROGRAM DETECTION PROCESS	18/242,793
490	Resource allocation to avoid command timeouts in a storage device	18/461,939
491	Fairness and consistency in MFND	18/461,779
492	MEMORY DEVICE INCLUDING WORD LINE CONTACT STRIPS AND METHODS OF FORMING THE SAME	18/462,955
493	PROGRAMMING TECHNIQUES TO IMPROVE ERASE STATE UPPER TAILS IN A MEMORY DEVICE	18/243,314
494	CHEMICAL MECHANICAL POLISHING PROCESS USING STEAM FOR POLISHING FLUID DELIVERY AND AN APPARATUS FOR IMPLEMENTING THE SAME	18/462,830
495	BLOCK DATA ENCRYPTION OF NON-VOLATILE MEMORY THROUGH SELECTIVE SELECT GATE ERASE THROUGH CHARGE COUPLED SCHEME	18/463,525
496	MEMORY DIE STACK HAVING A SWITCH FOR SELECTIVELY CONNECTING A MEMORY DIE TO A SUBSTRATE	18/463,805
497	LOCATION-BASED MAINTENANCE OPERATIONS FOR A DATA STORAGE DEVICE	18/463,506
498	Topological Insulator Based Spin Torque Oscillator Reader	18/244,555
499	Multi-Tier Error Correction Codes for DNA Data Storage	18/464,494
500	Cache Writing to Zones to Maximize Write Bandwidth	18/464,503
501	BACK GRINDING TAPE HAVING TABS TO ASSIST IN REMOVING THE BACK GRINDING TAPE FROM A WAFER	18/464,779
502	Non-localized Spin Valve Reader Hybridized with Spin Orbit Torque Layer	18/367,877
503	Non-localized Spin Valve Multi-Free-Layer Reader Hybridized with Spin Orbit Torque Layers	18/367,882
504	APPARATUS AND METHODS FOR BACK-TO-BACK STATE MACHINE CONTROLLER BUS OPERATIONS	18/466,085
505	SEMICONDUCTOR DEVICE FABRICATION METHOD USING A DEPOSITION APPARATUS WITH A CONTOURED WAFER CARRIER RING	18/466,108
506	DC AND SYNCHRONIZED ENERGY ASSISTED PERPENDICULAR MAGNETIC RECORDING (EPMR) DRIVER CIRCUIT FOR HARD DISK DRIVE (HDD)	18/467,045
507	Spin-Orbit Torque SOT Reader with Recessed Spin Hall Effect Layer	18/368,220
508	DATA PATH OSCILLATOR MISMATCH ERROR REDUCTION FOR NON-VOLATILE MEMORY	18/467,005
509	BIT LINE TIMING BASED CELL TRACKING QUICK PASS WRITE FOR PROGRAMMING NON-VOLATILE MEMORY APPARATUSES	18/368,951
510	TOUCHDOWN DETECTION AND WRITE-SPACING SETTING IN MAGNETIC RECORDING HEADS WITH PROTRUDING FEATURES	18/468,448
511	IMPROVING THRESHOLD VOLTAGE BUDGET BY EMPLOYING AN OXIDE-NITRIDE PITCH DEPENDENT THRESHOLD VOLTAGE WINDOW	18/369,028
512	NON-VOLATILE MEMORY WITH EFFICIENT PRECHARGE IN SUB-BLOCK MODE	18/468,349
513	NEIGHBOR PLANE DISTURB (NPD) DETECTION FOR MEMORY DEVICES	18/369,296
514	STAIR-STEP CONFIGURATION FOR A SEMICONDUCTOR DIE OF AN INTEGRATED CIRCUIT	18/468,904
515	Tape Heads Having Shifted Array/Pad Arrangements	18/370,273

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U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
516	POWER IMPROVEMENT FOR MINIMUM SWITCHING FREQUENCY OPERATION	18/471,405
517	WORD LINE ZONE BASED UNSELECT WORD LINE BIAS TO ENABLE SINGLE-SIDE GATE-INDUCED DRAIN LEAKAGE ERASE	18/371,100
518	THREE-DIMENSIONAL MEMORY DEVICE WITH ISOLATION TRENCH FILL STRUCTURE HAVING LATERALLY-UNDULATING SIDEWALLS AND METHOD OF MAKING THE SAME	18/471,896
519	NON-VOLATILE MEMORY WITH SEQUENTIAL READ	18/471,455
520	METHOD FOR HANDLING EXTREME TEMPERATURES IN STORAGE DEVICES	18/372,152
521	MANAGING STREAMS BASED ON PREDICTED HOST COMMANDS	18/473,500
522	SCHEDULING EXECUTION OF COMMANDS IN A DATA STORAGE DEVICE BASED ON COMMAND PARAMETERS	18/473,774
523	CONTROLLING INPUT/OUTPUT PAD DISCHARGE RATE IN STORAGE DEVICES	18/372,777
524	Method and System for handling host commands overlapping with deferred unmap address ranges in storage devices	18/372,759
525	HOST PERFORMANCE BUFFER (HPB) READ PERFORMANCE ACROSS MULTIPLE HPB REGIONS	18/372,805
526	HARD DISK DRIVE SLIDER COATING FOR SUSPENSION MECHANICAL IMPROVEMENT	18/373,034
527	VOICE COIL MOTOR COMPOSITE MAGNET ASSEMBLY INCLUDING LOW-COERCIVITY MAGNETIC MATERIAL	18/373,957
528	TRENCH PATTERNING PROCESS USING MICROCRACKING	18/475,826
529	ENABLING POWER OPTIMIZATION THROUGH DRAM BANK MANAGEMENT IN SOLID STATE DRIVES	18/373,403
530	CAPILLARY FOR A WIRE BONDING MACHINE HAVING A DYNAMICALLY ADJUSTABLE CHAMFER DIAMETER	18/478,358
531	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING LATERALLY UNDULATING ISOLATION TRENCHES AND METHODS OF MAKING THE SAME	18/477,907
532	THREE-DIMENSIONAL MEMORY DEVICES INCLUDING SELF-ALIGNED SOURCE-CHANNEL JUNCTIONS AND METHODS FOR FORMING THE SAME	18/479,457
533	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING PHOSPHORUS-DOPED SILICON OXIDE ION-GETTERING STRUCTURES AND METHODS OF FORMING THE SAME	18/479,432
534	Data Storage Device and Method for Delaying Execution of a Host Write Command to Perform an Internal Memory Operation	18/376,122
535	ALIGNMENT TOOL FOR A SOLDER MACHINE	18/480,724
536	Key-group based Data management in KV SSD	18/480,671
537	NON-VOLATILE MEMORY WITH CURRENT DETECTION CIRCUIT	18/481,786
538	DATA STORAGE DEVICE SORTING ACCESS COMMANDS BASED ON PERFORMANCE AND OFF-TRACK MITIGATION OPTIMIZATION	18/377,666
539	READ FOR MEMORY CELL WITH THRESHOLD SWITCHING SELECTOR	18/482,538
540	Shortened Commands to Reduce Data Transmission	18/377,820
541	Multiple Command Format Interpretation for SSD	18/377,821
542	ARTIFICIAL SELECT GATE CUT FOR NAND	18/482,996
543	Adaptive Tuning of Memory Device Clock Rates Based on Usage Workloads	18/483,488
544	READ IN MULTI-TIER NON-VOLATILE MEMORY	18/483,010
545	DARK LASER HEATING BY POSITIVE PULSE BIASING IN HEAT ASSISTED MAGNETIC RECORDING	18/483,595
546	SUSPENSION LOAD BEAM RAIL-BASED GIMBAL LIMITER	18/378,400
547	Erase Type Detection Mechanism	18/485,050
548	Smart Host Stream Release	18/485,070
549	DATA TRANSFER FOR VEHICLES	18/485,140
550	FLEXIBLE PRINTED CIRCUIT FINGER LAYOUT FOR LOW CROSSTALK	18/379,587
551	INCREASED VCM CURRENT RESOLUTION DURING TRACK FOLLOW TO DECREASE NRRO	18/485,622
552	MAGNETIC RECORDING MEDIUM WITH MAGNESIUM-TITANIUM OXIDE (MTO) LAYER FORMED USING PULSED DIRECT CURRENT SPUTTER DEPOSITION	18/379,410
553	PROACTIVE DATA-VALID WINDOW TRACKING SCHEME FOR HS TM INTERFACE	63/590,046
554	Improved Host DRAM and PCIe bandwidth utilization for DRAM-less devices	18/488,421
555	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING SLOPING WORD LINES FOR STAIRLESS CONTACT AND METHODS OF FORMING THE SAME	18/488,360
556	Write Protect HW Acceleration	18/488,426
557	Bandwidth Averaging In A Stochastic System	18/489,555
558	SSD Optimization Awareness To Atomicity Of Different System Files	18/489,560

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No.	TITLE	Reg. No. / App. No.
559	POLE TIP RECESSION COMPENSATION BY DUAL HEATER RATIO OPTIMIZATION IN A HARD DISK DRIVE	18/490,225
560	Read-protected storage device with sequential logging	18/490,364
561	READ RECOVERY WITH TIME LIMIT IN NONVOLATILE MEMORY	18/490,782
562	METAL LINES LOCATED BETWEEN ETCH STOP LAYERS AND SEPARATED BY AIR GAPS AND METHODS OF FORMING THE SAME	18/491,297
563	SELECTABLE LOW POWER MODE FOR STORAGE DEVICES	18/491,540
564	DEVICES AND METHODS FOR METAL ORGANIC FRAMEWORK (MOF) BASED OXYGEN REPLENISHMENT IN DATA STORAGE DEVICES	18/492,559
565	SUPPRESSION OF PEAK ICC DURING BLOCK SELECTION IN NON-VOLATILE MEMORIES	18/492,545
566	MICRO SOLDER JOINT AND STENCIL APERTURE DESIGN	18/493,379
567	THREE-DIMENSIONAL MEMORY DEVICE WITH DIFFERENT WIDTH SUPPORT PILLAR STRUCTURES AND METHODS OF MAKING THE SAME	18/493,036
568	MEDIA UNDERLAYER STRUCTURE FOR HEAT-ASSISTED MAGNETIC RECORDING AND MEDIA FABRICATION METHODS THEREFOR	18/383,638
569	Sloped Interconnector for Stacked Die Package	11,756,932