

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

Assignment ID: PAT144755

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Patent Collateral Agreement (DDTL)
SEQUENCE:	1

CONVEYING PARTY DATA

Name	Execution Date
Western Digital Technologies, Inc.	02/12/2024

RECEIVING PARTY DATA

Company Name:	JPMorgan Chase Bank, N.A., as the Agent
Street Address:	10 South Dearborn
City:	Chicago
State/Country:	ILLINOIS
Postal Code:	60603

PROPERTY NUMBERS Total: 225

Property Type	Number
Application Number:	18382860
Application Number:	18493043
Application Number:	18493527
Application Number:	18383813
Application Number:	18383836
Application Number:	18383730
Application Number:	18383854
Application Number:	18383820
Application Number:	18384051
Application Number:	18384160
Application Number:	18384204
Application Number:	18495534
Application Number:	18494852
Application Number:	18495552
Application Number:	18496203
Application Number:	18385756
Application Number:	18499024
Application Number:	18499069
Application Number:	18499363

PATENT

Property Type	Number
Application Number:	18499370
Application Number:	18386210
Application Number:	18386191
Application Number:	18499325
Application Number:	18499863
Application Number:	18499849
Application Number:	18499797
Application Number:	18500188
Application Number:	18386326
Application Number:	18501490
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Application Number:	18501619
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Application Number:	18504408
Application Number:	18504413
Application Number:	18388513
Application Number:	18505292
Application Number:	18506620
Application Number:	18506281
Application Number:	18506155
Application Number:	18507026
Application Number:	18389155
Application Number:	18508638
Application Number:	18389284
Application Number:	18389332
Application Number:	18508554
Application Number:	18389439
Application Number:	18509010
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Application Number:	18509051
Application Number:	18510070
Application Number:	18509523

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Application Number:	18509708
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Application Number:	18528718
Application Number:	18528736
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Property Type	Number
Application Number:	18532404
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Property Type	Number
Application Number:	18395602
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Application Number:	12416893
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Application Number:	14018172

Property Type	Number
Application Number:	14878635
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Application Number:	10397378
Application Number:	10704611
Application Number:	10981657
Application Number:	11102814
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Application Number:	13336088
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Application Number:	14243570
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Application Number:	12101065
Application Number:	12348005
Application Number:	12853924
Application Number:	13204387
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Application Number:	14135467
Application Number:	14135407

Property Type	Number
Application Number:	14331033
Application Number:	14494807
Application Number:	13170955
Application Number:	12706519
Application Number:	14022779
Application Number:	15491915
Application Number:	15427706
Application Number:	10772855
Application Number:	11537404
Application Number:	11536974
Application Number:	11196826
Application Number:	14815886
Application Number:	14815891
Application Number:	11267534
Application Number:	12183006
Application Number:	13926824

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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NAME OF SUBMITTER:	Michael Violet
SIGNATURE:	Michael Violet
DATE SIGNED:	02/22/2024

Total Attachments: 10

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Patent Collateral Agreement

This February 12, 2024, Western Digital Technologies, Inc. (“*Debtor*”) with its principal place of business and mailing address at 5601 Great Oaks Parkway, San Jose, CA 95119, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the “*Agent*”), with its mailing address at 10 South Dearborn, Chicago, IL 60603, acting as collateral agent hereunder for the Secured Parties as defined in the Security Agreement, dated as of June 20, 2023, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the “*Security Agreement*”) for the benefit of the Secured Parties, a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, “*Patent Collateral*”):

(i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on Schedule A hereto (the “*Patents*”); and

(ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

WESTERN DIGITAL TECHNOLOGIES, INC.,
as Debtor

By: DocuSigned by:
Cynthia Tregillis
9A5264DA2BF04C5...
Name: Cynthia Tregillis
Title: Senior Vice President,
Chief Legal Officer and Secretary

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By: *Caitlin Stewart*
Name: Caitlin Stewart
Title: Executive Director

**SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS**

No.	TITLE	Reg. No. / App. No.
1	Adaptive wear-leveling of sub-blocks in non-volatile memory	18/382,860
2	Namespace Management Using Mastership In Multi-Host Storage Systems	18/493,043
3	SEMICONDUCTOR WAFER THINNED BY CRACK PROPAGATION	18/493,527
4	PARTIAL SPEED CHANGES TO IMPROVE IN-ORDER TRANSFER	18/383,813
5	HARD DISK DRIVE INTERPOSE SWAGE	18/383,836
6	METHOD FOR ISOLATING FAULTY NAND TEMPERATURE SENSOR	18/383,730
7	TIME BOUND PARTIAL FORMAT OPERATION IN A STORAGE DEVICE	18/383,854
8	SCHEME TO FETCH OPTIMAL READ PARAMETERS BY SKIPPING INVALID WORDLINES	18/383,820
9	DATA STORAGE DEVICE WITH SYMMETRIC SPLIT BURST SERVO PATTERN	18/384,051
10	Notched Head Design For Tape Applications	18/384,160
11	WORD LINE BIAS DURING STRIPE ERASE IN A MEMORY DEVICE	18/384,204
12	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING DUMMY VIA CAVITIES AND METHOD FOR MAKING SAME	18/495,534
13	INTEGRATED CHARGE PUMP TESTING CIRCUITS	18/494,852
14	PERIPHERAL CIRCUIT WITH SEMICONDUCTOR PILLAR CONTAINING LOCAL INTERCONNECTS AND METHODS FOR FORMING THE SAME	18/495,552
15	Rear Soft Bias Dual Free Layer Sensor With Patterned Decoupling Layer	18/496,203
16	3-Band Magnetic Recording Tape and Tape Drive	18/385,756
17	NUCLEIC ACID SEQUENCING USING NANOPORES	18/499,024
18	METHODS AND SYSTEMS FOR NUCLEIC ACID SEQUENCING USING NANOPORES	18/499,069
19	Preprocessing for Correcting Insertions and Deletions in DNA Data Storage	18/499,363
20	Nested Error Correction Codes for DNA Data Storage	18/499,370
21	DATA PROCESSING METHODS AND APPARATUS FOR USE WITH FEATURE MAPS IN SPARSE CONVOLUTIONAL NEURAL NETWORKS	18/386,210
22	DATA PROCESSING METHODS AND APPARATUS FOR USE WITH FEATURE MAPS IN SPARSE CONVOLUTIONAL NEURAL NETWORKS	18/386,191
23	CROSS-POINT OVONIC MEMORY DEVICE HAVING DIFFERENT SIZE ELECTRODES AND METHOD OF MAKING THE SAME	18/499,325
24	Multi-Functional Universal Serial Bus (USB) Drive	18/499,863
25	Efficient Address Translation Cache Lookup Operations	18/499,849
26	SUB-BLOCK SEPARATION IN NAND MEMORY THROUGH WORD LINE BASED SELECTORS	18/499,797
27	DUAL SPINDLE MOTORS AND DUAL SPINDLE MOTOR CONTROL FOR DATA STORAGE	18/500,188
28	DATA STORAGE DEVICE WITH EMBEDDED MODE HOP PREDICTOR PATTERNS	18/386,326
29	ACCESSING SHARED PARTITIONS ON A STORAGE DRIVE OF A REMOTE DEVICE	18/501,490
30	MAGNETIC RECORDING MEDIA WITH SACRIFICIAL LAYER AND CORRESPONDING ETCHING PROCESSES TO MINIMIZE HEAD TO MEDIA SPACING	18/386,936
31	Host Queues Recovery in Exception Flows	18/386,797
32	ECO-FRIENDLY PRINTED CIRCUIT BOARD FOR HIGH TEMPERATURE AND LOW TEMPERATURE APPLICATIONS	18/501,619
33	Deep Neural Network Device Based on Dual Spin Orbit Torque (SOT) Devices	63/547,479
34	Burst Awareness Scheduler Over Host Interface	18/502,694
35	Speculative address translation service requests	18/502,538
36	Data Storage Device and Method for Multiple Meta Die Balancing	18/387,162
37	HYBRID ADDRESS TRANSLATION CACHE USING DRAM	18/503,656
38	Data Routing In Networked SSDs	18/503,649
39	CREATING A SOLDER BARRIER BY CHANGING A MATERIAL PROPERTY OF A TRACE ON A PRINTED CIRCUIT BOARD	18/504,408
40	DETERMINING A BACK DRILLING DEPTH FOR A PRINTED CIRCUIT BOARD USING A PRINTED CIRCUIT BOARD TEST COUPON	18/504,413
41	Method and device for data storage device user authentication	18/388,513
42	Optimizations for Payload Fetching in NVMe Commands	18/505,292
43	DIFFERENTIAL SENSE OF EMBEDDED CONTACT SENSOR (ECS) AND NEAR-FIELD TEMPERATURE SENSOR (NTS) UTILIZING CHOPPING AMPLIFIER	18/506,620
44	Peer-To-Peer Communication Using Drain Buffers In Multi-Function Device	18/506,281
45	NONVOLATILE MEMORY WITH DISTRIBUTED XOR PROTECTION	18/506,155
46	NON-VOLATILE MEMORY WITH THREE DIMENSIONAL STACKED WORD LINE SWITCHES	18/507,026

**SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS**

No.	TITLE	Reg. No. / App. No.
47	STUCK BITS ENCODING AND DECODING ON A STORAGE DEVICE	18/389,155
48	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING LATERALLY UNDULATING ISOLATION TRENCHES AND METHODS OF MAKING THE SAME	18/508,638
49	REDUCING READ DISTURB IN A SEMI-CIRCULAR MEMORY CELL OF A MEMORY DEVICE	18/389,284
50	STATE DEPENDENT SUSPEND-RESUME-GO FOR PERFORMANCE IMPROVEMENT IN A MEMORY DEVICE	18/389,332
51	EVEN/ODD WORD LINE DRIVING IN 3D MEMORY	18/508,554
52	POWER SAVING DURING OPEN BLOCK READ WITH LARGE BLOCK OPENNESS	18/389,439
53	BONDING STRUCTURES FOR HIGH-DENSITY METAL-TO-METAL BONDING AND METHODS FOR FORMING THE SAME	18/509,010
54	BONDING STRUCTURES FOR HIGH-DENSITY METAL-TO-METAL BONDING AND METHODS FOR FORMING THE SAME	18/509,035
55	BONDING STRUCTURES FOR HIGH-DENSITY METAL-TO-METAL BONDING AND METHODS FOR FORMING THE SAME	18/509,051
56	DYNAMIC PROGRAM PERFORMANCE MODULATION IN A MEMORY DEVICE	18/510,070
57	ERASE VERIFY MODE TO REDUCE POWER CONSUMPTION IN ERASE OPERATION OF NON-VOLATILE MEMORY APPARATUS	18/509,523
58	VARIABLE FOGGY VERIFY LEVELS FOR SELECTED CHECKPOINT STATES FOR NON-VOLATILE MEMORY APPARATUSES	18/509,708
59	DELAYED SELECT GATE RAMP-UP FOR PEAK READ CURRENT CONSUMPTION REDUCTION FOR NON-VOLATILE MEMORY APPARATUS	18/509,848
60	Magnetic Recording Head with A Cross-Track Current Flow In A Low Resistance Path	18/511,235
61	SENSE TIME SEPARATION IN FOGGY-FINE PROGRAM TO IMPROVE OPTIMAL VT WIDTH	18/510,857
62	ON-CHIP QLC AND TLC MIX OPERATION	18/511,333
63	ACHIEVING DIFFERENT HIGH VOLTAGES ON INDIVIDUAL BITLINES OF A MEMORY DEVICE	18/510,978
64	METHOD FOR DETECTING AND RECOVERING AN INOPERABLE DRIVE	18/511,724
65	STORAGE SYSTEMS FOR LARGE LANGUAGE MODEL FINE-TUNING	18/513,600
66	Proactive Correction Of Potential Transmission Errors In A Storage Device	18/513,949
67	Cache Write Overlap Handling	18/515,932
68	DRAM-less SSD with Command Draining	18/516,219
69	TLC Data Programming With Hybrid Parity	18/515,758
70	DATA STORAGE DEVICE WITH FLEXIBLE LOGICAL TRACKS AND RADIUS-INDEPENDENT DATA RATE	18/516,164
71	ENERGY-ASSISTED MAGNETIC RECORDING DATA STORAGE DEVICE WITH OPPORTUNISTIC BOOSTED LASER PRE-BIASING	18/516,146
72	DATA STORAGE DEVICE WITH SELF-LEARNING OSCILLATION DETECTOR	18/516,481
73	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING CRACK-RESISTANT BACKSIDE PASSIVATION STRUCTURE AND METHODS OF FORMING THE SAME	18/516,064
74	THREE-DIMENSIONAL MEMORY DEVICE INCLUDING CRACK-RESISTANT BACKSIDE PASSIVATION STRUCTURE AND METHODS OF FORMING THE SAME	18/516,170
75	ENHANCED PRYING STRUCTURE FOR ELECTRONIC DEVICE	18/516,012
76	TIME TAG WORD LINE SHIFT TO REDUCE FAILED BIT COUNT SPIKES FOR EDGE WORD LINES	18/517,579
77	NON-VOLATILE MEMORY WITH OPERATION ADJUSTMENT BASED ON OPEN BLOCK RATIO AND CYCLING	18/519,962
78	SOT MRAM INCLUDING MTJ AND SELECTOR LOCATED ON OPPOSITE SIDES OF SOT LAYER AND METHOD OF MAKING THE SAME	18/520,299
79	SOT MRAM INCLUDING MTJ AND SELECTOR LOCATED ON OPPOSITE SIDES OF SOT LAYER AND METHOD OF MAKING THE SAME	18/520,401
80	SMART ERASE INHIBIT	18/519,426
81	PROCESSING CORE INCLUDING INTEGRATED HIGH CAPACITY HIGH BANDWIDTH STORAGE MEMORY	18/519,210
82	NVMe Completion And Interrupt	18/522,514
83	GENERATING AND USING A STATE TRANSITION MATRIX FOR DECODING DATA IN A DNA-BASED STORAGE SYSTEM	18/523,202
84	THREE-DIMENSIONAL MEMORY DEVICE WITH VARIABLE WORD LINE VIA CONTACT DENSITY AS FUNCTION OF CONTACT DEPTH AND METHODS OF FORMING THE SAME	18/523,129
85	MEMORY DIE WITH ON-CHIP BINARY VECTOR DATABASE SEARCH	18/526,698

**SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS**

No.	TITLE	Reg. No. / App. No.
86	MEMORY DIE WITH ON-CHIP BINARY VECTOR DATABASE SEARCH	18/526,821
87	DYNAMIC TRACK PITCH IN SHINGLED MAGNETIC RECORDING HARD DISK DRIVE	18/528,686
88	SECTOR SLIDING IN SHINGLED MAGNETIC RECORDING HARD DISK DRIVE	18/528,718
89	DETERMINISTIC BANDWIDTH FOR A DATA STORAGE DEVICE	18/528,736
90	DNA STORAGE ERROR CORRECTION CODE ARCHITECTURE FOR OPTIMIZED DECODING	18/528,771
91	Data Storage Device Configuration Using Mutual Information	18/531,483
92	Modulation Code and ECC Rate Optimization Using Symbol Context Mutual Information	18/531,491
93	BONDING STRUCTURES FOR HIGH-DENSITY METAL-TO-METAL BONDING AND METHODS FOR FORMING THE SAME	18/530,953
94	DNA DATA STORAGE DEVICE WITH VARIABLE RELIABILITY TIERS	18/531,675
95	THREE-DIMENSIONAL MEMORY DEVICE WITH THROUGH-STACK CONTACT VIA STRUCTURES AND METHOD OF MAKING THE SAME	18/532,221
96	Channel Circuit with Zero Force Equalizer	18/532,404
97	APPARATUS AND METHODS FOR READ RETRY WITH CONDITIONAL DATA REFRESH	18/533,110
98	DFL Reader Signal Sidebump Imbalance Reduction	18/533,533
99	QUALITY OF SERVICE (QOS) OPTIMIZED OPEN BLOCK CLOSURE	18/533,440
100	OPTIMIZED HANDLING OF HIGH CURRENT CONSUMPTION DURING AN OPEN BLOCK READ	18/533,508
101	EFFICIENT ASSEMBLY FOR ELECTROLYTIC CAPACITORS ON SOLID STATE DRIVES	18/534,409
102	METHOD FOR OPTIMIZING INTERFACE TRAINING ON A STORAGE DEVICE	18/533,565
103	Minimizing redundancy for stuck bit coding	18/533,655
104	FAST INITIALIZATION OF MEDIA AFTER LOGICAL BLOCK ADDRESS (LBA) REMAPPING OPERATION	18/535,489
105	LUBRICANTS AND METHODS TO DETERMINE DEWETTING THICKNESS THEREOF	18/538,014
106	MANAGEMENT AND STORAGE OF NEURAL NETWORK WEIGHTS	18/538,890
107	Magnetic Recording Devices Having External Alternating Current Sources	18/540,472
108	SSD AUXILIARY BATTERY POWER FOR HANDLING UNGRACEFUL SHUTDOWN WITH HOST	18/542,437
109	LOGICAL BLOCK FORMATION BASED ON BLOCK ERASE LOOPS	18/541,892
110	FLEXIBLE SIZED SUPER BLOCK FOR OPTIMIZED PERFORMANCE AND ENDURANCE	18/541,811
111	SECURE PEER-TO-PEER FILE SHARING USING DISTRIBUTED OWNERSHIP DATA	18/543,545
112	PEER-TO-PEER FILE SHARING USING CONSISTENT HASHING FOR DISTRIBUTING DATA AMONG STORAGE NODES	18/543,569
113	Hard Disk Drive Disk Media Curvature Mitigation	18/544,189
114	ALTERNATING-BIAS SIGNAL RESISTANCE DETECTION FOR RESISTIVE TEMPERATURE DETECTORS IN DISK DRIVES	18/545,028
115	Magnetic Sensor Half-Bridge Based on Inverse Spin Hall Effect with Reduced Thermal Drift	18/545,847
116	HYBRID THERMAL INTERFACE MATERIAL WITH EMBEDDED METAL LAYER	18/545,601
117	MULTI-STAGE DECODER WITH ADAPTIVE LEARNING	18/545,831
118	Removable Memory Card with Efficient Card Lock Mechanism, XY Ratios, Anti-Reverse Insertion Feature, Pullout Feature, and Pads Layout	18/545,527
119	HIGH SPEED RECEIVER CIRCUITRY	18/390,996
120	IMPROVED BITSCAN TECHNIQUES IN A MEMORY DEVICE	18/389,982
121	APPARATUS AND METHODS FOR MANAGING SELECTOR DEVICE THRESHOLD VOLTAGE DRIFT	18/389,960
122	APPARATUS AND METHODS FOR MANAGING SELECTOR DEVICE THRESHOLD VOLTAGE DRIFT	18/389,980
123	APPARATUS AND METHODS FOR MANAGING SELECTOR DEVICE THRESHOLD VOLTAGE DRIFT	18/389,987
124	ENHANCED BIT ERROR RATE ESTIMATION SCAN PROCESS	18/390,296
125	DYNAMIC BIT LINE VOLTAGE DURING PROGRAM VERIFY TO PROVIDE MORE THRESHOLD VOLTAGE BUDGET	18/390,824
126	WORD LINE SWITCH GATE VOLTAGE AND WELL VOLTAGE SEPARATION	18/391,560
127	DYNAMIC FLASH INTERFACE MODULE (FIM) OPTIMIZATION	18/390,325
128	Spin Orbit Torque (SOT) Device Having a Topological Insulator Layer and a Diffusion Barrier Layer	18/392,230
129	Current Monitoring in a Memory Device to Improve Short Detection	18/393,067
130	OPEN BLOCK DETECTION USING CURRENT CONSUMPTION PEAK DURING FOURTH TIME PERIOD OF READ OPERATION AND METHOD OF LOWERING CURRENT CONSUMPTION FOR NON-VOLATILE MEMORY APPARATUS	18/392,585
131	Smart Reduced-Verify Algorithm for Non-Volatile Memory Apparatuses	18/392,904
132	ADAPTABLE ELECTROSTATIC DISCHARGE CLAMP TRIGGER CIRCUIT	18/391,792
133	NON-VOLATILE MEMORY WITH LEAK TESTS	18/393,557

**SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS**

No.	TITLE	Reg. No. / App. No.
134	Head Velocity Derating for Data Storage Devices Including Disk Media	18/395,602
135	Three-Dimensional Memory Device Containing Peripheral Circuit with Fin Field Effect Transistors and Method of Making the Same	18/396,150
136	Magnetic Heads Having Low Magnetic Coercivity (HC) and High Saturated Magnetic Flux Density (BS) in Ferromagnetic (FM) Layer(s) or Shield(s) With Minimized Saturation	18/397,007
137	Magnetic Heads Having Low Magnetic Coercivity (HC) and High Saturated Magnetic Flux Density (BS) in Ferromagnetic (FM) Layer(s) or Shield(s) With Minimized Saturation	18/397,016
138	Data Storage Device with Efficient Decoder Pool and Method for On-the-Fly Decoder Initialization	18/397,133
139	POSITIVE LASER BIAS ELECTRICAL CONTROL ARCHITECTURE FOR DARK LASER HEATING IN HEAT ASSISTED MAGNETIC RECORDING	18/402,926
140	Tape head module having a congruent extension and method for mass producing same	18/404,216
141	NON-VOLATILE MEMORY WITH ENHANCED EARLY PROGRAM TERMINATION MODE FOR NEIGHBOR PLANE DISTURB	18/405,156
142	LOW NOISE AMPLIFIERS WITH SHIELDS FOR NANOPORE APPLICATIONS	18/406,202
143	HYBRID MEMORY MANAGEMENT OF NON-VOLATILE MEMORY (NVM) DEVICES FOR USE WITH RECURRENT NEURAL NETWORKS	18/406,897
144	Just-In-Time Low Capacity DRAM Memory Allocation	18/406,586
145	Magnetic Recording Head With Assisting Electric Current In Trailing Shield	18/408,014
146	Nitrogen Doped Oxides For Lower Bandgap	18/407,553
147	Dopants to Decrease BiSbX's and YBiPt's Bandgap for Optimal Current-In-Plane (CIP) Conductivity	63/619,447
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149	DATA STORAGE DEVICE EXECUTING HOST ACCESS COMMANDS IN A MANNER TO OPTIMIZE PERFORMANCE AND REDUCE ENERGY COSTS	18/410,679
150	VARYING SUSPENSION ARM LENGTH FOR MAGNETIC STORAGE DEVICE	18/410,727
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163	THREE DIMENSIONAL NAND MULTIPLY AND ACCUMULATE WITH DYNAMIC INPUTS	18/417,239
164	A Multiple Function Nonvolatile Memory express (NVMe) device (MFND) Performance Improvement By Over Reading	18/419,013
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166	CABLING FOR RACK-MOUNT DEVICES	11/670,309
167	PCI EXPRESS LOAD SHARING NETWORK INTERFACE CONTROLLER CLUSTER	12/265,698
168	HOT SWAPPABLE COMPUTER CARD CARRIER	12/416,895
169	HOT SWAPPABLE COMPUTER CARD CARRIER	12/416,898
170	Storage Device Failover	14/231,051
171	Virtual Channel For Data Transfers Between Devices	14/018,172
172	SYSTEMS AND METHODS FOR STORAGE ERROR MANAGEMENT	14/878,635

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174	APPARATUS, SYSTEM, AND METHOD FOR DATA STORAGE USING PROGRESSIVE RAID	11/952,115
175	APPARATUS, SYSTEM, AND METHOD FOR A FRONT-END, DISTRIBUTED RAID	11/952,116
176	APPARATUS, SYSTEM, AND METHOD FOR A MODULAR BLADE	11/952,119
177	APPARATUS, SYSTEM, AND METHOD FOR A DEVICE SHARED BETWEEN MULTIPLE INDEPENDENT HOSTS	11/952,121
178	Apparatus and Method for Securing data on a Portable Storage Device	10/304,772
179	PERSONAL PORTABLE STORAGE	10/398,647
180	Robust Self-Maintaining File System	10/397,378
181	Method and System for Maintaining Backup of Portable Storage Devices	10/704,611
182	Unified Local-Remote Logical Volume	10/981,657
183	Adaptive Booting from Mass Storage Device	11/102,814
184	Signaling to a peripheral via irregular read operations	11/356,983
185	Device and method for monitoring, rating and/or tuning to an audio content channel	13/336,088
186	Apparatus, Methods and Computer Code for Handling an Impending Decoupling between a Transient Peripheral Device and a Host Device	13/204,586
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210	Firmware Reversion Trigger and Control	14/331,033
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215	Shared Data Storage System with High Availability and Hot Plugging	15/491,915
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222	Systems and Methods for a Mass Data Storage System Having a File-Based Interface to a Host and a Non-File-Based Interface to Secondary Storage	14/815,891
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