PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI631441

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Security Agreement (Supplemental)

CONVEYING PARTY DATA

Name	Execution Date
Sandisk Technologies, Inc.	10/30/2024

RECEIVING PARTY DATA

Company Name:	JPMorgan Chase Bank, N.A., as Collateral Agent
Street Address:	10 S. Dearborn L2
City:	Chicago
State/Country:	ILLINOIS
Postal Code:	60603

PROPERTY NUMBERS Total: 190

Property Type	Number
Patent Number:	12121896
Patent Number:	12014802
Patent Number:	12006539
Patent Number:	11946894
Patent Number:	11940404
Patent Number:	11932904
Patent Number:	11892445
Patent Number:	11846564
Patent Number:	11837330
Patent Number:	11747329
Patent Number:	11738336
Patent Number:	11609208
Patent Number:	11579217
Patent Number:	11327073
Patent Number:	11208682
Patent Number:	11112468
Patent Number:	10545678
Patent Number:	10474396
Patent Number:	9959216
Patent Number:	9946607

Property Type	Number
Patent Number:	9794341
Patent Number:	9766992
Patent Number:	9755141
Patent Number:	9703636
Patent Number:	9582058
Patent Number:	9367353
Patent Number:	9280429
Patent Number:	9244785
Patent Number:	9075557
Patent Number:	8996851
Patent Number:	8954385
Patent Number:	8782389
Patent Number:	8503468
Patent Number:	8270830
Patent Number:	8199511
Patent Number:	8174835
Patent Number:	8148962
Patent Number:	7887358
Patent Number:	7634585
Patent Number:	7452236
Patent Number:	7302534
Patent Number:	7136973
Application Number:	18888896
Application Number:	18823094
Application Number:	18823112
Application Number:	18824608
Application Number:	18825487
Application Number:	18811118
Application Number:	18893461
Application Number:	18800681
Application Number:	18882360
Application Number:	18882390
Application Number:	18882410
Application Number:	18904344
Application Number:	18826339
Application Number:	18826542
Application Number:	18887054
Application Number:	18825432

Property Type	Number
Application Number:	18830759
Application Number:	18917095
Application Number:	18905088
Application Number:	18897326
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Application Number:	18894550
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Application Number:	18894270
Application Number:	18797072
Application Number:	18887730
Application Number:	18886576
Application Number:	18818259
Application Number:	18805352
Application Number:	18816377
Application Number:	18806220
Application Number:	18803091
Application Number:	18824214
Application Number:	18813213
Application Number:	18917638
Application Number:	18917675
Application Number:	18882112
Application Number:	18828504
Application Number:	18909661
Application Number:	18827036
Application Number:	18883650
Application Number:	18827981
Application Number:	18824083
Application Number:	18808409
Application Number:	18903283
Application Number:	18890025
Application Number:	18886384
Application Number:	18886398
Application Number:	18896420
Application Number:	18905292
Application Number:	18897505
Application Number:	18897573
Application Number:	18897684
Application Number:	18891932

Property Type	Number
Application Number:	18921761
Application Number:	18883214
Application Number:	18883219
Application Number:	18883221
Application Number:	18825864
Application Number:	18897714
Application Number:	18811536
Application Number:	18892779
Application Number:	18830257
Application Number:	18886461
Application Number:	18902041
Application Number:	18891177
Application Number:	18897891
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Application Number:	18804492
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Application Number:	18817040
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Application Number:	18829622
Application Number:	18829608
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Application Number:	18916496
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Application Number:	18894152
Application Number:	18914512
Application Number:	18813426
Application Number:	18824397
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Application Number:	18916686
Application Number:	18825264
Application Number:	18825319
Application Number:	18897295
Application Number:	18904260

Property Type	Number
Application Number:	18904223
Application Number:	18914582
Application Number:	18904530
Application Number:	18922262
Application Number:	18914526
Application Number:	18914949
Application Number:	18919573
Application Number:	62833130
Application Number:	17602319
Application Number:	62987831
Application Number:	17905724
Application Number:	63013236
Application Number:	17996360
Application Number:	62705639
Application Number:	18004402
Application Number:	18325942
Application Number:	18165089
Application Number:	17661578
Application Number:	17464533
Application Number:	16908581
Application Number:	18775668
Application Number:	18738801
Application Number:	17643401
Application Number:	17649249
Application Number:	18590557
Application Number:	18406202
Application Number:	17659688
Application Number:	18740042
Application Number:	18670512
Application Number:	18760409
Application Number:	18352398
Application Number:	18364506
Application Number:	18479457
Application Number:	18646016
Application Number:	18499024
Application Number:	18499069
Application Number:	18389439
Application Number:	18649071

Property Type	Number
Application Number:	18442580
Application Number:	18679470
Application Number:	18436345
Application Number:	18437794
Application Number:	18443975
Application Number:	18442693
Application Number:	18663824
Application Number:	18443992
Application Number:	18443933
Application Number:	18442709
Application Number:	18603582
Application Number:	18442684
Application Number:	18651922
Application Number:	18588236
Application Number:	18738634
Application Number:	18631140
Application Number:	18631149
Application Number:	18443663

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 8007130755
Email: Michael.Violet@wolterskluwer.com
Correspondent Name: Michael Violet
Address Line 1: 4400 Easton Commons Way
Address Line 2: Suite 125
Address Line 4: Columbus, OHIO 43219

NAME OF SUBMITTER:	Michael Violet
SIGNATURE:	Michael Violet
DATE SIGNED:	11/14/2024

Total Attachments: 9
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Patent Collateral Agreement

This October 30, 2024, Sandisk Technologies, Inc. ("*Debtor*") with its principal place of business and mailing address at 951 SanDisk Dr., Milpitas, CA 95035, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the "*Agent*"), with its mailing address at 10 South Dearborn, Chicago, IL 60603, acting as collateral agent hereunder for the Secured Parties as defined in the Security Agreement (and, to the extent provided in Section 15 of the Security Agreement, the 2029/2032 Notes Secured Parties), dated as of June 20, 2023, among Agent and the debtors party thereto, as supplemented by that certain Assumption and Supplemental Security Agreement, dated as of April 26, 2024, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the "*Security Agreement*") for the benefit of the Secured Parties (and, to the extent provided in Section 15 of the Security Agreement, the 2029/2032 Notes Secured Parties), a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, "*Patent Collateral*"):

(i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on Schedule A hereto (the "*Patents*"); and

(ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

SANDISK TECHNOLOGIES, INC.,
as Debtor

DocuSigned by:
By: Cynthia Tregillis
9A5264DA2BFD423...
Name: Cynthia Tregillis
Title: Senior Vice President,
Chief Legal Officer and Secretary

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By: _____

Name: Timothy Lee
Title: Executive Director

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
1	NUCLEIC ACID SEQUENCING BY SYNTHESIS USING MAGNETIC SENSOR ARRAYS	12,121,896
2	DEVICES AND METHODS FOR LOCATING A SAMPLE READ IN A REFERENCE GENOME	12,014,802
3	REFERENCE-GUIDED GENOME SEQUENCING	12,006,539
4	LOW NOISE AMPLIFIERS WITH FEEDBACK FOR NANOPORE APPLICATIONS	11,946,894
5	LOW NOISE AMPLIFIERS WITH SHIELDS FOR NANOPORE APPLICATIONS	11,940,404
6	ENHANCED OPTICAL DETECTION FOR NUCLEIC ACID SEQUENCING USING THERMALLY-DEPENDENT FLUOROPHORE TAGS	11,932,904
7	DEVICES, SYSTEMS, AND METHODS OF USING SMART FLUIDS TO CONTROL TRANSLOCATION SPEED THROUGH A NANOPORE	11,892,445
8	OPTICAL SYSTEMS AND METHODS FOR LOCATING QUERY SYMBOLS IN A REFERENCE SEQUENCE	11,846,564
9	REFERENCE-GUIDED GENOME SEQUENCING	11,837,330
10	MAGNETIC GRADIENT CONCENTRATOR/RELUCTANCE DETECTOR FOR MOLECULE DETECTION	11,747,329
11	SPIN TORQUE OSCILLATOR (STO) SENSORS USED IN NUCLEIC ACID SEQUENCING ARRAYS AND DETECTION SCHEMES FOR NUCLEIC ACID SEQUENCING	11,738,336
12	DEVICES AND METHODS FOR MOLECULE DETECTION BASED ON THERMAL STABILITIES OF MAGNETIC NANOPARTICLES	11,609,208
13	DEVICES AND METHODS FOR FREQUENCY- AND PHASE-BASED DETECTION OF MAGNETICALLY-LABELED MOLECULES USING SPIN TORQUE OSCILLATOR (STO) SENSORS	11,579,217
14	THERMAL SENSOR ARRAY FOR MOLECULE DETECTION AND RELATED DETECTION SCHEMES	11,327,073
15	ENHANCED OPTICAL DETECTION FOR NUCLEIC ACID SEQUENCING USING THERMALLY-DEPENDENT FLUOROPHORE TAGS	11,208,682
16	Magnetoresistive Sensor Array for Molecule Detection and Related Detection Schemes	11,112,468
17	Shared Data Storage System with High Availability and Hot Plugging	10,545,678
18	SYSTEM AND METHOD FOR MANAGING MULTIPLE FILE SYSTEMS IN A MEMORY	10,474,396
19	Generating and Using an Enhanced Initialization Vector	9,959,216
20	SYSTEMS AND METHODS FOR STORAGE ERROR MANAGEMENT	9,946,607
21	Data Storage Verification in Distributed Storage System	9,794,341
22	Storage Device Failover	9,766,992
23	A Method for Fabricating MRAM Bits on a Tight Pitch	9,755,141
24	Firmware Reversion Trigger and Control	9,703,636
25	Power Inrush Management of Storage Devices	9,582,058
26	STORAGE CONTROL SYSTEM WITH POWER THROTTLING MECHANISM AND METHOD OF OPERATION THEREOF	9,367,353
27	Power Fail Latching Based on Monitoring Multiple Power Supply Voltages in a Storage Device	9,280,429
28	Simulated Power Failure and Data Hardening	9,244,785
29	Virtual Channel For Data Transfers Between Devices	9,075,557
30	Host Device and Method for Securely Booting the Host Device with Operating System Code Loaded From a Storage Device	8,996,851
31	Efficient Recovery of Transactional Data Stores	8,954,385
32	Storage Device and Method for Updating a Shadow Master Boot Record	8,782,389
33	PCI EXPRESS LOAD SHARING NETWORK INTERFACE CONTROLLER CLUSTER	8,503,468
34	OPTICAL NETWORK FOR CLUSTER COMPUTING	8,270,830
35	HOT SWAPPABLE COMPUTER CARD CARRIER	8,199,511
36	HOT SWAPPABLE COMPUTER CARD CARRIER	8,174,835
37	Transient Load Voltage Regulator	8,148,962
38	CONNECTOR CLAMP	7,887,358
39	In-line cache using nonvolatile memory between host and disk device	7,634,585
40	CABLING FOR RACK-MOUNT DEVICES	7,452,236
41	Dual Media Storage Device	7,302,534
42	Dual Media Storage Device	7,136,973
43	NUCLEIC ACID SEQUENCING BY SYNTHESIS USING MAGNETIC SENSOR ARRAYS	18/888,896
44	Configurable Arithmetic HW Accelerator	18/823,094
45	Data Storage With Real Time Dynamic Clock Frequency Control	18/823,112
46	BIPOLAR DECODERS FOR NONVOLATILE MEMORY WITH SPIKE ATTENUATION FOR THRESHOLD SELECTOR SWITCHES	18/824,608
47	ADDRESS PATH ROUTING REDUCTION STRATEGY FOR NONVOLATILE MEMORY DECODERS	18/825,487

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
48	HIGH BANDWIDTH FLASH MEMORY CONTAINING A STACK OF BONDED LOGIC AND MEMORY DIE ASSEMBLIES AND METHODS FOR FORMING THE SAME	18/811,118
49	METAL CHLORIDE GAS GENERATION METHOD AND APPARATUS	18/893,461
50	Data Storage Device and Method for Combining Prediction Models for Read Threshold Calibration	18/800,681
51	MULTILAYER ELECTRODE DEVICES AND METHOD OF MAKING THE SAME	18/882,360
52	MULTILAYER ELECTRODE DEVICES AND METHOD OF MAKING THE SAME	18/882,390
53	MULTILAYER ELECTRODE DEVICES AND METHOD OF MAKING THE SAME	18/882,410
54	MULTILAYER ELECTRODE DEVICES AND METHOD OF MAKING THE SAME	18/904,344
55	AREA EFFICIENT 3D NAND-BASED VECTOR-MATRIX MULTIPLIER CIRCUIT WITH COMMON-MODE CURRENT CANCELLATION	18/826,339
56	MITIGATING BIT LINE IR DROP IN 3D NAND NEURAL NETWORK ACCELERATOR	18/826,542
57	CHARGE PUMP CIRCUIT CONFIGURATION IN NONVOLATILE MEMORY	18/887,054
58	MULTI-PLANE LEAKAGE DETECTION IN NONVOLATILE MEMORY	18/825,432
59	THROUGHPUT OPTIMIZED 3D NAND-BASED VECTOR-BY-MATRIX MULTIPLIER CIRCUIT	18/830,759
60	OFFSET CALIBRATION SCHEMES IN TIME-BASED 3D NAND-BASED VECTOR-MATRIX MULTIPLIER CIRCUIT	18/917,095
61	NAND ACCELERATOR FOR VECTOR-VECTOR MULTIPLICATION	18/905,088
62	APPARATUS AND METHODS FOR MODIFYING IMPEDANCES IN TIME-BASED VECTOR-MATRIX MULTIPLICATION CIRCUITS	18/897,326
63	MULTI-PLANE NONVOLATILE MEMORY WITH SERIAL ENCODER AND DECODER CIRCUITS	18/825,452
64	NON-VOLATILE MEMORY WITH NON-DISCHARGING READ	18/894,550
65	CROSS-POINT SPIN-ORBIT TORQUE MAGNETORESISTIVE MEMORY ARRAY AND METHOD OF MAKING THE SAME	18/798,180
66	PRE-CHARGE UNSELECTED BLOCK WORD LINE BEFORE PROGRAM	18/894,270
67	PRE-CHARGE AT READ RECOVERY CLOCK FROM BIT LINE SIDE FOR SUB-BLOCK ONE PERFORMANCE IMPROVEMENT	18/797,072
68	TECHNIQUE TO DETECT AN UNSELECTED SUB-BLOCK STATUS IN A MEMORY DEVICE	18/887,730
69	TAMPER-RESISTANT MICROELECTRONIC CIRCUIT PACKAGES	18/886,576
70	Controller Memory Buffer (CMB) as Cache	18/818,259
71	DEVICES AND METHODS FOR TERMINATING TRANSMISSION LINES	18/805,352
72	DATA STORAGE SYSTEMS AND PROCESSES FOR DATA SEARCHING AND ORGANIZATION	18/816,377
73	NON-CONTACT SEMICONDUCTOR DIE SINGULATION PROCESS	18/806,220
74	SEMICONDUCTOR PACKAGE HAVING BIFACIAL SEMICONDUCTOR WAFERS	18/803,091
75	THREE-DIMENSIONAL MEMORY DEVICE WITH SIDE-CONTACT THROUGH-STACK CONTACT VIA STRUCTURES AND METHODS FOR FORMING THE SAME	18/824,214
76	OPTIMIZING DATA RETRIEVAL FROM STORAGE DEVICES	18/813,213
77	THREE-DIMENSIONAL MEMORY DEVICE WITH TOP-CONTACT THROUGH-STACK CONTACT VIA STRUCTURES AND METHODS FOR FORMING THE SAME	18/917,638
78	THREE-DIMENSIONAL MEMORY DEVICE WITH TOP-CONTACT THROUGH-STACK CONTACT VIA STRUCTURES AND METHODS FOR FORMING THE SAME	18/917,675
79	DOUBLE MAGNETIC TUNNEL JUNCTION MAGNETORESISTIVE MEMORY DEVICE AND METHOD OF MAKING THEREOF	18/882,112
80	SOT MRAM ARRAY INCLUDING SHARED BIT LINE CONNECTION VIA STRUCTURES AND METHOD OF MAKING THE SAME	18/828,504
81	MEMORY DEVICE INCLUDING A PERFORATED DIELECTRIC BRIDGE LAYER AND METHOD FOR FORMING THE SAME	18/909,661
82	NON-VOLATILE MEMORY ARRAY WITH INTEGRATED MEMORY AND ACCESS TRANSISTORS AND METHOD OF MAKING THE SAME	18/827,036
83	THREE-DIMENSIONAL MEMORY DEVICE WITH BACKSIDE GATE ELECTRODE AND METHODS OF FORMING THE SAME	18/883,650
84	STRUCTURES AND METHODS FOR ACCURATE SEGMENTING OF BAD BLOCKS OF NON-VOLATILE MEMORY	18/827,981
85	NON-VOLATILE MEMORY WITH ADJUSTABLE ERASE VOLTAGE	18/824,083
86	MULTI SENSE TIME VALLEY SEARCH IN NAND	18/808,409
87	Data Storage Device and Method for Dynamic Bit-Error-Rate Estimation Scan (BES)	18/903,283

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
88	FAILSAFE POWER MANAGEMENT TO AVOID SHORT-CIRCUITING FROM WATER DAMAGE IN SOLID STATE DRIVE USING CONDUCTIVITY DETECTOR	18/890,025
89	IN-PLACE ERASE TECHNIQUES FOR NONVOLATILE MEMORY DEVICES	18/886,384
90	NON-VOLATILE MEMORY WITH VARIABLE ON PITCH	18/886,398
91	EFFICIENT TRAINING METHOD FOR UNMATCHED DATA OUTPUT PATH IN NON-VOLATILE MEMORY	18/896,420
92	SGS VOLTAGE IN UNSELECTED BLOCKS DURING PROGRAM	18/905,292
93	REDUCED CURRENT SENSING TECHNIQUES	18/897,505
94	WORD LINE ZONE ERASE TECHNIQUES FOR MEMORY DEVICES	18/897,573
95	THRESHOLD VOLTAGE TRACKING TECHNIQUES FOR MEMORY DEVICES	18/897,684
96	FASTER METHOD TO PREVENT HYBRID SINGLE LEVEL CELL DEFECTS IN SYSTEM	18/891,932
97	STATE SKIP CODING FOR FRACTIONAL BIT-PER-CELL TECHNOLOGY TO IMPROVE DATA RETENTION	18/921,761
98	ENABLE OPEN SUB-BLOCK ERASE IN SUB-BLOCK MODE OPERATION	18/883,214
99	GATE INDUCED DRAIN LEAKAGE ERASE WITH ADAPTIVE BIAS ON TOP DRAIN-SIDE SELECT GATE TRANSISTOR AND BOTTOM SOURCE-SIDE SELECT GATE TRANSISTOR	18/883,219
100	CYCLING-AWARE ADAPTIVE PROGRAM VOLTAGE TUNING FOR PERFORMANCE IMPROVEMENT	18/883,221
101	SEMICONDUCTOR DEVICE WITH STRUCTURALLY REINFORCED CORNERS	18/825,864
102	READ TECHNIQUES FOR NON-VOLATILE MEMORY	18/897,714
103	Dynamic Clustering-Based Allocation of Free Chunks at L2P in Thin Provisioning	18/811,536
104	MANAGING TIME-CRITICAL COMMANDS IN A MULTI-CORE STORAGE DEVICE	18/892,779
105	POWER ON DATA RETENTION MANAGEMENT WITH DYNAMIC ACTIVATION ENERGY TABLE FOR NON-VOLATILE MEMORIES	18/830,257
106	DIE LEVEL FAILURE RECOVERY	18/886,461
107	ELECTRONIC DEVICE ENCLOSURE HAVING A PLURALITY OF SURFACE FEATURES	18/902,041
108	BONDED ASSEMBLIES AND METHODS FOR FORMING THE SAME USING POLYMER-BASED HYBRID BONDING	18/891,177
109	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING MULTI-SURFACE SCHOTTKY SOURCE CONTACT AND METHODS FOR FORMING THE SAME	18/897,891
110	THREE-DIMENSIONAL MEMORY DEVICE CONTAINING THERMALLY CONDUCTIVE AND INSULATING TRENCH FILL STRUCTURE AND METHODS FOR FORMING THE SAME USING LASER ANNEALING	18/920,034
111	Data Storage Device and Method for Providing Prolonged High Performance for Tenants in a Multi-Tenancy Environment	18/804,492
112	Data Storage Device and Method for Video Frame Link-Based Management and Processing	18/810,720
113	Pipeline Optimization in Low Power Mode Using PMR	18/817,040
114	Host Controlled Mitigation of Panic Situation	18/819,515
115	Dynamic Lane Allocation on Power Limited, Dual Port PCIe Device	18/829,622
116	Command Processing in Sequential Write Required Zone	18/829,608
117	HOST INDEPENDENT CONTROL OF STORAGE DEVICES USING CONTROL DEVICES	18/830,183
118	PEER-TO-PEER SURVEILLANCE CAMERA ARCHITECTURE USING SHARED METADATA DATASTORE	18/901,234
119	NONVOLATILE MEMORY WITH VOLTAGE OVERSHOOT MITIGATION	18/919,469
120	Apparatus and Processes for Magnetic Detection of an Analyte	18/830,920
121	NON-VOLATILE MEMORY WITH LOCATION DEPENDENT CONTROL GATE VOLTAGE	18/916,496
122	NONVOLATILE MEMORY WITH MULTI-CELL WEIGHT STRUCTURE	18/916,844
123	JOINT LDPC AND RAID DECODING SCHEME	18/922,289
124	PCIe LANE ADAPTER FOR ENABLING FLEXIBLE SWITCHING OF SPEED AND CAPACITY CONFIGURATIONS OF STORAGE DRIVES	18/894,152
125	ACTIVE AND PASSIVE ADAPTER FOR A MICROSD CARD	18/914,512
126	Data Storage Device and Method for Resource Optimization in Video Processing	18/813,426
127	MEMORY STRUCTURE WITH SECURE GLOBAL ERASE	18/824,397
128	SYNCHRONIZATION POINTS BASED PARAMETER TUNING IN A STORAGE DEVICE	18/894,234
129	Data Storage Device and Method for Maintaining a Weightage of Commands in a Plurality of Queue Layers	18/909,057
130	Data Storage Device and Method to Access Logical Block Range	18/916,686
131	Host and Dual Write Method for Avoiding Data Loss When Writing to an External Data Storage Device	18/825,264
132	Data Storage Device and Method for Buffer Occupancy-Based Data Placement to Avoid Video Loss	18/825,319

SCHEDULE A
TO PATENT COLLATERAL AGREEMENT
U.S. PATENTS AND PATENT APPLICATIONS

No.	TITLE	Reg. No. / App. No.
133	Data Storage Device and Method for Speculation-Driven Partial Shutdown	18/897,295
134	Data Storage Device and Method for On-the-Fly Mathematical Processing of Data Read from the Data Storage Device	18/904,260
135	Data Storage Device and Method for Avoiding Returning Zeros to a Host	18/904,223
136	TRANSIENT STATE MANAGEMENT OF AN INPUT/OUTPUT IMPACTED STORAGE DEVICE	18/914,582
137	Balanced Transfers on Interfaces	18/904,530
138	Efficient Data Access for Accelerated Administrative Commands	18/922,262
139	OPERATING IN A WRITE THROUGH MODE TRANSITION WHILE MAINTAINING DATA INTEGRITY AFTER AN ABRUPT SHUTDOWN ON A STORAGE DEVICE	18/914,526
140	Apparatus For Allowing The Protected mSets To Continue To Be Used During Control Sync (CS) On The Base Of Shadow uLayer	18/914,949
141	Self-Tracking Dynamic Allocation of Free Chunks at L2P in Thin Provisioning	18/919,573
142	NUCLEIC ACID SEQUENCING BY SYNTHESIS USING MAGNETIC SENSOR ARRAYS	62/833,130
143	NUCLEIC ACID SEQUENCING BY SYNTHESIS USING MAGNETIC SENSOR ARRAYS	17/602,319
144	MAGNETIC SENSOR ARRAYS FOR NUCLEIC ACID SEQUENCING AND METHODS OF MAKING AND USING THEM	62/987,831
145	MAGNETIC SENSOR ARRAYS FOR NUCLEIC ACID SEQUENCING AND METHODS OF MAKING AND USING THEM	17/905,724
146	High-Throughput DNA Sequencing with Single-Molecule Sensor-Arrays	63/013,236
147	HIGH-THROUGHPUT NUCLEIC ACID SEQUENCING WITH SINGLE-MOLECULE-SENSOR ARRAYS	17/996,360
148	Single-Molecule, Real-Time, Label-Free Dynamic Biosensing with Nanoscale Magnetic Field Sensors	62/705,639
149	SINGLE-MOLECULE, REAL-TIME, LABEL-FREE DYNAMIC BIOSENSING WITH NANOSCALE MAGNETIC FIELD SENSORS	18/004,402
150	SPIN TORQUE OSCILLATOR (STO) SENSORS USED IN NUCLEIC ACID SEQUENCING ARRAYS AND DETECTION SCHEMES FOR NUCLEIC ACID SEQUENCING	18/325,942
151	DEVICES AND METHODS FOR MOLECULE DETECTION BASED ON THERMAL STABILITIES OF MAGNETIC NANOPARTICLES	18/165,089
152	THERMAL SENSOR ARRAY FOR MOLECULE DETECTION AND RELATED DETECTION SCHEMES	17/661,578
153	Magnetoresistive Sensor Array for Molecule Detection and Related Detection Schemes	17/464,533
154	DEVICES AND METHODS FOR GENOME SEQUENCING	16/908,581
155	POWER REALLOCATION FOR MEMORY DEVICE	18/775,668
156	SSD WAFER DEVICE AND METHOD OF MANUFACTURING SAME	18/738,801
157	DEVICES, SYSTEMS, AND METHODS OF USING SMART FLUIDS TO CONTROL MOLECULE SPEEDS	17/643,401
158	SELF-ALIGNED SURFACE MODIFICATION FOR MAGNETOCHEMICAL SENSORS	17/649,249
159	LOW NOISE AMPLIFIERS WITH FEEDBACK FOR NANOPORE APPLICATIONS	18/590,557
160	LOW NOISE AMPLIFIERS WITH SHIELDS FOR NANOPORE APPLICATIONS	18/406,202
161	AMPLIFIERS FOR BIOLOGICAL SENSING APPLICATIONS	17/659,688
162	Reducing Link Up Time In PCIe Systems	18/740,042
163	DATA STORAGE DEVICE WITH NOISE INJECTION	18/670,512
164	Data Storage Device and Method for Device-Initiated Hibernation	18/760,409
165	SENSITIVITY AMPLIFICATION TECHNIQUES FOR MAGNETOCHEMICAL SENSORS	18/352,398
166	Magnetic Control of Molecule Translocation Speed Through a Nanopore	18/364,506
167	THREE-DIMENSIONAL MEMORY DEVICES INCLUDING SELF-ALIGNED SOURCE-CHANNEL JUNCTIONS AND METHODS FOR FORMING THE SAME	18/479,457
168	THREE-DIMENSIONAL MEMORY DEVICE WITH PILLAR SHAPED TRENCH BRIDGE STRUCTURES AND METHODS OF FORMING THE SAME	18/646,016
169	NUCLEIC ACID SEQUENCING USING NANOPORES	18/499,024
170	METHODS AND SYSTEMS FOR NUCLEIC ACID SEQUENCING USING NANOPORES	18/499,069
171	POWER SAVING DURING OPEN BLOCK READ WITH LARGE BLOCK OPENNESS	18/389,439
172	THREE-DIMENSIONAL MEMORY DEVICE WITH DUMMY SLIT REGIONS AND METHODS OF MAKING THE SAME	18/649,071
173	Host Bandwidth Limited SSDs With High-Rate NANDs	18/442,580
174	DATA-VALID WINDOW TRACKING FOR HIGH SPEED INTERFACE	18/679,470
175	ERASE BIAS SCHEME TO LOWER VERAMAX AND NAND CHIP-SIZE SHRINK	18/436,345

SCHEDULE A
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U.S. PATENTS AND PATENT APPLICATIONS

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176	READ METHOD ENHANCEMENT TO REDUCE READ DISTURB IN MIXED-MODE MEMORY STORAGE REGIONS	18/437,794
177	Early Read Start Time For Random Access SSDs	18/443,975
178	SINGLE-LEVEL MEMORY CELL ERROR ON-CHIP DETECTION	18/442,693
179	DECISION FEEDBACK EQUALIZER SENSE AMPLIFIER CIRCUITS AND METHODS FOR DOUBLE DATA RATE NONVOLATILE MEMORY DEVICES	18/663,824
180	METHODS TO IMPROVE CURRENT CONSUMPTION AND READ TIME IN SUCCESSIVE READS	18/443,992
181	DYNAMIC WORD LINE RAMP UP KICK FOR MEMORY DEVICES	18/443,933
182	REAL TIME RAMP RATE ADJUSTMENT FOR BETTER PERFORMANCE AND CURRENT CONSUMPTION TRADEOFF	18/442,709
183	LATERAL SUB-BLOCK MODE IN A MEMORY DEVICE	18/603,582
184	STRING BASED ERASE INHIBIT FOR ONE SIDED GATE-INDUCED DRAIN LEAKAGE ERASE	18/442,684
185	SYSTEM AND METHOD FOR MINIMIZING INSERTION LOSSES AND LOOP INDUCTANCE IN A PCB LAYOUT	18/651,922
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187	SEMICONDUCTOR DEVICE INCLUDING EMBEDDED SEMICONDUCTOR DIES	18/738,634
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190	NON-VOLATILE MEMORY WITH HYBRID ROUTING FOR SHARED WORD LINE SWITCHES	18/443,663