PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT4532752

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SRC LABS, LLC	08/02/2017

RECEIVING PARTY DATA

Name:	SAINT REGIS MOHAWK TRIBE
Street Address:	412 STATE ROUTE 37
City:	AKWESASNE
State/Country:	NEW YORK
Postal Code:	13655

PROPERTY NUMBERS Total: 42

Property Type	Number
Patent Number:	6026459
Patent Number:	6076152
Patent Number:	6247110
Patent Number:	6295598
Patent Number:	6339819
Patent Number:	6434687
Patent Number:	6594736
Patent Number:	6836823
Patent Number:	6941539
Patent Number:	6961841
Patent Number:	6964029
Patent Number:	6983456
Patent Number:	6996656
Patent Number:	7003593
Patent Number:	7124211
Patent Number:	7134120
Patent Number:	7149867
Patent Number:	7155602
Patent Number:	7155708
Patent Number:	7167976

Property Type	Number
Patent Number:	7197575
Patent Number:	7225324
Patent Number:	7237091
Patent Number:	7299458
Patent Number:	7373440
Patent Number:	7406573
Patent Number:	7421524
Patent Number:	7424552
Patent Number:	7565461
Patent Number:	7620800
Patent Number:	7680968
Patent Number:	7703085
Patent Number:	7890686
Patent Number:	8589666
Patent Number:	8713518
Patent Number:	8930892
Patent Number:	9153311
Patent Number:	9530483
Patent Number:	9727269
Application Number:	13365090
Application Number:	14284616
Application Number:	13903720

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	CHRIS EVANS
SIGNATURE:	/Chris Evans/
DATE SIGNED:	08/02/2017

Total Attachments: 6

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Patent Assignment Agreement

THIS PATENT ASSIGNMENT AGREEMENT is entered into on August 1, 2017 by and between SRC Labs, LLC, a Delaware limited liability company (Assignor) and Saint Regis Mohawk Tribe, a federally recognized American Indian Tribe (Assignee).

WHEREAS, Assignor is the sole and exclusive owner of the U.S. Patents and pending patent applications identified in Schedule A (the "**Patents**"); and

WHEREAS, Assignee desires to acquire all rights, title and interest in and to the Patents;

NOW, THEREFORE, the parties agree as follows:

1. **Assignment**. Be it known that in consideration of the payment by Assignee to Assignor of the sum of ten dollars ($10) and other valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Assignor hereby irrevocably conveys, transfers, and assigns to Assignee, and Assignee hereby accepts, all of Assignor's right, title, and interest in and to the following

    (a) the patents and patent applications set forth in Schedule A hereto and all issuances, divisions, continuations, continuations-in-part, reissues, extensions, reexaminations, and renewals thereof (the "**Patents**");

    (b) all rights of any kind whatsoever of Assignor accruing under any of the foregoing provided by applicable law of any jurisdiction, by international treaties and conventions, and otherwise throughout the world;

    (c) any and all royalties, fees, income, payments, and other proceeds now or hereafter due or payable with respect to any and all of the foregoing; and

    (d) any and all claims and causes of action with respect to any of the foregoing, whether accruing before, on, or after the date hereof, including all rights to and claims for damages, restitution, and injunctive and other legal and equitable relief for past, present, and future infringement, misappropriation, violation, misuse, breach, or default, with the right but no obligation to sue for such legal and equitable relief and to collect, or otherwise recover, any such damages.

2. **Covenants**. Assignor covenants and agrees and warrants that it has a full and unencumbered title to the invention hereby assigned, and further covenants and agrees that it has the right to grant such rights to said Patents and that it will, at any time upon request without cost or further compensation, execute and deliver any and

all papers or instruments that, in the opinion of the Assignee, may be necessary or desirable to secure said Assignee the full enjoyment of the rights and properties herein conveyed or intended to be conveyed by this instrument.

3. **Recordation and Further Actions**. Assignor hereby authorizes the Commissioner for Patents in the United States Patent and Trademark Office to record and register this Patent Assignment upon request by Assignee. Following the date hereof, Assignor shall take such steps and actions, and provide such cooperation and assistance to Assignee and its successors, assigns, and legal representatives, including the execution and delivery of any affidavits, declarations, oaths, exhibits, assignments, powers of attorney, or other documents, as may be necessary to effect, evidence, or perfect the assignment of the Assigned Patents to Assignee, or any assignee or successor thereto.

4. **Counterparts**. This Patent Assignment Agreement may be executed in counterparts, each of which shall be deemed an original, but all of which together shall be deemed one and the same agreement. A signed copy of this Patent Assignment Agreement delivered by facsimile, e-mail, or other means of electronic transmission shall be deemed to have the same legal effect as delivery of an original signed copy of this Patent Assignment Agreement.

5. **Successors and Assigns**. This Patent Assignment shall be binding upon and shall inure to the benefit of the parties hereto and their respective successors and assigns.

6. **Governing Law**. This Patent Assignment and any claim, controversy, dispute, or cause of action (whether in contract, tort, or otherwise) based upon, arising out of, or relating to this Patent Assignment Agreement and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of New York, without giving effect to any choice or conflict of law provision or rule (whether of the State of New York or any other jurisdiction).

IN WITNESS WHEREOF, Assignor has duly executed and delivered this Patent Assignment as of the date first above written.

SRC LABS, LLC

Signature: _____

Name and Title: Crystal Moore, President

Date: 8-2-17

AGREED TO AND ACCEPTED:

SAINT REGIS MOHAWK TRIBE

By: _____
Eric Thompson, Tribal Chief

Date: 8.2.17

By: _____
Beverly Cook, Tribal Chief

Date: 8-2-17

By: _____
Michael Conners, Tribal Chief

Date: 8-2-17

Schedule A

Jurisdiction	Title	Status	Patent No./Serial No.	Issued/Filing Date
U.S.	System and method for dynamic priority conflict resolution in a multi-processor computer system having shared memory resources	Issued	6,026,459	2/15/2000
U.S.	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem	Issued	6,076,152	6/13/2000
U.S.	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem	Issued	6,247,110	6/12/2001
U.S.	Split directory-based cache coherency technique for a multi-processor computer system	Issued	6,295,598	9/25/2001
U.S.	Multiprocessor with each processor element accessing operands in loaded input buffer and forwarding results to FIFO output buffer	Issued	6,339,819	1/15/2002
U.S.	System and method for accelerating web site access and processing utilizing a computer system incorporating reconfigurable processors operating under a single operating system image	Issued	6,434,687	8/13/2002
U.S.	System and method for semaphore and atomic operation management in a multiprocessor	Issued	6,594,736	7/15/2003
U.S.	Bandwidth enhancement for uncached devices	Issued	6,836,823	12/28/2004
U.S.	Efficiency of reconfigurable hardware	Issued	6,941,539	9/6/2005
U.S.	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem	Issued	6,961,841	11/1/2005
U.S.	System and method for partitioning control-dataflow graph representations	Issued	6,964,029	11/8/2005
U.S.	Process for converting programs in high-level programming languages to a unified executable for hybrid computing platforms	Issued	6,983,456	1/3/2006
U.S.	System and method for providing an arbitrated memory bus in a hybrid computing system	Issued	6,996,656	2/7/2006
U.S.	Computer system architecture and memory controller for close-coupling within a hybrid processing system utilizing an adaptive processor interface port	Issued	7,003,593	2/21/2006
U.S.	System and method for explicit communication of messages between processes running on different nodes in a clustered multiprocessor system	Issued	7,124,211	10/17/2006
U.S.	Map compiler pipelined loop structure	Issued	7,134,120	11/7/2006

U.S.	System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware	Issued	7,149,867	12/12/2006
U.S.	Interface for integrating reconfigurable processors into a general purpose computing system	Issued	7,155,602	12/26/2006
U.S.	Debugging and performance profiling using control-dataflow graph representations with reconfigurable hardware emulation	Issued	7,155,708	12/26/2006
U.S.	Interface for integrating reconfigurable processors into a general purpose computing system	Issued	7,167,976	1/23/2007
U.S.	Switch/network adapter port coupling a reconfigurable processing element to one or more microprocessors for use with interleaved memory controllers	Issued	7,197,575	3/27/2007
U.S.	Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions	Issued	7,225,324	3/29/2007
U.S.	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem	Issued	7,237,091	6/26/2007
U.S.	System and method for converting control flow graph representations to control-dataflow graph representations	Issued	7,299,458	11/20/2007
U.S.	Switch/network adapter port for clustered computers employing a chain of multi-adaptive processors in a dual in-line memory module format	Issued	7,373,440	5/13/2008
U.S.	Reconfigurable processor element utilizing both coarse and fine grained reconfigurable elements	Issued	7,406,573	7/29/2008
U.S.	Switch/network adapter port for clustered computers employing a chain of multi-adaptive processors in a dual in-line memory module format	Issued	7,421,524	9/2/2008
U.S.	Switch/network adapter port incorporating shared memory resources selectively accessible by a direct execution logic element and one or more dense logic devices	Issued	7,424,552	9/9/2008
U.S.	Switch/network adapter port coupling a reconfigurable processing element to one or more microprocessors for use with interleaved memory controllers	Issued	7,565,461	7/21/2009
U.S.	Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions	Issued	7,620,800	11/17/2009
U.S.	Switch/network adapter port incorporating shared memory resources selectively accessible by a direct execution logic element and one or more dense logic devices in a fully buffered dual in-line memory module format (FB-DIMM)	Issued	7,680,968	3/16/2010

U.S.	Process for converting programs in high-level programming languages to a unified executable for hybrid computing platforms	Issued	7,703,085	4/20/2010
U.S.	Dynamic priority conflict resolution in a multi-processor computer system having shared resources	Issued	7,890,686	2/15/2011
U.S.	Elimination of stream consumer loop overshoot effects	Issued	8,589,666	11/19/2013
U.S.	System and method for computational unification of heterogeneous implicit and explicit processing elements	Issued	8,713,518	4/29/2014
U.S.	System and method for computational unification of heterogeneous implicit and explicit processing elements	Issued	8,930,892	1/6/2015
U.S.	System and method for retaining DRAM data when reprogramming reconfigurable devices with DRAM memory controllers	Issued	9,153,311	3/27/2014
U.S.	System and method for retaining dram data when reprogramming reconfigurable devices with DRAM memory controllers incorporating a data maintenance block colocated with a memory module or subsystem	Issued	9,530,483	12/27/2016
U.S.	System and method for retaining DRAM data when reprogramming reconfigurable devices with DRAM memory controllers incorporating a data maintenance block colocated with a memory module or subsystem	Issued	9,727,269	8/8/2017
U.S.	Mobile electronic devices utilizing reconfigurable processing techniques to enable higher speed applications with lowered power consumption	Pending	13/365,090	2/2/2012
U.S.	System and method for thermally coupling memory devices to a memory controller in a computer memory board	Pending	14/284,616	3/22/2014
U.S.	Multi-processor computer architecture incorporating distributed multi-ported common memory modules	Pending	13/903,720	5/28/2013