TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
COMERICA BANK		09/11/2009	Texas banking association:

RECEIVING PARTY DATA

Name:	LOGICVISION
Street Address:	25 Metro Drive
Internal Address:	3rd Floor
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95110
Entity Type:	CORPORATION: DELAWARE

PROPERTY NUMBERS Total: 8

Property Type	Number	Word Mark
Serial Number:	77576058	SILICON QUALITY AT THE RIGHT COST
Serial Number:	77407740	DRAGONFLY
Registration Number:	3435241	SILICON INSIGHT
Registration Number:	3435237	LOGICVISION
Serial Number:	77284913	YIELD INSIGHT
Registration Number:	3020734	ETCHECKER
Registration Number:	3127630	EYES IN THE DIE
Registration Number:	2097329	

CH $215.00 77576058

CORRESPONDENCE DATA

Fax Number: (858)550-6420
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 858-550-6403
Email: erin.obrien@cooley.com
Correspondent Name: Erin O'Brien

Address Line 1:	c/o Cooley Godward Kronish LLP
Address Line 2:	4401 Eastgate Mall
Address Line 4:	San Diego, CALIFORNIA 92121

ATTORNEY DOCKET NUMBER:	036703-1181 LOGICVISION
NAME OF SUBMITTER:	Erin O'Brien
Signature:	/Erin O'Brien/
Date:	09/11/2009

Total Attachments: 7
source=Logicvision IP release#page1.tif
source=Logicvision IP release#page2.tif
source=Logicvision IP release#page3.tif
source=Logicvision IP release#page4.tif
source=Logicvision IP release#page5.tif
source=Logicvision IP release#page6.tif
source=Logicvision IP release#page7.tif

RELEASE OF SECURITY INTEREST

This Release of Security Interest is made as of September 11, 2009 by COMERICA BANK ("Bank") in favor of LogicVision, Inc., a Delaware Corporation, with its principal place of business at 25 Metro Drive, 3rd Floor, San Jose, CA 95110 ("Company").

Recital

WHEREAS, COMPANY assigned certain interests in the patents and trademarks described on Exhibits A and B and attached hereto, respectively (collectively, the "Intellectual Property") to BANK under an Intellectual Property Security Agreement dated as of April 24, 2009, and recorded with the US Patent and Trademark Office as set forth on Exhibits A and B.

WHEREAS, COMPANY has satisfied all its obligations to BANK in the Intellectual Property Security Agreement, and BANK wishes to release its security interest in the Intellectual Property.

Agreement

Now Therefore, BANK agrees that it terminates and releases its security interest in the Intellectual Property and reassigns to COMPANY, without warranty or recourse, all interest of BANK in the Intellectual Property.

BANK: COMERICA BANK

Michael S. Sak
Assistant Vice President
September 11, 2009

Address:
Comerica Bank
CLS Collateral Services, MC 7575
39200 Six Mile Road
Livonia, MI 48152

EXHIBIT A

PATENTS

Title	App. No.	Filing Date	Reg. No.	Date Granted
Circuit and method for measuring delay of high speed signals	10/991365	11/19/04	7453255	11/18/08
Clocking methodology for at-speed testing of scan circuits with synchronous clocks	11/060407	2/18/05	7424656	9/9/08
Method and circuit for collecting memory failure information	10/690594	10/23/03	7370251	5/6/08
Method and apparatus for storing and distributing memory repair information	11/853383	9/11/07	n/a	n/a
Memory repair circuit and method	10/868208	6/16/04	7257733	8/14/07
Boundary scan with strobed pad driver enable	10/701497	11/6/03	7219282	5/15/07
Method and circuit for at-speed testing of scan circuits	10/739055	12/19/03	7194669	3/20/07
Method of and program product for performing gate-level diagnosis of failing vectors	10/435094	5/12/03	7191374	3/13/07
Memory repair analysis method and circuit	10/774512	3/6/07	7188274	2/10/04
Circuit and method for adding parametric test capability to digital boundary scan	10/414309	4/16/03	7159159	1/2/07
Circuit and method for measuring jitter of high speed signals	10/947189	9/23/04	7158899	1/2/07
Clock controller for at-speed testing of scan circuits	11/013319	12/17/04	7155651	12/26/06
Method and test circuit for testing memory internal write enable	10/638388	8/12/03	7139946	11/21/06
Verification of embedded test structures in circuit designs	10/349452	1/23/03	7103860	9/5/06
Insertion of embedded test in RTL to GDSII flow	11/144764	6/6/05	n/a	n/a

Bank's security interest recorded at the US Patent and Trademark Office on May 4, 2009 at Reel and Frame Number 022629/0938.

Title	App. No.	Filing Date	Reg. No.	Date Granted
Method, system and program product for testing and/or diagnosing circuits using embedded test controller access data	09/954078	9/18/01	6961871	11/1/05
Masking circuit and method of masking corrupted bits	11/109844	4/20/05	n/a	n/a
Circuit and method for low frequency testing of high frequency signal waveforms	10/895336	7/21/04	n/a	n/a
Circuit and method for testing high speed data circuits	10/727583	12/5/03	6895535	5/17/05
Circuit and method for accurately applying a voltage to a node of an integrated circuit	10/634902	8/6/03	6885213	4/26/05
Method and program product for detecting bus conflict and floating bus conditions in circuit designs	09/817299	4/19/05	6883134	3/27/01
Method and program product for designing hierarchical circuit for quiescent current testing and circuit produced thereby	10/011128	12/10/01	6868532	3/15/05
Method and program product for designing hierarchical circuit for quiescent current testing	10/015751	12/17/01	6862717	3/1/05
Method of testing embedded memory array and embedded memory controller for use therewith	09/888607	6/26/01	6834361	12/21/04
Method of designing circuit having multiple test access ports, circuit produced thereby and method of using same	09/843307	4/27/01	6829730	12/7/04
Method for scan testing of digital circuit, digital circuit for use therewith and program product for incorporating test methodology into circuit description	09/773541	2/2/01	6763489	7/13/04
Test access circuit and method of accessing embedded test controllers in integrated circuit modules	10/139294	5/7/02	6760874	7/6/04
Method of masking corrupt bits during signature analysis and circuit for use therewith	10/162917	6/6/02	6745359	6/1/04

Title	App. No.	Filing Date	Reg. No.	Date Granted
Method for collecting failure information for a memory using an embedded test controller	10/156117	5/29/02	6738938	5/18/04
Method and program product for completing a circuit design having embedded test structures	10/323815	12/20/02	6725435	4/20/04
Circuit and method for determining the location of defect in a circuit	10/162916	6/6/02	6717415	4/6/04
Method and circuit for testing high frequency mixed signal circuits with low frequency signals	10/300620	11/21/02	6703820	3/9/04
Method for scan controlled sequential sampling of analog signals and circuit for use therewith	09/768501	1/25/01	6691269	2/10/04
Self-contained embedded test design environment and environment setup utility	10/323979	12/20/02	6678875	1/13/04
Scan test method for providing real time identification of failing test patterns and test bist controller for use therewith	10/180116	6/27/02	6671839	12/30/03
Heirarchial design and test method and system, program product embodying the method and integrated circuit produced thereby	09/626877	7/27/00	6615392	9/2/03
Method and circuitry for controlling clocks of embedded blocks during logic bist test mode	10/125384	4/19/02	6614263	9/2/03
Circuit and method for detecting transient voltages on a DC power supply rail	09/888605	6/26/01	6590412	7/8/03
Method and circuit for testing DC parameters of circuit input and output nodes	09/570412	5/12/00	6586921	7/1/03
Circuit synthesis method using technology parameters extracting circuit	10/021810	12/20/01	6567971	5/20/03
Method and apparatus for testing high performance circuits	09/607128	6/29/00	6510534	1/21/03
Method for testing circuits with tri-state drivers and circuit for use therewith	09/472386	12/23/99	6487688	11/26/02

Title	App. No.	Filing Date	Reg. No.	Date Granted
Method and circuit for testing high frequency mixed signal circuits with low frequency signals	09/842700	4/27/01	6492798	12/10/02
Method and apparatus for testing circuits with multiple clocks	09/430686	10/29/99	6442722	5/27/02
Method and circuit for built in self test of phase locked loops	09/184516	11/2/98	6396889	5/28/02
Method for testability analysis and test point insertion at the re-level of a hardware development language (HDL) specification	09/098555	6/16/98	636520	3/26/02
Method and apparatus for controlling power level during blat	09/218764	12/22/98	6330681	12/11/01
Method of testing at-speed circuits having asynchronous clocks and controller for use therewith	09/309827	5/11/99	6327684	12/4/01
Test Circuit and method for measuring switching point voltages and integral non-linearity (INL) of analog to digital converters	09/191154	11/12/98	6211803	4/3/01
Programmable clock signal generation circuits and methods for generating accurate, high frequency, clock signals	09/316197	5/21/99	6204694	3/20/01
Method and apparatus for scan testing digital circuits	09/192839	11/16/98	6145105	11/7/00
Clock skew management method and apparatus	09/209790	12/11/98	6115827	9/5/00
Asynchronous interface	08/825446	3/28/97	5900753	5/4/99
Method and apparatus for testing digital to analog and analog to digital converters	08/663493	6/14/96	5659312	8/19/97
Method for at-speed testing of memory interface using scan	11/439497	5/24/06	n/a	n/a
Semiconductor characterization and production information system	10/262737	10/2/02	6720194	4/13/04

Title	App. No.	Filing Date	Reg. No.	Date Granted
Method and system for collecting diverse data types within a manufacturing environment and accessing the diverse data types through a network portal	09/896170	6/29/01	n/a	n/a
Processor interface for test access port	10/892203	7/16/02	n/a	n/a
Method for testing parameters of high speed data signals	10/724193	12/1/03	n/a	n/a
Ceiling lamp junction box/lamp rod folding installation structure	10/690596	10/23/03	6945665	9/20/05
Method and system for licensing intellectual property circuits	10/357203	2/4/03	n/a	n/a
Circuit and method for compensating for non-linear distortion	10/100620	3/18/02	n/a	n/a
Method and apparatus for high-speed interconnect testing	08/948842	10/10/97	6000051	12/7/99
Bist architecture for measurement of integrated circuit delays	08/771302	12/20/96	5923676	7/13/99

EXHIBIT B

TRADEMARKS

Mark	App. No.	Filing Date	Reg. No.	Reg. Date
SILICON QUALITY AT THE RIGHT COST	77/576058	9/22/08	n/a	n/a
DRAGONFLY	77/407740	2/27/08	n/a	n/a
SILICON INSIGHT	77/284887	9/20/07	3,435,241	5/27/08
LOGICVISION	77/284832	9/20/07	3,435,237	5/27/08
YIELD INSIGHT	77/284913	9/20/07	n/a	n/a
ETCHECKER	78/496616	10/7/04	3,020,734	11/29/05
EYES IN THE DIE	78/377274	3/2/04	3,127,630	8/8/06
(Design Only)	75/147370	8/8/96	2,097,329	9/16/97

Bank's security interest recorded at the US Patent and Trademark Office on May 4, 2009 at Reel and Frame Number 003962/0022.