

TRADEMARK ASSIGNMENT

Electronic Version v1.1
 Stylesheet Version v1.1

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|------------------------------------------|--------------------------------------------------------------------------------------|-----------------------|-------------------------------------|
| SUBMISSION TYPE: | NEW ASSIGNMENT | | |
| NATURE OF CONVEYANCE: | Security Agreement | | |
| CONVEYING PARTY DATA | | | |
| Name | Formerly | Execution Date | Entity Type |
| SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC | | 12/14/2009 | LIMITED LIABILITY COMPANY: DELAWARE |
| RECEIVING PARTY DATA | | | |
| Name: | JPMORGAN CHASE BANK, N.A., as collateral agent | | |
| Street Address: | 270 Park Avenue | | |
| City: | New York | | |
| State/Country: | NEW YORK | | |
| Postal Code: | 10017 | | |
| Entity Type: | Association: UNITED STATES | | |
| PROPERTY NUMBERS Total: 3 | | | |
| Property Type | Number | Word Mark | |
| Serial Number: | 77825219 | ZURIUM | |
| Serial Number: | 77502351 | GREENPOINT | |
| Serial Number: | 77502376 | GREENPOINT | |
| CORRESPONDENCE DATA | | | |
| Fax Number: | (866)826-5420 | | |
| | <i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i> | | |
| Phone: | 3016380511 | | |
| Email: | ipresearchplus@comcast.net | | |
| Correspondent Name: | IP Research Plus, Inc. | | |
| Address Line 1: | 21 Tadcaster Circle | | |
| Address Line 2: | Attn: Penelope J.A. Agodoa | | |
| Address Line 4: | Waldorf, MARYLAND 20602 | | |
| ATTORNEY DOCKET NUMBER: | 35265 | | |

OP \$90.00 77825219

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**TRADEMARK
 REEL: 004122 FRAME: 0834**

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| NAME OF SUBMITTER: | Penelope J.A. Agodoa |
| Signature: | /pja/ |
| Date: | 12/30/2009 |
| <p>Total Attachments: 17 source=35265#page1.tif source=35265#page2.tif source=35265#page3.tif source=35265#page4.tif source=35265#page5.tif source=35265#page6.tif source=35265#page7.tif source=35265#page8.tif source=35265#page9.tif source=35265#page10.tif source=35265#page11.tif source=35265#page12.tif source=35265#page13.tif source=35265#page14.tif source=35265#page15.tif source=35265#page16.tif source=35265#page17.tif</p> | |

PATENT AND TRADEMARK SECURITY
 AGREEMENT, dated as of December 14, 2009 (this
 “Agreement”), among SEMICONDUCTOR COMPONENTS
 INDUSTRIES, LLC (the “Grantor”) and JPMORGAN CHASE
 BANK, N.A., as Collateral Agent (the “Collateral Agent”).

Reference is made to the Security Agreement dated as of August 4, 1999, as amended and restated as of March 3, 2003 (as amended, supplemented or otherwise modified from time to time, the “Security Agreement”), among the Grantor, ON Semiconductor Corporation (“Holdings”), the subsidiaries of Holdings party thereto and the Collateral Agent. The Lenders have agreed to extend credit to the Grantor subject to the terms and conditions set forth in the Amended and Restated Credit Agreement dated as of August 4, 1999, as amended and restated as of March 6, 2007 (as amended, supplemented or otherwise modified from time to time (the “Amended and Restated Credit Agreement”). The obligations of the Lenders to continue to extend such credit are conditioned upon, among other things, the execution and delivery of this Agreement. Accordingly, the parties hereto agree as follows:

SECTION 1. Terms. Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Security Agreement. The rules of construction specified in Section 1.03 of the Security Agreement also apply to this Agreement.

SECTION 2. Grant of Security Interest. As security for the payment or performance, as the case may be, in full of the Obligations, the Grantor, pursuant to the Security Agreement, did and hereby does grant to the Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in, all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by the Grantor or in which the Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the “Patent and Trademark Collateral”):

all letters patent of the United States or the equivalent thereof in any other country, all registrations and recordings thereof, and all applications for letters patent of the United States or the equivalent thereof in any other country, including registrations, recordings and pending applications in the United States Patent and Trademark Office or any similar offices in any other country, including those listed on Schedule A (the “Patents”) and all reissues, continuations, divisions, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, use and/or sell the inventions disclosed or claimed therein;

all trademarks, service marks, trade names, corporate names, company names, business names, fictitious business names, trade styles, trade dress, logos, other source or business identifiers, designs and general intangibles of like nature, now existing or hereafter adopted or acquired, all registrations and recordings

thereof, and all registration and recording applications filed in connection therewith, including registrations and registration applications in the United States Patent and Trademark Office, any State of the United States or any similar offices in any other country or any political subdivision thereof, and all extensions or renewals thereof, including, without limitation, those listed on Schedule A hereto (the "Trademarks");

all goodwill associated with or symbolized by the Patents and Trademarks;
and

all other assets, rights and interests that uniquely reflect or embody the Patents and Trademarks.

SECTION 3. Termination. This Agreement is made to secure the satisfactory performance and payment of the Obligations. Upon termination of the Security Agreement or release of a Grantor's obligations thereunder, this Agreement shall automatically terminate as to such Grantor.

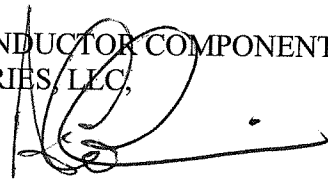
SECTION 4. Security Agreement. The security interests granted to the Collateral Agent herein are granted in furtherance, and not in limitation of, the security interests granted to the Collateral Agent pursuant to the Security Agreement. The Grantor hereby acknowledges and affirms that the rights and remedies of the Collateral Agent with respect to the Patent and Trademark Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Security Agreement, the terms of the Security Agreement shall govern.

SECTION 5. Counterparts. This Agreement may be executed in any number of counterparts, each of which shall constitute an original but all of which, when taken together, shall constitute one agreement. Delivery of an executed counterpart of a signature page of this Agreement by facsimile or other customary means of electronic transmission shall be effective as delivery of a manually executed counterpart hereof.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

SEMICONDUCTOR COMPONENTS
INDUSTRIES, LEC,

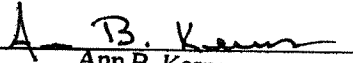
by



Name: Donald A. Colvin
Title: Executive Vice President
and Chief Financial Officer

JPMORGAN CHASE BANK, N.A., as
Collateral Agent,

by


Name: Ann B. Kerns
Title: Vice President

Schedule A

| <u>Debtor Name (Registered Owner of I.P.)</u> | <u>Type of Intellectual Property (Patent, Trademark)</u> | <u>Title of Intellectual Property</u> | <u>Patent No./ Pub. App. No./ Serial No.</u> | <u>Issuance Date/ Date Filed</u> |
|---------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------|
| Semiconductor Components Industries, LLC | Patent | EDGE SEAL FOR A SEMICONDUCTOR DEVICE AND METHOD THEREFOR | 12/499241 | 5/25/2007 |
| | Patent | EDGE SEAL FOR A SEMICONDUCTOR DEVICE AND METHOD THEREFOR | 12/499429 | 5/25/2007 |
| | Patent | METHOD OF FORMING A LEADED MOLDED ARRAY PACKAGE | 12/535475 | 10/28/2005 |
| | Patent | TRANSISTOR DIAGNOSTIC CIRCUIT | 12/548293 | 11/14/2005 |
| | Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 12/549100 | 12/29/2006 |
| | Patent | METHOD OF FORMING A MOLDED ARRAY PACKAGE DEVICE HAVING AN EXPOSED TAB | 12/553706 | 10/5/2005 |
| | Patent | METHOD FOR DETECTING A CURRENT AND COMPENSATING FOR AN OFFSET VOLTAGE | 12/557206 | 9/10/2009 |
| | Patent | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND STRUCTURE | 12/569732 | 9/29/2009 |
| | | | | |

| <u>Debtor Name (Registered Owner of I.P.)</u> | <u>Type of Intellectual Property (Patent, Trademark)</u> | <u>Title of Intellectual Property</u> | <u>Patent No./ Pub. App. No./ Serial No.</u> | <u>Issuance Date/ Date Filed</u> |
|---------------------------------------------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------|
| | Patent | HIGH VOLTAGE SENSOR DEVICE AND METHOD THEREFOR | 12/570300 | 1/25/2005 |
| | Patent | GROUND FAULT CIRCUIT INTERRUPTER AND METHOD | 12/572870 | 10/2/2009 |
| | Patent | LOW CLAMP VOLTAGE ESD DEVICE AND METHOD THEREFOR | 200910140241.5 | 7/10/2008 |
| | Patent | SEMICONDUCTOR TRENCH HAVING A SEALING PLUG AND METHOD | 200910140240.0 | 9/8/2008 |
| | Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 200910151749.5 | 9/8/2008 |
| | Patent | METHOD OF FORMING AN INTEGRATED SEMICONDUCTOR DEVICE AND STRUCTURE THEREFOR | 200910151751.2 | 9/11/2008 |
| | Patent | METHOD OF FORMING AN MOS TRANSISTOR AND STRUCTURE THEREFOR | 200910151750.8 | 9/24/2008 |
| | Patent | TWO TERMINAL MULTI-CHANNEL ESD DEVICE AND METHOD THEREFOR | 200910173120.0 | 10/15/2008 |
| | Patent | METHOD FOR REGULATING A VOLTAGE AND CIRCUIT THEREFOR | 09106134.5 | 3/2/2006 |

| <u>Debtor Name (Registered Owner of I.P.)</u> | <u>Type of Intellectual Property (Patent, Trademark)</u> | <u>Title of Intellectual Property</u> | <u>Patent No./ Pub. App. No./ Serial No.</u> | <u>Issuance Date/ Date Filed</u> |
|---------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------------------|--------------------------------------------------|--------------------------------------|
| | Patent | METHOD FOR REGULATING A VOLTAGE AND CIRCUIT THEREFOR | 09106133.6 | 3/2/2006 |
| | Patent | METHOD FOR REGULATING A VOLTAGE AND CIRCUIT THEREFOR | 09106132.7 | 4/18/2006 |
| | Patent | METHOD FOR MAKING A DIRECT CHIP ATTACH DEVICE AND STRUCTURE | 09106190.6 | 6/26/2003 |
| | Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 09106192.4 | 9/5/2007 |
| | Patent | CLASS-D AMPLIFIER AND METHOD THEREFOR | 09106796.4 | 3/3/2006 |
| | Patent | METHOD OF FORMING A SIGNAL LEVEL TRANSLATOR AND STRUCTURE THEREFOR | 09106794.6 | 4/17/2006 |
| | Patent | METHOD OF FORMING LOW CAPACITANCE ESD DEVICE AND STRUCTURE THEREFOR | 09106792.8 | 9/21/2007 |
| | Patent | METHOD OF FORMING A HIGH CAPACITANCE DIODE AND STRUCTURE THEREFOR | 09106793.7 | 9/21/2007 |
| | Patent | FLIP CHIP STRUCTURE AND METHOD OF MANUFACTURE | 09107126.3 | 9/20/2007 |
| | Patent | MULTI-CHANNEL ESD DEVICE | 09107694.5 | 9/21/2007 |

| <u>Debtor Name (Registered Owner of I.P.)</u> | <u>Type of Intellectual Property (Patent, Trademark)</u> | <u>Title of Intellectual Property</u> | <u>Patent No./ Pub. App. No./ Serial No.</u> | <u>Issuance Date/ Date Filed</u> |
|---------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------|
| | Patent | AND METHOD THEREFOR | | |
| | Patent | POWER SUPPLY CONTROLLER AND METHOD THEREFOR | 09107782.8 | 10/31/2007 |
| Semiconductor Components Industries, LLC | Patent | LED CURRENT CONTROLLER AND METHOD THEREFOR | 09108822.8 | 6/29/2006 |
| | Patent | CONSTANT CURRENT CHARGE PUMP CONTROLLER | 09108813.9 | 7/7/2006 |
| | Patent | AMPLIFICATION CIRCUIT AND METHOD THEREFOR | 09108824.6 | 7/25/2006 |
| | Patent | CHARGE PUMP CONTROLLER AND METHOD THEREFOR | 09108825.5 | 8/28/2006 |
| | Patent | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT AND STRUCTURE THEREFOR | 09108783.5 | 10/23/2007 |
| | Patent | LOW CLAMP VOLTAGE ESD DEVICE AND METHOD THEREFOR | 10-2009-0061172 | 7/10/2008 |
| | Patent | THINNED SEMICONDUCTOR WAFER AND METHOD OF THINNING A SEMICONDUCTOR WAFER | 10-2009-0077418 | 9/8/2008 |
| | Patent | SEMICONDUCTOR TRENCH HAVING A SEALING PLUG AND METHOD | 10-2009-0081345 | 9/8/2008 |

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|--------|--------------------------------------------------------------------------------|-------------------|-----------------------------|
| Patent | SEMICONDUCTOR DEVICE HAVING VERTICAL CHARGE-COMPENSATING STRUCTURE AND | 10-2009-0082835 | 9/8/2008 |
| Patent | METHOD OF FORMING A POWER SUPPLY CONTROLLER AND SYSTEM THEREFOR | PCT/US2009/056483 | 9/10/2009 |
| Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 098132534 | 11/14/2008 |
| Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 098132548 | 11/14/2008 |
| Patent | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 098132547 | 11/14/2008 |
| Patent | METHOD FOR CHANGING AN OUTPUT VOLTAGE AND CIRCUIT THEREFOR | 098132532 | 12/17/2008 |
| Patent | AMPLIFIER WITH REDUCED OUTPUT TRANSIENTS AND METHOD THEREFOR | 098133643 | 10/21/2008 |
| Patent | DC-DC CONVERTER CONTROLLER HAVING OPTIMIZED LOAD TRANSIENT RESPONSE AND METHOD | 10-2009-7016926 | 10/24/2005 NFL 8/13/2009 |
| Patent | SINGLE INPUT DUAL OUTPUT VOLTAGE POWER SUPPLY AND METHOD THEREFOR | 10-2009-7015945 | 1/10/2007 NFL 7/29/2009 |
| Patent | METHOD OF FORMING A POWER SUPPLY CONTROLLER AND STRUCTURE THEREFOR | 200780051213.5 | 3/19/2007 NFL 8/11/2009 |

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|--------|--------------------------------------------------------------------|-------------------|------------------------|-----|
| Patent | METHOD OF FORMING A POWER SUPPLY CONTROLLER AND STRUCTURE THEREFOR | 10-2009-7018727 | 3/19/2007 9/8/2009 | NFL |
| Patent | POWER SUPPLY CONTROLLER AND METHOD THEREFOR | 200780051811.2 | 3/19/2007 8/27/2009 | NFL |
| Patent | POWER SUPPLY CONTROLLER AND METHOD THEREFOR | 10-2009-7018728 | 3/19/2007 9/8/2009 | NFL |
| Patent | METHOD OF FORMING A CHARGE PUMP CONTROLLER AND STRUCTURE THEREFOR | PCT/US2007/067790 | 4/30/2007 9/23/2009 | NFL |
| Patent | CIRCUIT AND METHOD FOR REGULATING VOLTAGE | 11/424222 | 6/14/2006 | |
| Patent | CIRCUIT AND METHOD FOR REGULATING VOLTAGE | 200710110043.5 | 6/12/2007 | |
| Patent | CIRCUIT AND METHOD FOR REGULATING VOLTAGE | 08104881.6 | 5/02/2008 | |
| Patent | Alignment of Trench For Mos | 12/560,025 | 4/26/2005 | |

| Registered Owner | Title | Application # | Patent # | Patent Recording |
|------------------------------------------|----------------------------------------------------------------|---------------|----------|------------------|
| Semiconductor Components Industries, LLC | Multi-phase power supply controller and method therefor | 11/970326 | | |
| | Monolithically integrated multiplexor-translator demultiplexor | 11/966723 | | |
| | Method of forming a PWM controller and structure therefor | 11/954546 | | |
| | PWM controller and method therefor | 11/954506 | | |
| | Semiconductor component and method of manufacture | 11/931994 | | |

| Registered Owner | Title | Application # | Patent Recording # |
|------------------|-----------------------------------------------------------------------|---------------|--------------------|
| | Semiconductor component and method of manufacture | 11/931606 | |
| | Power supply controller and method therefor | 11/930933 | |
| | Regulated charge pump and method therefor | 11/916508 | |
| | Multi-chip semiconductor connector assemblies | 11/860379 | 7,508,060 |
| | Method of forming a high capacitance diode and structure therefor | 11/859638 | |
| | Multi-channel ESD device and method therefor | 11/859624 | |
| | Method of forming low capacitance ESD device and structure therefor | 11/859570 | 7,538,395 |
| | Flip chip structure and method of manufacture | 11/858289 | |
| | Semiconductor component and method of manufacture | 11/850153 | |
| | Method of forming an ESD detector and structure therefor | 11/843822 | |
| | Semiconductor die singulation method | 11/834924 | |
| | Method of forming a buck-boost mode power supply controller structure | 11/816699 | |
| | Low power voltage detection circuit and method therefor | 11/815835 | |
| | Amplification circuit and method therefor | 11/815431 | |
| | Power supply control method and structure therefor | 11/814656 | |
| | PWM controller and method therefor | 11/780611 | 7453298 |
| | Vertical MOS transistor and method therefor | 11/777893 | |
| | Improved power supply controller and method therefor | 11/776843 | 7545134 |

| Registered Owner | Title | Application # | Patent Recording # |
|------------------|-----------------------------------------------------------------------------|---------------|--------------------|
| | Digital compensation tuning for switching power supply control | 11/735615 | |
| | Method of forming a current sense circuit and structure therefor | 11/719998 | |
| | Digital compensation tuning for switching power supply control | 11/685091 | |
| | Switching power supply controller with unidirectional transient gain change | 11/555460 | |
| | Power supply output monitor | 11/367003 | 7466894 |
| | Fan speed control system | 10/178436 | 7483270 |
| | Semiconductor device having enhanced performance and method | 12/131295 | |
| | Switching power supply control | 11/109466 | |
| | Encapsulated chip scale package having flip-chip on lead frame structure | 12/107568 | |
| | Method for manufacturing a semiconductor component and structure therefor | 12/049909 | |
| | Semiconductor package structure for vertical mount and method | 12/017856 | 7566967 |
| | Voltage regulator compensation circuit and method | 09/249266 | 6064187 |
| | Fan speed control system | 09/470800 | 6188189 |
| | Voltage regulator compensation circuit and method | 09/557785 | 6229292 |
| | Address selection circuitry and method using single analog input line | 09/383447 | 6255973 |
| | Switching voltage regulator failure detection circuit and method | 09/688412 | 6473280 |
| | Method and apparatus for determining fan speed | 09/595953 | 6528987 |

| Registered Owner | Title | Application # | Patent Recording # |
|------------------|--------------------------------------------------------------------------------|---------------|--------------------|
| | Four current transistor temperature sensor and method | 09/837816 | 6554469 |
| | Hiccup-mode short circuit protection circuit and method for linear voltage | 09/882998 | 6680837 |
| | Switched noise filter circuit for DC-DC converters constant on time | 10/762650 | 6958594 |
| | Self-aligned transistor | 11/864327 | 7397070 |
| | Semiconductor device having trench charge compensation regions and method | 11/442733 | 7411266 |
| | Power semiconductor device having improved performance and method | 12/236947 | |
| | Low side driver | 12/188962 | |
| | Boosted switch drive with charge transfer | 10/976196 | |
| | Power conversion integrated circuit and method for programming | 10/946611 | |
| | Method of forming a charge pump controller and structure therefor | 11/996475 | |
| | High voltage sensor device | 11/925017 | |
| | Method of forming a power supply controller and structure therefor | 11/917327 | |
| | Power supply controller and method therefor | 11/917315 | |
| | Single input dual output voltage power supply and method therefor | 11/912795 | |
| | Method of forming an mos transistor and structure therefor | 11/840826 | |
| | DC-DC converter controller having optimized load transient response and method | 11/817766 | |
| | Amplification circuit and method therefor | 11/817392 | |

| Registered Owner | Title | Application # | Patent Recording # |
|------------------|------------------------------------------------------------------------------|---------------|--------------------|
| | Charge pump controller and method therefor | 11/815843 | |
| | Current controller and method therefor | 11/814660 | |
| | LED current controller and method therefor | 11/813985 | |
| | Communication circuit and method therefor | 11/720860 | |
| | DC-to-DC converter and method therefor | 11/576030 | |
| | Electronic package having down-set leads and methods | 11/575204 | |
| | Semiconductor trench having a sealing plug and method | 12/206541 | |
| | Semiconductor device having vertical charge-compensating structure | 12/206516 | |
| | Thinned semiconductor wafer and method of thinning a semiconductor wafer | 12/206043 | |
| | Method of thinning a semiconductor wafer | 12/172075 | |
| | Method of thinning a semiconductor wafer and a semiconductor wafer transport | 12/172013 | |
| | Low clamp voltage ESD device and method therefor | 12/170630 | |
| | Charge pump converter and method therefor | 12/161387 | |
| | Method of forming a bi-directional diode and structure therefor | 12/134401 | |
| | Method of forming an oscillator circuit and structure therefor | 12/126122 | |
| | Transient voltage suppressor and method | 12/116745 | |
| | Method for manufacturing an energy storage device and structure therefor | 12/108361 | |

| Registered Owner | Title | Application # | Patent Recording # |
|----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|---------------|--------------------|
| Semiconductor Components Industries, LLC | Method for adjusting threshold voltage and circuit therefor | 12/098847 | |
| | Method of forming a semiconductor package | 12/098813 | |
| | Method of forming an integrated semiconductor device and structure therefor | 12/208537 | |
| | Semiconductor component and structure therefor | 12/206570 | |
| | Transient voltage suppressor and methods | 12/098369 | |
| | Amplifier circuit and method therefor | 12/091152 | |
| | Charge pump controller and method therefor | 12/090825 | |
| | Method of forming a power supply controller and structure therefor | 12/056531 | |
| | Method of forming a MOS transistor and structure therefor | 12/236718 | |
| | Antenna integrated with retrieval component in a hearing aid | 10/975914 | |
| | Image sensor utilizing dark current canceling feature | 11/544878 | |
| | Method of forming a shielded semiconductor device and structure therefor | 12/170202 | |
| | Direct matched and ultra low power transceiver architecture for wireless medical applications | 60/972341 | |
| | System unit element selection | 12/098357 | |
| Diagnostic and maintenance systems and methods for LED power management circuits | 11/535047 | | |
| Programmable crystal oscillator | 12/045224 | | |
| Current limited voltage supply | 12/196983 | | |

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|------------------------------------------|-----------|--------|------------|-----------|
| Semiconductor Components Industries, LLC | Trademark | ZURIUM | 77/825/219 | 9/11/2009 |
|------------------------------------------|-----------|--------|------------|-----------|

| <u>Registered Owner</u> | <u>Trademark</u> | <u>Application #</u> | <u>Registration #</u> |
|------------------------------------------|--------------------------------|----------------------|-----------------------|
| Semiconductor Components Industries, LLC | GREENPOINT (Class 16) | 77/502,351 | 3,618,590 |
| | GREENPOINT & Design (Class 16) | 77/502,376 | 3,618,591 |