TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Assignment of Security Agreement

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
PNC Bank, National Association		03/06/2013	federally chartered bank: UNITED STATES

RECEIVING PARTY DATA

Name:	Integrian Holdings, LLC
Street Address:	320 N. Jensen Road
City:	Vestal
State/Country:	NEW YORK
Postal Code:	13850
Entity Type:	LIMITED LIABILITY COMPANY: NEW YORK

PROPERTY NUMBERS Total: 10

Property Type	Number	Word Mark
Serial Number:	75333605	DRICLAD
Serial Number:	75844816	HYPERBGA
Serial Number:	76476536	ENDICOTT INTERCONNECT
Serial Number:	76476537	ENDICOTT INTERCONNECT TECHNOLOGIES
Serial Number:	76476538	
Serial Number:	76657204	COREEZ
Serial Number:	76657205	COREEZ
Serial Number:	76700170	
Serial Number:	76700201	EV MICROELECTRONICS
Serial Number:	76700202	ENDICOTT INTERCONNECT EUROPE

OP $265.00 75333605

CORRESPONDENCE DATA

Fax Number: 6077236605

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent

via US Mail.

Phone:	6077235341
Email:	elawson@hhk.com
Correspondent Name:	Erica Lawson - Hinman, Howard & Kattell
Address Line 1:	80 Exchange Street
Address Line 2:	700 Security Mutual Building
Address Line 4:	Binghamton, NEW YORK 13901

NAME OF SUBMITTER:	Erica L. Lawson
Signature:	/Erica L. Lawson/
Date:	03/06/2013

Total Attachments: 119
source=Integrian Holdings General Assignment#page1.tif
source=Integrian Holdings General Assignment#page2.tif
source=Integrian Holdings General Assignment#page3.tif
source=Integrian Holdings General Assignment#page4.tif
source=Integrian Holdings General Assignment#page5.tif
source=Integrian Holdings General Assignment#page6.tif
source=Integrian Holdings General Assignment#page7.tif
source=Integrian Holdings General Assignment#page8.tif
source=Integrian Holdings General Assignment#page9.tif
source=Integrian Holdings General Assignment#page10.tif
source=Integrian Holdings General Assignment#page11.tif
source=Integrian Holdings General Assignment#page12.tif
source=Integrian Holdings General Assignment#page13.tif
source=Integrian Holdings General Assignment#page14.tif
source=Integrian Holdings General Assignment#page15.tif
source=Integrian Holdings General Assignment#page16.tif
source=Integrian Holdings General Assignment#page17.tif
source=Integrian Holdings General Assignment#page18.tif
source=Integrian Holdings General Assignment#page19.tif
source=Integrian Holdings General Assignment#page20.tif
source=Integrian Holdings General Assignment#page21.tif
source=Integrian Holdings General Assignment#page22.tif
source=Integrian Holdings General Assignment#page23.tif
source=Integrian Holdings General Assignment#page24.tif
source=Integrian Holdings General Assignment#page25.tif
source=Integrian Holdings General Assignment#page26.tif
source=Integrian Holdings General Assignment#page27.tif
source=Integrian Holdings General Assignment#page28.tif
source=Integrian Holdings General Assignment#page29.tif
source=Integrian Holdings General Assignment#page30.tif
source=Integrian Holdings General Assignment#page31.tif
source=Integrian Holdings General Assignment#page32.tif
source=Integrian Holdings General Assignment#page33.tif
source=Integrian Holdings General Assignment#page34.tif
source=Integrian Holdings General Assignment#page35.tif
source=Integrian Holdings General Assignment#page36.tif
source=Integrian Holdings General Assignment#page37.tif
source=Integrian Holdings General Assignment#page38.tif

source=Integrian Holdings General Assignment#page39.tif
source=Integrian Holdings General Assignment#page40.tif
source=Integrian Holdings General Assignment#page41.tif
source=Integrian Holdings General Assignment#page42.tif
source=Integrian Holdings General Assignment#page43.tif
source=Integrian Holdings General Assignment#page44.tif
source=Integrian Holdings General Assignment#page45.tif
source=Integrian Holdings General Assignment#page46.tif
source=Integrian Holdings General Assignment#page47.tif
source=Integrian Holdings General Assignment#page48.tif
source=Integrian Holdings General Assignment#page49.tif
source=Integrian Holdings General Assignment#page50.tif
source=Integrian Holdings General Assignment#page51.tif
source=Integrian Holdings General Assignment#page52.tif
source=Integrian Holdings General Assignment#page53.tif
source=Integrian Holdings General Assignment#page54.tif
source=Integrian Holdings General Assignment#page55.tif
source=Integrian Holdings General Assignment#page56.tif
source=Integrian Holdings General Assignment#page57.tif
source=Integrian Holdings General Assignment#page58.tif
source=Integrian Holdings General Assignment#page59.tif
source=Integrian Holdings General Assignment#page60.tif
source=Integrian Holdings General Assignment#page61.tif
source=Integrian Holdings General Assignment#page62.tif
source=Integrian Holdings General Assignment#page63.tif
source=Integrian Holdings General Assignment#page64.tif
source=Integrian Holdings General Assignment#page65.tif
source=Integrian Holdings General Assignment#page66.tif
source=Integrian Holdings General Assignment#page67.tif
source=Integrian Holdings General Assignment#page68.tif
source=Integrian Holdings General Assignment#page69.tif
source=Integrian Holdings General Assignment#page70.tif
source=Integrian Holdings General Assignment#page71.tif
source=Integrian Holdings General Assignment#page72.tif
source=Integrian Holdings General Assignment#page73.tif
source=Integrian Holdings General Assignment#page74.tif
source=Integrian Holdings General Assignment#page75.tif
source=Integrian Holdings General Assignment#page76.tif
source=Integrian Holdings General Assignment#page77.tif
source=Integrian Holdings General Assignment#page78.tif
source=Integrian Holdings General Assignment#page79.tif
source=Integrian Holdings General Assignment#page80.tif
source=Integrian Holdings General Assignment#page81.tif
source=Integrian Holdings General Assignment#page82.tif
source=Integrian Holdings General Assignment#page83.tif
source=Integrian Holdings General Assignment#page84.tif
source=Integrian Holdings General Assignment#page85.tif
source=Integrian Holdings General Assignment#page86.tif
source=Integrian Holdings General Assignment#page87.tif
source=Integrian Holdings General Assignment#page88.tif
source=Integrian Holdings General Assignment#page89.tif
source=Integrian Holdings General Assignment#page90.tif
source=Integrian Holdings General Assignment#page91.tif
source=Integrian Holdings General Assignment#page92.tif
source=Integrian Holdings General Assignment#page93.tif

source=Integrian Holdings General Assignment#page94.tif
source=Integrian Holdings General Assignment#page95.tif
source=Integrian Holdings General Assignment#page96.tif
source=Integrian Holdings General Assignment#page97.tif
source=Integrian Holdings General Assignment#page98.tif
source=Integrian Holdings General Assignment#page99.tif
source=Integrian Holdings General Assignment#page100.tif
source=Integrian Holdings General Assignment#page101.tif
source=Integrian Holdings General Assignment#page102.tif
source=Integrian Holdings General Assignment#page103.tif
source=Integrian Holdings General Assignment#page104.tif
source=Integrian Holdings General Assignment#page105.tif
source=Integrian Holdings General Assignment#page106.tif
source=Integrian Holdings General Assignment#page107.tif
source=Integrian Holdings General Assignment#page108.tif
source=Integrian Holdings General Assignment#page109.tif
source=Integrian Holdings General Assignment#page110.tif
source=Integrian Holdings General Assignment#page111.tif
source=Integrian Holdings General Assignment#page112.tif
source=Integrian Holdings General Assignment#page113.tif
source=Integrian Holdings General Assignment#page114.tif
source=Integrian Holdings General Assignment#page115.tif
source=Integrian Holdings General Assignment#page116.tif
source=Integrian Holdings General Assignment#page117.tif
source=Integrian Holdings General Assignment#page118.tif
source=Integrian Holdings General Assignment#page119.tif

General Assignment

PNC

THIS GENERAL ASSIGNMENT (this "**Assignment**") is made as of March 6, 2013 by PNC Bank, National Association ("**Assignor**"), to Integrian Holdings, LLC, a New York limited liability company ("**Assignee**").

RECITALS

A. Assignor and Assignee are parties to that certain Loan Sale Agreement, dated as of March 6, 2013 (the "**Loan Sale Agreement**"). All capitalized terms not otherwise defined in this Assignment shall have the meanings ascribed to such terms in the Loan Sale Agreement.

B. Pursuant the Loan Sale Agreement, Assignor agreed to sell to Assignee the Loans and the Loan Documents listed on Schedule 1 attached to the Loan Sale Agreement.

C. This Assignment is being delivered by Assignor to Assignee in accordance with and subject to the terms of the Loan Sale Agreement to effect the assignment contemplated thereby.

ASSIGNMENT

NOW, THEREFORE, in consideration of the receipt by Assignor of the payment of the Purchase Price, as provided in the Loan Sale Agreement, Assignor hereby assigns and transfers to Assignee all right, title and interest of Assignor in and to the Loans and the Loan Documents set forth on Schedule 1 attached hereto.

Subject to the terms of the Loan Sale Agreement, Assignee hereby assumes any and all of Assignor's obligations and liabilities under or with respect to the Loans and the Loan Documents including, without limitation, (a) any obligation now existing or hereafter arising to make advances under any of the Loans, and (b) any and all of Assignor's other performance obligations now existing or hereafter arising under the Loan Documents; *provided, however*, with respect to each deposit account control agreement included among the Loan Documents, Seller hereby assigns only its right, title and interest thereunder as lender and secured party, and will retain all of Seller's right, title and interest thereunder as depository.

Except as expressly set forth in Section 6 of the Loan Sale Agreement, neither Assignor nor any of its officers, directors, employees or agents makes any representations or warranties to Assignee or any of its officers, directors, managers, employees or agents, express or implied, in connection with the sale of the Loans and the Loan Documents, this Assignment, or the transactions described in this Assignment or with respect to any Obligor including, without limitation, those regarding, concerning or pertaining to: (i) the validity or enforceability of the Loan Documents; (ii) the collectability of any Loan; (iii) the financial condition of any Obligor; (iv) the existence or nature of any collateral securing any Loan; (v) the existence, validity, perfection or priority of any lien or security interest securing any Loan, whether created (or intended to be created) by the Loan Documents or otherwise; (vi) the marketability, value, or status of title, ownership or possession of any collateral securing any Loan; (vii) the environmental condition of any collateral securing any Loan; (viii) compliance with any applicable rule, law or

regulation of any governmental authority pertaining to any Obligor, any Loan, the Loan Documents, or any collateral securing any Loan including, without limitation, the Equal Credit Opportunity Act, 15 U.S.C. § 1691 et seq., the Real Estate Settlement and Procedures Act, 12 U.S.C. § 2601 et seq., the Fair Housing Act, 42 U.S.C. § 3601 et seq., the Fair Debt Collections Practices Act,15 U.S.C. § 1692 et seq., the Fair Credit Reporting Act, 15 U.S.C. § 1681 et seq., the Gramm-Leach-Bliley Act, Pub.L. 106-102, 113 stat. 1338, enacted November 12, 1999, and/or Regulations AA, B and/or Z of the Board of Governors of the Federal Reserve System, (ix) the existence or basis for any claim, counterclaim, defense, or offset relating to any Loan or the Loan Documents; (x) the future performance of any Obligor; or (xi) any facts or matters relating or pertaining to any of the foregoing. WITHOUT LIMITING THE FOREGOING, THIS ASSIGNMENT AND THE ASSIGNMENT, SALE AND TRANSFER OF THE LOANS AND THE LOAN DOCUMENTS TO ASSIGNEE ARE MADE WITHOUT RECOURSE OF ANY KIND TO ASSIGNOR, AND ARE MADE ON AN "AS IS", "WHERE IS" BASIS, "WITH ALL FAULTS" AND WITHOUT ANY REPRESENTATIONS OR WARRANTIES, EXPRESS OR IMPLIED, OF ANY KIND OR NATURE WHATSOEVER BY ASSINGOR, OTHER THAN THE SPECIFIC REPRESENTATIONS AND WARRANTIES EXPRESSLY SET FORTH IN SECTION 6 OF THE LOAN SALE AGREEMENT.

Assignor restates each of the representations and warranties of Assignor under the Loan Sale Agreement as if fully set forth herein, and hereby represents and warrants to Assignee that each of the representations and warranties of Assignor set forth in the Loan Sale Agreement are true and correct.

Assignee restates each of the representations, warranties and acknowledgments of Assignee under the Loan Sale Agreement as if fully set forth herein, and hereby represents and warrants to Assignor that each of the representations and warranties of Assignee set forth in the Loan Sale Agreement are true and correct.

Assignor hereby authorizes Assignee to file (on behalf of Assignor) one or more financing statement amendments pursuant to the applicable Uniform Commercial Code reflecting the assignment of all financing statements included among the Loan Documents from Assignor to Assignee.

Nothing in this Assignment shall be construed to be a modification of or limitation on any provision of the Loan Sale Agreement, including the representations, warranties and covenants set forth therein.

This Assignment is being delivered pursuant and subject to all of the terms and conditions of the Loan Sale Agreement. To the extent that there is any conflict between the terms of this Assignment and the terms of the Loan Sale Agreement, the terms of the Loan Sale Agreement shall prevail.

This Agreement has been negotiated in and shall be governed by and construed and enforced in accordance with the laws of the Commonwealth of Pennsylvania without regard to the principles thereof relating to conflict of laws.

ASSIGNOR AND ASSIGNEE, ON BEHALF OF THEMSELVES AND THEIR SUCCESSORS AND ASSIGNS, AGREE THAT ANY SUIT, ACTION OR PROCEEDING, WHETHER CLAIM OR COUNTERCLAIM, BROUGHT OR INSTITUTED BY OR AGAINST ANY PARTY HERETO OR ANY SUCCESSOR OR ASSIGN OF ANY PARTY HERETO, ARISING OUT OF OR IN ANY WAY RELATING TO THIS ASSIGNMENT, OR ANY FACTS OR CIRCUMSTANCES IN WHICH THIS ASSIGNMENT IS INVOLVED IN ANY WAY,

SHALL BE TRIED ONLY BY A COURT AND NOT BY A JURY. EACH PARTY HERETO KNOWINGLY, VOLUNTARILY AND INTENTIONALLY WAIVES ANY RIGHT TO A TRIAL BY JURY IN ANY SUCH SUIT, ACTION OR PROCEEDING. EACH OF THE PARTIES HERETO REPRESENTS AND WARRANTS THAT THIS WAIVER OF THE RIGHT TO A JURY TRIAL HAS BEEN MADE AFTER CONSULTATION WITH LEGAL COUNSEL.

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument.

IN WITNESS WHEREOF, the undersigned have caused this General Assignment to be executed as a document under seal of the date and year first written above.

WITNESS / ATTEST:

Print Name: L E DAVIS
Title:_____
(Include title only if an officer of entity signing to the right)

INTEGRIAN HOLDINGS, LLC

By:_____ (SEAL)
Print Name: JAMES T. MATTHEWS
Title: MEMBER

PNC BANK, NATIONAL ASSOCIATION

By:_____ (SEAL)
Print Name:_____
Title:_____

ANY PARTY HERETO OR ANY SUCCESSOR OR ASSIGN OF ANY PARTY HERETO, ARISING OUT OF OR IN ANY WAY RELATING TO THIS ASSIGNMENT, OR ANY FACTS OR CIRCUMSTANCES IN WHICH THIS ASSIGNMENT IS INVOLVED IN ANY WAY, SHALL BE TRIED ONLY BY A COURT AND NOT BY A JURY. EACH PARTY HERETO KNOWINGLY, VOLUNTARILY AND INTENTIONALLY WAIVES ANY RIGHT TO A TRIAL BY JURY IN ANY SUCH SUIT, ACTION OR PROCEEDING. EACH OF THE PARTIES HERETO REPRESENTS AND WARRANTS THAT THIS WAIVER OF THE RIGHT TO A JURY TRIAL HAS BEEN MADE AFTER CONSULTATION WITH LEGAL COUNSEL.

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument.

IN WITNESS WHEREOF, the undersigned have caused this General Assignment to be executed as a document under seal of the date and year first written above.

WITNESS / ATTEST:

INTEGRIAN HOLDINGS, LLC

_____

Print Name:_____
Title:_____
(Include title only if an officer of entity signing to the right)

By:_____ (SEAL)
Print Name:_____
Title:_____

PNC BANK, NATIONAL ASSOCIATION

By:_____ (SEAL)
Print Name: PATRICK M. CORNISH
Title: VP

[General Assignment]

SCHEDULE 1

[ATTACH SCHEDULE 1 TO LOAN SALE AGREEMENT]

	Revolving Credit Note 2.10.12 $50,000,000	Original
Stock Certificate	**Endicott Interconnect Technologies, Inc.**	
	Douglas Matthews 3,952 Shares	Original
	Thomas Davis 1,563 Shares	Original
	Christopher Mellon 781 Shares	Original
	Lawrence Davis 1,726 Shares	Original
	Theresa Matthews 1,978 Shares	Original
	William Maines 10,500 Shares	Original
	David Maines 10,500 Shares	Original
	James F Matthews 1,731 Shares	Original
	Judith Matthews 1,731 Shares	Original
	James T Matthews 3,952 Shares	Original
	James Orband 1,563 Shares	Original
	John Matthews 3,952 Shares	Original
	Robert Matthews 1,978 Shares	Original
	Endicott Medtech, Inc.	
	Endicott Interconnect Technologies, Inc. 100 Shares	Original
Stock Power		
	Rober Matthews	Original
	John Matthews	Original
	Endicott Interconnect Technologies, Inc.	Original
	Theresa Matthews	Original
	Douglas Matthews	Original
	James Matthews	Original
	David Maines	Original
	William Maines	Original
	Lawrence Davis	Original
	Thomas Davis	Original
	Christopher Mellon	Original
	James Orband	Original
	Collateral Pledge Agreement 2.10.12 Endicott	Original
	Collateral Pledge Agreement 2.10.12 Owners	Original
	Capital Call Agreement 2.10.12	Original
	Revolving Credit and Security Agreement 2.10.12	Original
	Trademark and Patent Security Agreement 2.10.12	Original
	HHK Letter on Credit and Secuirty Agreement 2.10.12	Original
	Counsel's Memorandum - Blank Rome 2.10.12	Original
	Subordination Agreement 2.10.12 - Huron	Original
	Subordination Agreement 2.10.12 - Endicott	Original
	UCCs	Copies
	Landlord's Waiver and Consent	Original
	Financial Condition Certificate	Original
	Power of Attorney	Original
	Officer's Certificate	Original
	Borrowing Request and Disbursement	Original
	Blocked Accoutn Control Agreement JPMorgan Chase	Original

TRADEMARK AND PATENT SECURITY AGREEMENT

THIS TRADEMARK AND PATENT SECURITY AGREEMENT (the "Agreement") made as of this February 10, 2012 by **ENDICOTT INTERCONNECT TECHNOLOGIES, INC.**, a New York corporation ("Endicott"), **EI TRANSPORTATION COMPANY LLC**, a Delaware limited liability company ("EI Transport"), **ENDICOTT MEDTECH, INC.**, a New York corporation ("Medtech," together with Endicott and EI Transport, collectively, the "Grantor"), in favor of **PNC BANK, NATIONAL ASSOCIATION**, in its capacity as agent ("Agent") for the Lenders.

WITNESSETH

WHEREAS, Grantor (together with each Person joined as borrower to the Loan Agreement from time to time, collectively the "Borrowers") has entered into that certain Revolving Credit and Security Agreement with Agent and the financial institutions party thereto from time to time as lenders (the "Lenders") dated as of the date hereof (as same may be amended, restated, supplemented or modified from time to time, the "Loan Agreement") providing for the extensions of credit to be made to Borrowers by Lenders;

WHEREAS, Grantor has granted to Agent, for the benefit of Lenders, a security interest in all of the assets of Grantor including all right, title and interest of Grantor in, to and under all now owned and hereafter acquired trademarks and patents, together with the goodwill of the business symbolized by Grantor's trademarks and patents and all products and proceeds thereof, to secure the payment of all amounts owing by Borrowers and guarantors under the Loan Agreement;

NOW, THEREFORE, in consideration of the premises set forth herein and for other good and valuable consideration, receipt and sufficiency of which are hereby acknowledged, Grantor agrees as follows:

1. Incorporation of Loan Agreement. The Loan Agreement and the terms and provisions thereof are hereby incorporated in their entirety by this reference. Capitalized terms used herein and not otherwise defined herein shall have the meanings ascribed to them in the Loan Agreement.

2. Grant and Reaffirmation of Grant of Security Interests. To secure the payment and performance of the Obligations under the Loan Agreement, Grantor hereby grants to Agent, for its benefit and the benefit of Lenders, and hereby reaffirms its grant pursuant to the Loan Agreement of a continuing security interest in Grantor's entire right, title and interest in and to the following, whether now owned or existing or hereafter created, acquired or arising:

(i) each trademark, trademark application, patent and patent application listed on Schedule 1 annexed hereto (such trademarks and trademark applications, the "Trademarks" and such patents and patent applications, the "Patents"), together with any reissues, continuations or extensions thereof, and all of the goodwill of the business connected with the use of, and symbolized by, each Trademark; and

(ii) all products and proceeds of the forgoing, including without limitation, any claim by Grantor against third parties for past, present or future (a) infringement or dilution of any Trademark or Patent, or (b) injury to the goodwill associated with any Trademark.

3. Covenants. Grantor agrees not to sell, grant any option, assign, license (other than in the ordinary course of business) or further encumber its rights and interest in the Trademarks or Patents without prior written consent of Agent.

4. Representations and Warranties. Grantor hereby represents and warrants that the Trademarks and Patents listed on Schedule I attached hereto constitute all trademarks, trademark applications, patents and patent applications owned or registered to Grantor as of the date of this Agreement.

5. Termination. This Agreement shall continue in effect until all of the Obligations are indefeasibly paid and satisfied in full and the Loan Agreement is terminated.

[signatures to appear on following page]

IN WITNESS WHEREOF, Grantor has duly executed this Agreement as of the date first written above.

ENDICOTT INTERCONNECT TECHNOLOGIES, INC.

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

ENDICOTT MEDTECH, INC.

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

EI TRANSPORTATION COMPANY, LLC

By: Endicott Interconnect Technologies, Inc., its sole member

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

Agreed and Accepted
As of the Date First Written Above

PNC BANK, NATIONAL ASSOCIATION,
as Agent

By: _____
Name: Ronald Heiken
Title: Vice President

[SIGNATURE PAGE TO TRADEMARK AND PATENT SECURITY AGREEMENT]

COMPANY ACKNOWLEDGMENT

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6th day of February, 2012, by William Lynn as CFO of Endicott Interconnect Technologies, Inc.

ANN B. CIANFLONE
Notary Public, State of New York
[Seal] No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/ 2013

Notary Public, State of New York
My commission expires on 2/13/2013

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6 day of February, 2012, by William Lynn as CFO of EI Transportation Company, LLC.

ANN B. CIANFLONE
Notary Public, State of New York
[Seal] No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/ 2013

Notary Public, State of New York
My commission expires on 2/13/2013

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6 day of February, 2012, by William Lynn as CFO of Endicott Medtech, Inc.

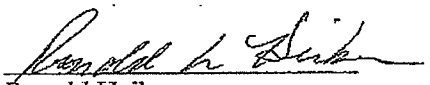
ANN B. CIANFLONE
Notary Public, State of New York
[Seal] No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/ 2013

Notary Public, State of New York
My commission expires on 2/13/2013

[ACKNOWLEDGEMENT TO TRADEMARK AND PATENT SECURITY AGREEMENT]

Agreed and Accepted
As of the Date First Written Above

PNC BANK, NATIONAL ASSOCIATION,
as Agent

By: 
Name: Ronald Heiken
Title: Vice President

[SIGNATURE PAGE TO TRADEMARK AND PATENT SECURITY AGREEMENT]

SCHEDULE 1

TRADEMARK REGISTRATIONS

Trademark/Service Mark	Country	Filing Date	Application No.	Registration No.	Registration Date	Status
COREEZ	US	3/24/2006	76/657,204	3,619,679	5/12/2009	Registered
CoreEZ	US	3/24/2006	76/657,205	3,564,994	1/20/2009	Registered
DRICLAD	US	7/31/1997	75/333,605	2,594,509	7/16/2002	Registered
DRICLAD	Australia	1/14/1998	752680	752680	7/1/1998	Dead
DRICLAD	Brazil	1/22/1998	820508039	820508039	1/27/2009	Registered
DRICLAD	Canada	11/27/1997	862725			Dead
DRICLAD	China		9800105902	1435500	8/21/2000	Dead
DRICLAD	France	5/9/2000		000721563	7/23/2001	
DRICLAD	Japan	11/14/1997	H09-177086	4245007	2/26/1999	Registered
DRICLAD	Korea	9/10/1998	1998-0023497	456079	9/29/1999	Registered
DRICLAD	Malaysia			98011217		Dead
DRICLAD	Mexico	1/30/1998		572577		Dead
DRICLAD	Mexico	1/30/1998		572578		Dead
DRICLAD	Philippine		4-1998-07682			Dead
DRICLAD	Switzerland			465915		Dead
DRICLAD	Taiwan			00108344		Registered
DRICLAD	Taiwan			00896915		Registered
DRICLAD	Thailand	10/6/1998	371207	KOR128454	2/15/2001	
Endicott Interconnect	US	12/16/2002	76/476,536	2,831,497	4/13/2004	Registered
Endicott Interconnect Europe	US	11/2/2009	76/700,202			Dead
Endicott Interconnect Technologies	US	12/16/2002	76/476,537	2,829,453	4/6/2004	Registered
eV Microelectronics	US	11/2/2009	76/700,201			Dead
HYPERBGA	US	11/9/1999	75/844,816	2,632,339	10/8/2002	Registered

Trademark/Service Mark	Country	Filing Date	Application No.	Registration No.	Registration Date	Status
HYPERBGA	Australia	2/24/2000	824959	824959	2/16/2001	Registered
HYPERBGA	Canada	8/10/2004	1226508	TMA642449	6/20/2005	Registered
HYPERBGA	Canada		1044049			Dead
HYPERBGA	China	6/6/2000	2000079269	1622402	8/21/2001	Registered
HYPERBGA	France	5/9/2000	1645605	001645605	7/23/2001	
HYPERBGA	Japan		2000-004060	4472510		Registered
HYPERBGA	Korea	11/29/1999	1999-0045422	488735	2/9/2001	Dead
HYPERBGA	Singapore		TOO/10304A	T00/10304A	6/14/2000	Registered
HYPERBGA	Switzerland			477543		Registered
HYPERBGA	Taiwan			00950034		Registered
HYPERBGA	Europe	5/9/2000	1645605	1645605	7/23/2001	Registered
EI Design	US	12/16/2002	76/476,538	2,829,454	4/6/2004	Dead
EI 3-D Design	US	11/2/2009	76/700,170			Dead

PATENT REGISTRATIONS

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-02-001				METHOD TO QUANTIFY COPPER THICKNESS	J. Rios et al							
1-02-002	2-03-002	United States	[redacted]	CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	F. Egitto V. Markovich T. Miller	2/24/2003	10/370,529	2004-0163964	6/14/2005	6,905,589		Issued
	CA-2-03-002	Canada		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	F. Egitto V. Markovich T. Miller		2452178			2,452,178		Issued
	EP-2-03-002	Europe		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	F. Egitto V. Markovich T. Miller							Abandoned
	JP-2-03-002	Japan		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	F. Egitto V. Markovich T. Miller		2004-038077					Abandoned
	TW-2-03-002	Taiwan		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	F. Egitto V. Markovich T. Miller		93103039					Issued
1-02-003	2-02-001	US		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich	12/19/2002	10/322,527	2004-0118596	10/26/2004	6,809,269		Issued

SCHEDULE -1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	CA-2-02-001	Canada		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich		2452178			2,452,178		Issued
	CN-2-02-001	China		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich		200310123253.X					Issued
	EP-2-02-001	Europe		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich		3257866.8					Abandoned
	JP-2-02-001	Japan		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich		2003-416107					Abandoned
	TW-2-02-001	Taiwan		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich		92134417					Issued
	2-02-001-CIP	US		INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE	J. Fuller J. Lauffer V. Markovich	3/6/2003	10/379,575	2004-0118598	3/29/2005	6,872,894		Issued
	2-02-001-CIPD	US		INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED	J. Fuller J. Lauffer V. Markovich	9/3/2004	10/933,260	2005-0023035	5/31/2005	6,900,392		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	P.R.	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SUBSTRATE								
	2-02-001D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY	J. Fuller J. Lauffer V. Markovich	3/30/2004	10/811,915	2004-0177998	5/23/2006	7,047,630		Issued
	2-02-001D2	US		CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	J. Fuller J. Lauffer V. Markovich	8/11/2004	10/915,483	2005-0011670	7/4/2006	7,071,423		Issued
	2-02-001D3	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY	J. Fuller J. Lauffer V. Markovich	2/9/2006	11/349,998	2006-0123626	3/18/2008	7,343,674		Issued
1-02-004	**ON HOLD**			PCB DUAL STRESS PROCESS	K. Knadle et al							On Hold
1-02-005	**2-03-001**	US		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas	1/30/2003	10/354,000	2004-0150969	12/7/2004	6,828,514		Abandoned
	CA-2-03-001	Canada		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas		2454289			2,454,289		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	EP-2-03-001	Europe		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas		4250455.5					Abandoned
	JP-2-03-001	Japan		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas		2004-007899					Abandoned
	TW-2-03-001	Taiwan		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas		93101219					Issued
	2-03-001-CIP1	US		MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich	3/24/2003	10/394,107	2004-0150114	4/25/2006	7,035,113		Issued
	EI-CA-2-03-001-CIP1	Canada		MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		2454971					Abandoned

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	EI-EP-2-03-001-CIP1	Europe		MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		4250436.5					Abandoned
	EI-JP-2-03-001-CIP1	Japan		MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		2004-21260					Abandoned
	EI-TW-2-03-001-CIP1	Taiwan		MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich	1/16/2004	93101217					Issued
	2-03-001-CIP2	US		INFORMATION HANDLING SYSTEM	L. Fraley V. Markovich	3/24/2003	10/394,135	2004-0150101	4/4/2006	7,023,707		Issued
	2-03-001D	US		METHOD OF MAKING HIGH SPEED CIRCUIT BOARD	B. Chan J. Lauffer H. Lin V. Markovich D. Thomas	3/30/2004	10/811,817	2004-0231888	12/26/2006	7,152,319		Issued
1-02-006	**ON HOLD**			CIRCUIT LINE PEEL TEST METHOD	D. Alcoe et al							
1-02-007	**2-03-007**	US		METHOD OF TESTING SPACINGS IN PATTERN OF	J. Durkot	7/11/2003	10/616,932	2005-0005438	3/21/2006	7,013,563		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				OPENINGS IN PCB CONDUCTIVE LAYER								
1-02-008	2-03-003	US		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge	4/9/2003	10/409,066	2004-0201136	10/25/2005	6,958,106		Issued
	CA-2-03-003	Canada		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge		2460577					Pending
	EP-2-03-003	Europe		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge							Abandoned
	JP-2-03-003	Japan		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge		2004-084492					Abandoned
	TW-2-03-003	Taiwan		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge		93108328					Issued
	2-03-003C	US		MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	T. Antesberger J. Kresge	6/13/2005	11/150,198	2005-0224167	2/6/2007			Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-001	2-03-011	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE	T. Antesberger J. Fuller J. Konrad J. Kresge S. Krasniak T. Wells	10/7/2003	10/679,302	2005-0074924	8/1/2006	7,084,014		Issued
	2-03-011D1	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE	T. Antesberger J. Fuller J. Konrad J. Kresge S. Krasniak T. Wells	10/26/2005	11/258,092	2006-0040426	1/16/2007	7,163,847		Issued
	2-03-011D2	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE	T. Antesberger J. Fuller J. Konrad J. Kresge S. Krasniak T. Wells	10/27/2005	11/259,043	2006-0046462	8/15/2006	7,091,066		Issued
1-03-002	ON HOLD			LASER REMOVAL OF SOLDERMASK AND CIRCUITRY AFTER PLATING	Antesberger et al							On Hold
1-03-003	ON HOLD			LASER REMOVAL OF SOLDERMASK AND CIRCUITRY AFTER PLATING	Antesberger et al							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-004	**ON HOLD**			VEHICLE ANTI-ACCELERATIO N STRUCTURE AND METHOD	G. Ashton et al							On Hold
1-03-005	**ON HOLD**			CONDUCTIVE SHEET PERSONALIZAT ION PROCESS	A. Bhatt et al							On Hold
1-03-006	**2-03-010**			SOFTWARE FOR FLEX MAKING EQUIPMENT	P. Lulkoski et al							On Hold
1-03-007	**2-03-009**	US		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	E. Foster G. Kevern A. Sargent	8/20/2003	10/643,909	2005-0039840	6/20/2006	7,063,762		Issued
	2-03-009D	US		CIRCUITIZED SUBSTRATE WITH CONDUCTIVE POLYMER AND SEED MATERIALS ADHESION LAYER	E. Foster G. Kevern A. Sargent	10/5/2005	11/242,841	2006-0029781	2/19/2008	7,332,212		Issued
1-03-008	**ON HOLD**			SOLDER BALL FORMATION PROC. AND PROD. RESULTING THEREFROM	D. Alcoe et al							On Hold
1-03-009	**ON HOLD**			LASER DRILLED BLIND VIA W/INTERSTITIA L ELECTRICAL CONNECTION	J. Larnerd et al							On Hold
1-03-010	**2-03-008**	US		ELECTRONIC COMPONENT TEST	D. Alcoe	7/31/2003	10/630,722	2005-0022376	9/19/2006	7,109,732		Issued

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				APPARATUS								
	CA-2-03-008	Canada		ELECTRONIC COMPONENT TEST APPARATUS	D. Alcoe		2475195					Abandoned
	EP-2-03-008	Europe		ELECTRONIC COMPONENT TEST APPARATUS	D. Alcoe							Abandoned
	JP-2-03-008	Japan		ELECTRONIC COMPONENT TEST APPARATUS	D. Alcoe							Abandoned
	TW-2-03-008	Taiwan		ELECTRONIC COMPONENT TEST APPARATUS	D. Alcoe							Abandoned
1-03-011	2-03-006	US		ELECTRONIC CARD	J. McNamara J. Fuller J. McNamara W. Wike	6/2/2003	10/449,019	2004-0242270				Abandoned
	CA-2-03-006	Canada		ELECTRONIC CARD	J. McNamara J. Fuller J. McNamara W. Wike		2465137					Abandoned
	EP-2-03-006	Europe		ELECTRONIC CARD	J. McNamara J. Fuller J. McNamara W. Wike							Abandoned

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	JP-2-03-006	Japan		ELECTRONIC CARD	J. McNamara J. Fuller J. McNamara W. Wike		2004-149093					Abandoned
	TW-2-03-006	Taiwan		ELECTRONIC CARD	J. McNamara J. Fuller J. McNamara W. Wike		93114136					Pending
1-03-012	2-03-004-CIP	US		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe	4/28/2003	10/423,877	2004-0183212	11/9/2004	6,815,837		Issued
	CA-2-03-004-CIP	Canada		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe		2458438					Abandoned
	EP-2-03-004-CIP	Europe		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe		4250754.1					Pending
	JP-2-03-004-CIP	Japan		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe		2004-057058					
	TW-2-03-004-CIP	Taiwan		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe		93103172					Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-012	US		ELECTRONIC PACKAGE WITH CONDUCTIVE PAD CAPABLE OF WITHSTANDING SIGNIFICANT LOADS AND INFORMATION HANDLING SYSTEM UTILIZING SAME	D. Alcoe	6/16/2004	10/868,066	2004-0238970				Abandoned
	2-03-005-CIP	US		PINNED ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	D. Alcoe	4/28/2003	10/423,972	2004-082604	8/8/2006	7,087,846		Issued
1-03-013				METHOD OF MAKING POWER CORE	M. Wozniak et al							
1-03-014	ON HOLD			TEMPORARY FLEXIBLE SUBSTRATE STIFFENER	D. Alcoe							On Hold
1-03-015	ON HOLD			NOVEL RESISTOR STRUCTURE	A. Sargent							On Hold
1-03-016	ON HOLD			NANOTUBE CAPACITOR STRUCTURE	A. Sargent							On Hold
1-03-017	ON HOLD			CAPACITOR WITH SOL-GEL MATRIX	A. Sargent							On Hold
1-03-018	ON HOLD			POLYMER WIRE AND NANOTUBE RESISTOR	A. Sargent							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-019	ON HOLD			CONDUCTIVE POLYMER CAPACITOR	A. Sargent							On Hold
1-03-020	ON HOLD			LCP DIELECTRIC CARRIER	D. Farquhar et al							On Hold
1-03-021	2-05-002	US		ELECTRONIC CARD ASSEMBLY	B. Chan H. Lin V. Markovich R. Smith	3/23/2005	11/086,324	2006-0213973	10/28/2008	7,441,709		Issued
1-03-022	ON HOLD			ELECTRONIC CARD WITH BUILT-IN WRITER	H. Lin et al							On Hold
1-03-023	ON HOLD			VEHICLE ALARM SYSTEM	J. Martin							On Hold
1-03-024	ON HOLD			RESIDUAL SOLDER REMOVAL APPARATUS AND METHOD	S. Anson et al							On Hold
1-03-025	ON HOLD			IMPROVED WIREBOND PAD PACKAGE AND METHOD OF MAKING	J. Konrad et al							On Hold
1-03-026	ON HOLD			BIOMETRIC ELECTRONIC DEVICE	A. Bhatt et al							On Hold
1-03-027	ON HOLD			PCB COMPENSATION GRID SOFTWARE	P. Lulkoski et al							On Hold
1-03-028	ON HOLD			BIOLOGICAL SOUND DETECTION DEVICE	A. Bhatt et al							On Hold
1-03-029	ON HOLD			MEDICAL	A. Bhatt et al							On

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				DEVICE								Hold
1-03-030	**2-04-003**	US		CIRCUITIZED SUBSTRATE	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas	3/31/2004	10/812,890	2005-0224985	7/18/2006	7,078,816		Issued
	EP-2-04-003	Europe		CIRCUITIZED SUBSTRATE	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas		5251748.9					Pending
	JP-2-04-003	Japan		CIRCUITIZED SUBSTRATE	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas		2005-097961					Abandoned
	TW-2-04-003	Taiwan		CIRCUITIZED SUBSTRATE	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas		94108414					Abandoned
	2-04-003D1	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas	2/9/2006	11/349,990	2006-0131755	8/26/2008	7,416,996		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-003D2	US		INFORMATION HANDLING SYSTEM UTILIZING A CIRCUITIZED SUBSTRATE HAVING A DIELECTRIC LAYER WITHOUT CONTINUOUS FIBERS	R. Japp V. Markovich C. Palomaki K. Papathomas D. Thomas	2/10/2006	11/350,777	2006-0125103	3/24/2009	7,508,076		Issued
	2-04-005	US		DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES	R. Japp K. Papathomas	3/31/2004	10/812,889	2008-0008727	9/18/2007	7,270,845		Issued
	EP-2-04-005	Europe		DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES	R. Japp K. Papathomas		5251747.1					Pending
	JP-2-04-005	Japan		DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES	R. Japp K. Papathomas		2005-088940					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	TW-2-04-005	Taiwan		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp K. Papathomas		94108442					Pendi g
	2-04-005D	US		CIRCUITIZED SUBSTRATE WITH DIELECTRIC LAYER HAVING DIELECTRIC COMPOSITION NOT INCLUDING CONTINUOUS OR SEMI-CONTINUOUS FIBERS	R. Japp K. Papathomas	9/6/2007	11/896,786	2008-0003407				Pendin g
1-03-031	**2-03-001-CIP3**	US		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich	9/15/2003	10/661,616	2004-0150095	1/31/2006	6,992,896		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	CA-2-03-001-CIP3	Canada		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich	8/16/8621						Pending
	EP-2-03-001-CIP3	Europe		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		4250437.3					Abandoned
	JP-2-03-001-CIP3	Japan		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		2004-022066					Abandoned
	TW-2-03-001-CIP3	Taiwan		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich		93101178					Issued
	2-03-001-CIP3C	US		STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	L. Fraley V. Markovich	9/30/2005	11/238,960	2006-0023439	1/9/2007	7,161,810		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-03-001-CIP3CD	US		METHOD OF MAKING A MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER	L. Fraley V. Markovich	6/19/2006	11/455,183	2006-0240594	2/23/2010	7,665,207		Issued
1-03-032	**ON HOLD**			CHIP-FLEX ATTACHMENT TOOL	D. Alcoe et al							On Hold
1-03-033	**2-04-011**	US		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILITIZING SAME	S. Desai H. Lin j. Lauffer V. Markovich D. Thomas	7/28/2004	10/900,385	2006-0022303	8/7/2007	7,253,502		Issued
	CN-2-04-011	China		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION	D. Thomas et al		200510084168.6					Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				HANDLING SYSTEM UTILIZING SAME								
	EP-2-04-011	Europe		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME			5254523.3					Abandoned
	IN-2-04-011	India		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM			1329/DEL/2005					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME								
	JP-2-04-011	Japan		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME			2005-209452					Abandoned
	TW-2-04-011			CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM	D. Thomas et al		94124018					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME								
	2-04-011D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE	S. Desai H. Lin j. Lauffer V. Markovich D. Thomas	6/12/2007	11/808,596	2007-0249089	2/5/2008	7,326,643		Issued
	EP-2-04-011D	Europe		CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	S. Desai H. Lin j. Lauffer V. Markovich D. Thomas		8012912.5					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-034	**2-04-014**	US		ELECTRICAL ASSEMBLY WITH INTERNAL MEMORY CIRCUITIZED SUBSTRATE HAVING ELECTRONIC COMPONENTS POSITIONED THEREON, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	F. Egitto J. Lauffer H. Lin V. Markovich D. Thomas	7/28/2004	10/900,386	2006-0022310	5/16/2006	7,045,897		Issued
1-03-035	**2-04-001**	US		METHOD OF MAKING PRINTED CIRCUIT BOARD WITH ELECTROPLATED CONDUCTIVE THROUGH HOLES AND BOARD RESULTING THEREFROM	R. Edwards	1/15/2004	10/757,586	2005-0157475				Abandoned
1-03-036	**ON HOLD**			ENHANCED PLATING PROCESS - REDUCED CURRENT DENSITY	R. Edwards							On Hold
1-03-037	**ON HOLD**			PCB WITH ROUNDED	T. Miller et al							On Hold

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				CIRCUIT LINES								
1-03-038	**ON HOLD**			PROCESS TO MAKE PCB WITH ROUNDED CIRCUIT LINES	T. Miller et al							On Hold
1-03-039	**ON HOLD**			HIGH FREQUENCY PRINTED CIRCUIT BOARD	F. Egitto							On Hold
1-03-040	**2-07-011**	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks	10/9/2007	11/907,006	2009-0092353	6/2/2009	7,541,058		Issued
	CN-2-07-011	China		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		200810168239.4					Pending
	EP-2-07-011	Europe		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		8253281.3					Abandoned

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	JP-2-07-011	Japan		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		2008-257667					Abandoned
	2-07-014	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks	10/19/2007	11/907,004	2009-0093073	5/11/2010	7,713,767		Issued
	CN-2-07-014	China		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		200810168238.X					Pending
	EP-2-07-014	Europe		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		8253280.5					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	JP-2-07-014	Japan		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	B. Chan H. Lin R. Magnuson V. Markovich M. Poliks		2008-258491					Abandoned
1-03-041	2-07-012	US		CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL ASSEMBLY UTILIZING SAME	B. Chan F. Egitto H. Lin R. Magnuson V. Markovich D. Thomas	10/25/2007	11/976,468	2009-0109624	6/15/2010	7,738,249		Issued
	CN-2-07-012	China		CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL ASSEMBLY UTILIZING SAME	B. Chan F. Egitto H. Lin R. Magnuson V. Markovich D. Thomas		200810171145.2					Pending
	EP-2-07-012	Europe		CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL	B. Chan F. Egitto H. Lin R. Magnuson V. Markovich D. Thomas		8253371.2					Abandoned

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				ASSEMBLY UTILIZING SAME								
	JP-2-07-012	Japan		CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL ASSEMBLY UTILIZING SAME	B. Chan F. Egitto H. Lin R. Magnuson V. Markovich D. Thomas		2008-262323					Abandoned
1-03-042	**ON HOLD**			WIRELESS REFRIGERATOR UNIT	A. Bhatt et al							On Hold
1-03-043	**2-03-012**	US		ITEM IDENTIFICATION CONTROL METHOD	A. Bhatt M. Hills J. McNamara C. Tiberia	12/22/2003	10/740,500	2005-0137890	9/21/2010	7,801,833		Issued
1-03-044	**2-04-004**	US		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING	I. Memis K. Papathomas	8/18/2004	10/920,235	2005-0224251	12/5/2006	7,145,221		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SYSTEM UTILIZING SAME								
	2-04-007	US		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp I. Memis K. Papathomas	3/23/2005	11/086,323	2005-0218524	12/30/2008	7,470,990	10/7/2024	Issued (CIP of EI-2-04-003)
	CN-2-04-007	China		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING	R. Japp I. Memis K. Papathomas		200610057200.6					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME								
	EP-2-04-007	Europe		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp I. Memis K. Papathomas		6251492.2					Pending
	IN-2-04-007	India		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY	R. Japp I. Memis K. Papathomas		355/DEL/2006					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME								
	TW-2-04-007	Taiwan		LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp I. Memis K. Papathomas		95108059					Pending
	2-04-007D	US		METHOD OF MAKING SAME LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION	R. Japp I. Memis K. Papathomas	4/5/2007	11/730,942	2007-0182016	8/26/2008	7,416,972		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-045	2-07-016	US		METHOD OF MAKING CIRCUITIZED SUBSTRATES HAVING FILM RESISTORS AS PART THEREOF	F. Egitto J. Kresge J. Lauffer	1/16/2008	12/007,820	2009-0178271				Pending
1-03-046	2-05-020	US		CIRCUITIZED SUBSTRATE WITH SHIELDED SIGNAL LINES AND PLATED-THRU-HOLES AND METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	B. Chan F. Egitto R. Magnuson V. Markovich D. Thomas	4/11/2006	11/401,401	2006-0214010	3/16/2010	7,679,005		Issued
1-03-047	2-05-022	US		METHOD OF MAKING PRINTED CIRCUIT BOARD WITH VARYING DEPTH CONDUCTIVE HOLES ADAPTED FOR RECEIVING PINNED ELECTRICAL COMPONENTS	N. Card B. Chan R. Day J. Lauffer R. Magnuson V. Markovich	1/19/2006	11/334,445	2006-0121722				Pending

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-048	**2-03-013**	US		PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	J. Lauffer V. Markovich J. McNamara D. Thomas	12/22/2003	10/740,398	2005-0133257	2/13/2007	7,176,383		Issued
	EP-2-03-013	Europe		PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	J. Lauffer V. Markovich J. McNamara D. Thomas		4257721.3					Pending
	JP-2-03-013	Japan		PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	J. Lauffer V. Markovich J. McNamara D. Thomas		2004-349471					Pending
	TW-2-03-013	Taiwan		PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	J. Lauffer V. Markovich J. McNamara D. Thomas		93138054					Pending
	2-03-013D	US		METHOD OF MAKING A PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	J. Lauffer V. Markovich J. McNamara D. Thomas	12/6/2006	11/634,287	2007-0089290	5/12/2009	7,530,167		Issued
	2-03-014	US		METHOD OF MAKING MULTILAYERED PRINTED CIRCUIT BOARD WITH FILLED CONDUCTIVE HOLES	J. Larnerd J. Lauffer V. Markovich K. Papathomas	12/18/2003	10/737,974	2005-0136646	5/1/2007	7,211,289		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	EP-2-03-014	Europe		METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	J. Larnerd J. Lauffer V. Markovich K. Papathomas							Abandoned
	JP-2-03-014	Japan		METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	J. Larnerd J. Lauffer V. Markovich K. Papathomas		2004-355230					Pending
	TW-2-03-014	Taiwan		METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	J. Larnerd J. Lauffer V. Markovich K. Papathomas		93137509					Pending
	2-03-014D	US		METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	J. Larnerd J. Lauffer V. Markovich K. Papathomas	4/5/2006	11/397,713	2006-0183316	3/25/2008	7,348,677		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-002	US		CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING, ELECTRICAL ASSEMBLY UTILIZING SAME AND METHOD OF MAKING	J. Lauffer V. Markovich C. Seastrand D. Thomas	3/3/2004	10/790,747	2005-0195585	4/24/2007	7,209,368		Issued
	2-04-002D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING	J. Lauffer V. Markovich C. Seastrand D. Thomas	5/9/2006	11/429,990	2006-0200977	12/9/2008	7,478,472		Issued
	2-04-009	US		CIRCUITIZED SUBSTRATE WITH FILLED ISOLATION BORDER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich	7/2/2004	10/882,170	2006-0000639	1/2/2007	7,157,647		Issued
	2-04-009D1	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH FILLED ISOLATION BORDER	J. Lauffer J. Larnerd V. Markovich	7/10/2006	11/482,945	2006-0248717	10/19/2010	7,814,649		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-013	US		CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich	7/2/2004	10/882,167	2006-0000636	1/2/2007	7,157,646		Issued
	CN-2-04-013	China		CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich		200510079925.0					Issued
	IN-2-04-013	India		CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY	J. Lauffer J. Larnerd V. Markovich		1330/DEL/2005					Pendin g

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME								
	JP-2-04-013	Japan		CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich							Abandoned
	TW-2-04-013	Taiwan		CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich		94120469					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-013D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER AND INFORMATION HANDLING SYSTEM UTILIZING SAME	J. Lauffer J. Larnerd V. Markovich	12/20/2006	11/641,810	2007-0144772	5/27/2008	7,377,033		Issued
	2-04-013DD	US		INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER	J. Lauffer J. Larnerd V. Markovich	1/18/2008	12/010,004	2008-0117583	2/17/2009	7,491,896		Issued
	2-04-016	US		METHOD OF MAKING CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF	J. Lauffer V. Markovich M. Wozniak	11/19/2004	10/991,532	2006-0110898	6/10/2008	7,383,629		Issued
	CN-2-04-016	China		CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL	J. Lauffer V. Markovich M. Wozniak		200510115609.4					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME								
	IN-2-04-016	India		CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	J. Lauffer V. Markovich M. Wozniak		2488/DEL/2005 8					Pendin g
	JP-2-04-016	Japan		CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING	J. Lauffer V. Markovich M. Wozniak		2005-299079					Abando ned

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SYSTEMS UTILIZING SAME								
	TW-2-04-016	Taiwan		CIRCUITIZED SUBSTRATE UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	J. Lauffer V. Markovich M. Wozniak		94139033					Pending
	2-04-016D	US		CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF	J. Lauffer V. Markovich M. Wozniak	4/17/2008	12/148,271	2008-0259581	11/23/2010	7,838,776		Issued
	2-04-016D2	US		CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF	J. Lauffer V. Markovich M. Wozniak	8/11/2010	12/854,252	2010-0328868				Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-049				SELF-SINTERING METAL INTERCONNECTION	M. Poliks et al							
1-03-050	**2-04-018**	US		CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	C. Danoski I. Memis S. Rosser	9/29/2004	10/953,923	2006-0065433	11/13/2007	7,294,791		Issued
	2-04-018D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM	C. Danoski I. Memis S. Rosser	8/15/2007	11/889,668	2007-0284140	9/15/2009	7,589,283		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-03-051	2-04-006	US		METHOD AND SYSTEM FOR TRACKING GOODS	B. Chan H. Lin W. Maines V. Markovich	6/4/2004	10/860,067	2005-0289019	6/23/2009	7,552,091		Issued
	CN-2-04-006	China		METHOD AND SYSTEM FOR TRACKING GOODS	B. Chan H. Lin W. Maines V. Markovich		200510073420.3					Pending
	EP-2-04-006	Europe		METHOD AND SYSTEM FOR TRACKING GOODS	B. Chan H. Lin W. Maines V. Markovich		1603074					Abandoned
	JP-2-04-006	Japan		METHOD AND SYSTEM FOR TRACKING GOODS	B. Chan H. Lin W. Maines V. Markovich		2005-147041					Abandoned
	TW-2-04-006	Taiwan		METHOD AND SYSTEM FOR TRACKING GOODS	B. Chan H. Lin W. Maines V. Markovich		94116633					Abandoned
1-03-052	ON HOLD			CHIP CARRIER TEST METHOD	V. Jadhav et al							On Hold
1-03-053	ON HOLD			CHIP CARRIER TEST METHOD	V. Jadhav et al							On Hold
1-03-054				INTERPOSER WITH DUAL SIDE SOLDER CONNECTIONS	D. Alcoe							
1-03-055	ON HOLD			THIN CORE REGISTRATION METHOD	J. Lauffer et al							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-04-001				DRICLAD-BASED NANOCOMPOSITE MATERIALS AND COMPONENTS	M. Poliks et al							
1-04-002	2-04-010	US		RADIO FREQUENCY DEVICE FOR TRACKING GOODS	B. Chan W. Kimler H. Lin W. Maines V. Markovich	6/4/2004	10/860,071	2005-0270160	11/28/2006	7,142,121		Issue
1-04-003	ON HOLD			GRID ARRAY PROBE STRUCTURE	C. Majka et al							On Hold
1-04-004	2-04-015	US		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	J. Konrad J. Kotylo J. Rios	10/21/2004	10/968,929	2006-0099727	8/8/2006	7,087,441		Issued
1-04-005	ON HOLD			SUBSTRATE WITH ADDED METAL TO PREVENT DISHING	J. Potenza et al							On Hold
1-04-006	ON HOLD			ENHANCED PCB SOLDER MOUNTING SITE	Paul Logan							On Hold
1-04-007	ON HOLD			DRICLAD – BATIO3 NANOCOMPOSITE MATERIAL	M. Poliks et al							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-04-008	2-04-008	US		HIGH SPEED CIRCUITIZED SUBSTRATE WITH REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	B. Chan J. Lauffer	9/30/2004	10/955,741	2005-0039950	2/7/2006	6,995,322		Issued
	CN-2-04-008	China		HIGH SPEED CIRCUITIZED SUBSTRATE W/REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	B. Chan J. Lauffer		200510105837.3					Issued
	IN-2-04-008	India		HIGH SPEED CIRCUITIZED SUBSTRATE W/REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM	B. Chan J. Lauffer		1828/DEL/2005					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME								
	JP-2-04-008	Japan		HIGH SPEED CIRCUITIZED SUBSTRATE W/REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	B. Chan J. Lauffer							Abandoned
	TW-2-04-008	Taiwan		HIGH SPEED CIRCUITIZED SUBSTRATE W/REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	B. Chan J. Lauffer		94132230					Pending
1-04-009	ON HOLD			TBD	P. Logan							On Hold
1-04-012	ON HOLD			IMPROVED GOLD ADHESION ADDITIVES	L. Matienzo							On Hold

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-04-013	**2-05-025**	US		SUBSTRATE TEST APPARATUS AND METHOD OF TESTING SUBSTRATES	K. Knadle	11/18/2005	11/281,456		10/31/2006	7,129,732		Issued
1-04-014	**ON HOLD**			ORGANIC PEDESTAL FOR ELECTRICALLY TESTING INTEGRATED CIRCUIT CHIPS	F. Egitto et al							On Hold
1-04-015	**ON HOLD**			PHOTOIMAGEABLE POLYMER NANOCOMPOSITE PASSIVE MATERIAL	M. Poliks et al							On Hold
1-04-016	**2-05-001**	US		INTERPOSER FOR USE WITH TEST APPARATUS	F. Egitto H. Lin	4/21/2005	11/110,901	2006-0238207	11/6/2007	7,292,055		Issued
	2-05-001D	US		METHOD OF MAKING AN INTERPOSER	F. Egitto H. Lin	9/27/2007	11/902,976	2008-0020566	3/31/2009	7,511,518		Issued
1-04-017	**ON HOLD**			DOUBLE-SIDED REFLOW SOLDER FIXTURE	P. Logan							On Hold
1-04-018	**2-05-014**	US		WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM	D. Calatka V. Calmidi S. Sathe	6/15/2005	11/152,048	2006-0284304	8/7/2007	7,253,518		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				UTILIZING SAME								
	2-05-014D	US		METHOD OF MAKING WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN	D. Calatka V. Calmidi S. Sathe	7/9/2007	11/822,573	2007-0254408	3/31/2009	7,510,912		Issued
1-04-019	**2-05-010**	US		MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW AND CIRCUITIZED SUBSTRATE FOR USE THEREIN	I. Memis	5/12/2005	11/127,160	2006-0255460	2/19/2008	7,332,818		Issued
	2-05-010D	US		METHOD OF MAKING MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW	I. Memis	12/21/2007	12/003,299	2008-0102562	11/24/2009	7,622,384		Issued
1-04-020	**2-04-017**	US		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD	R. Das J. Lauffer K. Papathomas M. Poliks	1/10/2005	11/031,085	2006-0151863	6/2/2009	7,541,265		Issued

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE								
	CN-2-04-017	China		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATES	R. Das J. Lauffer K. Papathomas M. Poliks		200510097424.5					Pending
	IN-2-04-017	India		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING	R. Das J. Lauffer K. Papathomas M. Poliks		3154/DEL/2005					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATES								
	JP-2-04-017	Japan		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATES	R. Das J. Lauffer K. Papathomas M. Poliks		2006-001082					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	TW-2-04-017	Taiwan		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATES	R. Das J. Lauffer K. Papathomas M. Poliks		94147056					
1-04-021	**ON HOLD**			METALLIC FOAM CONNECTION STRUCTURE	B. Chan							
1-04-022	**2-05-006**	US		PLATING METHOD FOR CIRCUITIZED SUBSTRATES	N. Card R. Edwards J. Konrad R. Magnuson T. Wells M. Wozniak	5/13/2005	11/128,272	2006-0255009	1/30/2007	7,169,313		Issued
1-04-023	**2-05-016**	US		METHOD OF TREATING CONDUCTIVE LAYER FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD	F. Egitto S. Krasniak J. Lauffer V. Markovich L. Matienzo	1/9/2006	11/327,493	2006-0121738	12/11/2007	7,307,022		Issued

SCHEDULE - 1

Discl. No.	Docket Nos.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				OF MAKING SAID SUBSTRATE HAVING SAID CONDUCTIVE LAYER AS PART THEREOF								
	2-05-016D	US		CIRCUITIZED SUBSTRATE WITH INCREASED ROUGHNESS CONDUCTIVE LAYER AS PART THEREOF	F. Egitto S. Krasniak J. Lauffer V. Markovich L. Matienzo	10/26/2007	11/976,629	2008-0054476				Pending
1-04-024	**ON HOLD**			EDS AT PLANE ENTRANCE	A. Bhatt et al							On Hold
1-04-025	**2-05-012**	US		CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS, MULTILAYERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	F. Egitto V. Markovich L. Matienzo	7/11/2005	11/177,442	2007-0007032	3/11/2008	7,342,183		Issued
	2-05-012D	US		METHOD OF MAKING MULTILAYERED CIRCUITIZED SUBSTRATE ASSEMBLY	F. Egitto V. Markovich L. Matienzo	9/28/2007	11/905,188	2008-0022520	11/2/2010	7,823,274		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-05-013	US		METHOD OF MAKING MULTILAYERED CIRCUITIZED SUBSTRATE ASSEMBLY HAVING SINTERED PASTE CONNECTIONS	F. Egitto V. Markovich L. Matienzo	7/11/2005	11/177,413	2007-0006452	2/26/2008	7,334,323		Issued
	2-05-013D	us		CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS AND MULTILAYERED SUBSTRATE ASSEMBLY HAVING SAID SUBSTRATE AS PART THEREOF	F. Egitto V. Markovich L. Matienzo	1/8/2008	12/007,178	2008-0105457				Pending
1-04-026	**2-04-019**	US		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING	B. Chan J. Lauffer	11/19/2004	10/991,451		11/15/2005	6,964,884		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SAME								
	CN-2-04-019	China		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	B. Chan J. Lauffer		200510115610.7					Pending
	IN-2-04-019	India		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND	B. Chan J. Lauffer		2489/DEL/2005					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				INFORMATION HANDLING SYSTEMS UTILIZING SAME								
	JP-2-04-019	Japan		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	B. Chan J. Lauffer		2005-301345					Abandoned
	TW-2-04-019	Taiwan		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND	B. Chan J. Lauffer		94139020					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				INFORMATION HANDLING SYSTEMS UTILIZING SAME								
	2-04-019D	US		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	B. Chan J. Lauffer	8/31/2005	11/215,206	2006-0180343				Pending
1-04-027	**2-05-003**	US		APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson	4/21/2005	11/110,919		11/13/2007	7,293,355		Issued
	CN-2-05-003	China		APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson		200610072098.7					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	EP-2-05-003	Europe		APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson							Abandoned
	JP-2-05-003	Japan		APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson							Abandoned
	TW-2-05-003	Taiwan		APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson		95112656					Pending
	2-05-003D	US		APPARATUS FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. Orband W. Wilson	8/3/2007	11/882,625	2007-0266555	2/12/2008	7,328,502		Issued
1-04-028	2-05-005	US		APPARATUS FOR MAKING CIRCUITIZED SUBSTRATES HAVING PHOTO-IMAGEABLE DIELECTRIC LAYERS IN A CONTINUOUS	J. Lauffer V. Markovich J. McNamara P. Moschak	4/21/2005	11/110,920	2006-0240364	11/9/2010	7,827,682		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patents Expires	Status
				MANNER								
	2-05-005D	US		METHOD FOR MAKING CIRCUITIZED SUBSTRATES HAVING PHOTO-IMAGEABLE DIELECTRIC LAYERS IN A CONTINUOUS MANNER	J. Lauffer V. Markovich J. McNamara P. Moschak	1/20/2010	12/657,394	2011-0173809	7/12/2011	7,977,034		Issued
1-04-029	**2-05-017**	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp J. Lauffer V. Markovich W. Wilson	1/4/2006	11/324,432	2007-0166944	6/3/2008	7,381,587		Issued
	CN-2-05-017	China		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp J. Lauffer V. Markovich W. Wilson		200610170522.1					Issued
	EP-2-05-017	Europe		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp J. Lauffer V. Markovich W. Wilson		6256578.3					Abandoned
	JP-2-05-017	Japan		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp J. Lauffer V. Markovich W. Wilson							

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	TW-2-05-017	Taiwan		METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Japp J. Lauffer V. Markovich W. Wilson		95148292					Pending
1-04-030	ON HOLD			METHOD OF MAKING CIRCUITIZED SUBSTRATE	A. Bhatt et al							On Hold
1-04-031	ON HOLD			VIA FILL TEST VEHICLE	J. Konrad et al							On Hold
1-04-032	2-04-020	US		CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer V. Markovich M. Poliks	1/10/2005	11/031,074		4/11/2006	7,025,607		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-04-020D	US		CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer V. Markovich M. Poliks	1/4/2006	11/324,273	2006-0154501				Pending
1-04-033	2-05-008	US		METHOD OF MAKING AN INTERNAL CAPACITIVE SUBSTRATE FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer V. Markovich J. Matthews	7/5/2005	11/172,794	2006-0154434	6/10/2008	7,384,856		Issued
1-04-034	ON HOLD			BGA/CCGA MODULE REWORK METHOD	B. Chan et al							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-05-001	**ON HOLD**			NI, PD AND CU PTH OVERPLATING	R. Edwards et al							On Hold
1-05-002	**ON HOLD**			CITC TEST COUPON	K. Knadle							On Hold
1-05-003	**2-05-009**	US		RESISTOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer V. Markovich	7/5/2005	11/172,786	2006-0151202	7/13/2006	7,235,745		Issued
	2-05-009D	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH A RESISTOR	R. Das J. Lauffer V. Markovich	5/2/2007	11/797,236	2008-0151515	1/18/2011	7,870,664		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-05-009D2	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH RESISTOR INCLUDING MATERIAL WITH METAL COMPONENT AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer V. Markovich	11/3/2010	12/938,759	2011-0043987				Pending
1-05-004	**2-05-018**	US		METHOD OF IMPROVING ELECTRICAL CONNECTIONS IN CIRCUITIZED SUBSTRATES	S. Desai J. Lauffer H. Lin V. Markovich R. Smith	12/19/2005	11/305,073	2007-0139977	12/8/2009	7,629,559		Issued
1-05-006	**ON HOLD**			LGA CONTACT	B. Chan et al							On Hold
1-05-007				LASER PROCESSING OF PASSIVES	R. Das et al							
1-05-008	**2-05-015**	US		METHOD AND APPARATUS FOR DEPOSITING CONDUCTIVE PASTE IN CIRCUITIZED SUBSTRATE	N. Card J. Lauffer	9/1/2005	11/216,133	2007-0048897	5/1/2007	7,211,470		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				OPENINGS								
1-05-009	**ON HOLD**			PCB TEST CARD	K. Knadle et al							On Hold
1-05-010	**2-06-001**	US		ADJUSTABLE THICKNESS THERMAL INTERPOSER AND ELECTRONIC PACKAGE UTILIZING SAME	D. Alcoe C. Varaprasad	4/4/2006	11/396,711	2007-0230130	12/8/2009	7,629,684		Issued
1-05-011	**2-05-028**	US		METHOD OF FORMING FIBROUS LAMINATE CHIP CARRIER STRUCTURES	R. Japp K. Papathomas C. Palomaki	7/16/2010	12/837,584					Pending
1-05-012	**ON HOLD**			HYPERZ HOLE FILL WITH PEELABLE LAYER	T. Antesberger et al							On Hold
1-05-013	**2-06-004**	US		CAPACITIVE SUBSTRATE	R. Das F. Egitto J. Lauffer H. Lin V. Markovich	5/23/2006	11/438,424	2007-0275525	3/1/2011	7,897,877		Issued
	2-06-004D	US		CAPACITIVE SUBSTRATE AND METHOD OF MAKING SAME	R. Das F. Egitto J. Lauffer H. Lin V. Markovich	3/2/2009	12/380,616	2009-0206051	9/28/2010	7,803,688		Issued
1-05-014	**ON HOLD**			FLUID HEAD	R. Edwards et							On

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				PTH ETCH PROCESS	al							Hold
1-05-015	2-08-009	US		PHOTOSENSITIVE DIELECTRIC FILM	J. Lauffer V. Markovich K. Papathomas	7/27/2009	12/460,975	2011-0017498				Pending
1-05-016	ON HOLD			IMPROVED METHOD TO ETCH COPPER	B. Blomberg							On Hold
1-05-017	2-05-023	US		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	S. Anderson S. Moore C. Palomaki S. Tran	10/20/2005	11/253,659	2007-0090170				Abandoned
	CN-2-05-023	China		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	S. Anderson S. Moore C. Palomaki S. Tran		200610140058.1					Issued
	JP-2-05-023	Japan		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	S. Anderson S. Moore C. Palomaki S. Tran		2006-267024					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	TW-2-05-023	Taiwan		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	S. Anderson S. Moore C. Palomaki S. Tran		95137377					Abandoned
1-05-018	2-05-019	US		DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas	11/3/2005	11/265,287	2006-0054870	4/26/2011	7,931,830		Issued
	CN-2-05-019	China		DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas		200610150779.0					Pending
	IN-2-05-019	India		DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas		2164/DEL/2006					Pending

SCHEDULE - 1

074658.01352/22095298v.5

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	JP-2-05-019	Japan		DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas		2006-288641					Pending
	TW-2-05-019	Taiwan		DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas		95138578					Pending
1-05-019	2-05-021	US		CIRCUITIZED SUBSTRATE WITH SOLDER-COATED MICROPARTICLE PASTE CONNECTIONS, MULTILAYERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZIGN SAME AND METHOD OF MAKING SAID SUBSTRATE	R. Das J. Lauffer R. Magnuson V. Markovich	10/6/2005	11/244,180	2007-0007033	10/28/2008	7,442,879		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-05-020				PREPREG-BASED EMBEDDED CAPACITORS	R. Das et al							Trade Secret
1-05-021	**2-06-010**	US		INTERPOSER AND TEST ASSEMBLY FOR TESTING ELECTRONIC DEVICES	B. Chan F. Egitto V. Markovich	12/4/2006	11/607,973	2007-0075726	3/10/2009	7,501,839		Issued
1-05-022	**ON HOLD**			ELECTRODE/CATHODE FOR ELECTROPLATING MICRO-PARTICLES	R. Das et al							On Hold
1-05-023	**2-05-024**	US		FLUOROPOLYMER DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas	3/28/2006	11/390,386	2006-0180936	9/30/2008	7,429,789		Issued
	JP-2-05-024	Japan		FLUOROPOLYMER DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	R. Japp V. Markovich K. Papathomas		2007-081228					Pending
1-05-024	**ON HOLD**			CERAMIC-FILLED THERMOSETTING	R. Das et al							On Hold

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				COMPOSITES HAVING LOW LOSS AND LOW K VALUES								
1-05-025	2-06-002	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	N. Card T. Miller W. Rudik	11/14/2006	11/598,647	2008-0110016	6/16/2009	7,547,577		Issued
	CN-2-06-002	China		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	N. Card T. Miller W. Rudik	11/5/2007	200710165173.9				11/5/2027	Issued
	IN-2-06-002	India		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	N. Card T. Miller W. Rudik		2156/DEL/2007					Pending
	JP-2-06-002	Japan		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	N. Card T. Miller W. Rudik		2007-280002					Abandoned
	TW-2-06-002	Taiwan		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	N. Card T. Miller W. Rudik		96138518					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-05-026	2-05-026	US		METHOD OF MAKING A CAPACITIVE SUBSTRATE FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE	R. Das J. Lauffer H. Lin V. Markovich	2/13/2006	11/352,279	2007-0010065	11/11/2008	7,449,381		Issued
	2-05-027	US		METHOD OF MAKING A CAPACITIVE SUBSTRATE USING PHOTOIMAGEABLE DIELECTRIC FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN	R. Das J. Lauffer H. Lin V. Markovich	2/13/2006	11/352,276	2007-0010064	9/30/2008	7,429,510		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE								
1-05-027	**ON HOLD**				A. Bhatt							On Hold
1-06-002	**2-07-001**	US		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	A. Bhatt R. Harendza R. Japp	1/12/2007	11/652,633	2008-0168651	10/6/2009	7,596,863		Issued
	CN-2-07-001	China		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	A. Bhatt R. Harendza R. Japp		200810000754.1					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	HK-2-07-001	Hong Kong		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	A. Bhatt R. Harendza R. Japp		9103246.7					Pending
	IN-2-07-001	India		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	A. Bhatt R. Harendza R. Japp		2709/DEL/2007					Pending
	JP-2-07-001	Japan		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	A. Bhatt R. Harendza R. Japp		2007-331780					Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-06-003	**2-06-011**	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER BALLS HAVING ROUGHENED SURFACES, METHOD OF MAKING ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE, AND METHOD OF MAKING MULTIPLE CIRCUITIZED SUBSTRATE ASSEMBLY	D. Alcoe P. Hart	1/8/2007	11/650,520	2008-0164300				Pendi g
1-06-004	**ON HOLD**			PACEMARKER ORGANIC CIRCUIT	A. Bhatt et al							On Hold
1-06-005	**2-06-015**	US		CRENELATED ISOLATION BORDER DESIGN	F. Egitto et al							
1-06-006	**2-06-009**	US		METHOD OF MAKING A CIRCUITIZED SUBSTRATE WITH ENHANCED CIRCUITRY AND ELECTRICAL ASSEMBLY UTILIZING SAID	J. Kresge C. Palomaki	11/1/2006	11/590,888	2008-0098595	9/29/2009	7,595,454		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SUBSTRATE								
1-06-007	**2-06-006**	US		HIGH SPEED INTERPOSER	D. Caletka F. Egitto	6/19/2006	11/454,896	2007-0289773	12/8/2009	7,629,541		Issued
	2-06-006D1	US		HIGH SPEED INTERPOSER	D. Caletka F. Egitto	1/24/2008	12/010,335	2008-0142258	1/25/2011	7,875,811		Issued
	2-06-006D2	US		METHOD OF MAKING HIGH SPEED INTERPOSER	D. Caletka F. Egitto	1/25/2008	12/010,469	2008-0120835				Pending
1-06-008	**2-06-005**	US		PHOTORESIST COMPOSITION WITH ANTIBACTERIAL AGENT	R. Keesler J. Konrad R. Magnuson R. Sinicki	7/25/2006	11/492,029	2008-0026316	12/22/2009	7,635,552		Issued
1-06-009	**2-06-007**	US		SOLDER MASK APPLICATION PROCESS	N. Card R. Day J. Konrad	8/8/2006	11/500,328	2008-0038670				Pending
1-06-010	**2-06-014**	US		PRINTED CONDUCTIVE LINES WITH LOW RESISTIVITY	R. Das et al	7/18/2011	13/184,699					Pending
1-06-011	**ABANDONED**			NANOTUBE INTERFACE MATERIAL	V. Calmidi et al							Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-06-012	2-06-008	US		HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp V. Markovich K. Papathomas	10/3/2006	11/541,776	2008-0078570	3/30/2010	7,687,722		Issue
	CN-2-06-008	China		HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp V. Markovich K. Papathomas		200710161542.7					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	IN-2-06-008	India		HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp V. Markovich K. Papathomas		2044/DEL/2007					Pending
	JP-2-06-008	Japan		HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp V. Markovich K. Papathomas		2007-257049						Abandoned

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-06-008D	US		HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	R. Japp V. Markovich K. Papathomas	3/2/2009	12/380,618	2009-0175000				Pending
1-06-013	**2-07-003**	US		METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SELECTED CONDUCTORS HAVING SOLDER THEREON	N. Card R. Harendza J. Konrad T. Mosher S. Pitely J. Rios	3/30/2007	11/730,212	2008-0241359	3/22/2011	7,910,156	3/30/2027	Issued
1-06-014				MICROVIA- OR TRENCH-FILLED EMBEDDED CAPACITOR	R. Das et al							
1-06-015	**ON HOLD**			IMPROVED ROLL-TO-ROLL PCB PROCESS	R. Das et al							On Hold
1-06-016				INTERNAL CAPACITOR WITH	R. Das et al							

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				RESISTOR COMPONENT								
1-06-017				INK-JET PRINTED CIRCUITS	R. Das et al							
1-06-018	2-07-002	US		FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	D. Alcoe V. Calmidi	3/26/2007	11/727,314	2008-0237840	12/14/2010	7,851,906		Issued
	CN-2-07-002	China		FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	D. Alcoe V. Calmidi		200810089718.7					Pending
	IN-2-07-002	India		FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	D. Alcoe V. Calmidi		422/DEL/2008					Pending
	JP-2-07-002	Japan		FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	D. Alcoe V. Calmidi		2008-057976					Pending
	TW-2-07-002	Taiwan		FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	D. Alcoe V. Calmidi		97106659					Pending
1-06-019	See 2-09-002			Z-AXIS INTERCONNECT STRUCTURES	R. Das et al							See 2-09-002

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-06-020	2-07-005	US		METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	T. Davis S. Desai J. Lauffer J. McNamara V. Markovich	5/2/2007	11/797,232	2007-0199195	12/8/2009	7,627,947		Issued
	CN-2-07-005	China		METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	T. Davis S. Desai J. Lauffer J. McNamara V. Markovich		200810094487.9					Pending
	IN-2-07-005	India		METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	T. Davis S. Desai J. Lauffer J. McNamara V. Markovich		887/DEL/2008					Pending
	EP-2-07-005	Europe		METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	T. Davis S. Desai J. Lauffer J. McNamara V. Markovich		8251545.3					Pending
	JP-2-07-005	Japan		METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	T. Davis S. Desai J. Lauffer J. McNamara V. Markovich		2008-114868					Pending
1-06-021				LAMINATE WITH EMBEDDED CHIPS	R. Das et al							

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-06-022	**2-06-013**	US		NON-FLAKING CAPACITOR MATERIAL, CAPACITIVE SUBSTRATE HAVING AN INTERNAL CAPACITOR THEREIN INCLUDING SAID NON-FLAKING CAPACITOR MATERIAL, AND METHOD OF MAKING A CAPACITOR MEMBER FOR USE IN A CAPACITIVE SUBSTRATE	R. Das J. Lauffer V. Markovich K. Papathomas	4/4/2007	11/730,761	2007-0177331				Pendir g
1-06-023				PCB WITH MISMATCHED LAYERING	R. Fotorny et al							Trade Secret
1-06-024	**2-07-006**	US		ADHESIVE BLEED PREVENTION METHOD AND PRODUCT PRODUCED FROM SAME	R. Magnuson L. Matienzo	7/31/2007	11/882,149	2009-0035455				Pendin g
1-06-025	**2-06-012**	US		CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL	K. Blackwell F. Egitto J. Lauffer V. Markovich	4/9/2007	11/783,306	2008-0244902	9/21/2010	7,800,916		Pendin g

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME								
	EP-2-06-012	Europe		CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	K. Blackwell F. Egitto J. Lauffer V. Markovich		8251098.3					Pending
	JP-2-06-012	Japan		CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING	K. Blackwell F. Egitto J. Lauffer V. Markovich		2008-098245					Pending

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.:	Docket No.:	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.:	Publication No.	Issued	Patent No.	Patent Expires	Status
				SYSTEM UTILIZING SAME								
	TW-2-06-012	Taiwan		CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	K. Blackwell F. Egitto J. Lauffer V. Markovich		97111078					Pending
1-06-026	EI-2-06-026	US		NANO-MICRO INTERCONNECT	R. Das et al							
1-06-027	2-06-027	US		EMBOSSING OPTICAL WAVEGUIDES	B. Chan et al							
1-06-028	2-07-008	US		CIRCUITIZED SUBSTRATE WITH CONDUCTIVE PASTE, ELECTRICAL ASSEMBLY INCLUDING SAID	R. Das K. Papathomas V. Markovich	5/23/2007	11/802,434	2007-0221404	11/22/2011	8,063,315	7/7/2030	Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE								
	2-07-008D	US		CIRCUITIZED SUBSTRATE WITH CONDUCTIVE PASTE, ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE	R. Das K. Papathomas V. Markovich	10/4/2011	13/252,256					Pending
	CN-2-07-008	China		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das K. Papathomas V. Markovich		200810108619.9					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	HK-2-07-008	Hong Kong		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das K. Papathomas V. Markovich		9103286.8					Pending
	EP-2-07-008	Europe		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das K. Papathomas V. Markovich		8251755.8					Abandoned
	IN-2-07-008	India		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE	R. Das K. Papathomas V. Markovich		912/DEL/2008					Pending

SCHEDULE - 1

074658.01352/22095298v.5

Discl No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE								
	JP-2-07-008	Japan		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das K. Papathomas V. Markovich		2008-127348					Pending
1-06-029	2-06-029	US		ELECTRICALLY CONDUCTIVE ADHESIVE (ECA) FOR MULTILAYER DEVICE INTERCONNECTS	R. Das et al	8/5/2011	13/198,756					Pending
1-06-030				MULTILAYER METAL WITHIN MICROVIA	R. Das et al							
1-06-031	2-07-009	US		METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION	T. Miller D. Stanke R. Testa	6/7/2007	11/808,140	2008-0301933	5/11/2010	7,712,210		Issued

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				PORTION								
1-06-032				BARRIER LAYER FOR WIREBOND/HASL MIXED METALLURGY	J. Konrad et al							
1-06-033	**2-07-013**	US		POWER CORE FOR USE IN CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	R. Japp K. Papathomas J. Kresge T. Antesberger	5/18/2010	12/782,187	2011-0284273				Pending
1-07-001	**2-08-003**	US		HIGH BANDWIDTH SEMICONDUCTOR BALL GRID ARRAY PACKAGE	K. Blackwell F. Egitto V. Markovich	11/4/2010	12/939,659					Pending
1-07-002	**2-07-004**	US		LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	B. Chan J. Kozol J. Lauffer H. Lin	4/2/2007	11/730,404	2008-0238323	11/30/2010	7,841,741		Issued
	CN-2-07-004	China		LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	B. Chan J. Kozol J. Lauffer H. Lin		200810087553.X					Abandoned
	HK-2-07-004	Hong Kong		LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	B. Chan J. Kozol J. Lauffer H. Lin		9103287.7					Pending

SCHEDULE - 1

074658.01352/22095298v.5

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	IN-2-07-004	India		LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	B. Chan J. Kozol J. Lauffer H. Lin		642/DEL/2008					Pending
1-07-003	2-07-010	US		METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING AT LEAST ONE CAPACITOR THEREIN	R. Das F. Egitto H. Lin J. Lauffer V. Markovich	7/26/2007	11/878,673	2008-0248596				Pending
1-07-004				BALANCED COOLING OF SOLDERED SUBSTRATES	K. Knadle et al							
1-07-005	2-07-040	US		DEFECTIVE CONDUCTIVE SURFACE PAD REPAIR FOR MICROELECTRONIC CIRCUIT CARDS	L. Matienzo et al	3/7/2011	13/041,655					Pending
1-07-006	2-07-007	US		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das M. Rowlands	6/4/2007	11/806,685	2008-0087459	3/30/2010	7,687,724		Issued

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	JP-2-07-007	Japan		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das M. Rowlands		2008-145499					Pending
	TW-2-07-007	Taiwan		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	R. Das M. Rowlands		97118394					Pending
	EI-2-07-007D	US		CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE,	R. Das M. Rowlands	10/20/2009	12/589,239	2011-0039212				Pending

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE								
1-07-007				DRILL DESIGN FOR MULTI PASS DRILLING	K. Haughan et al							Trade Secret
1-07-008				ELECTRICALLY RELIABLE LASER DRILLED MICRO VIAS WITH HIGH ASPECT RATIOS IN PCB STRUCTURES	L. Matienzo et al							Trade Secret
1-07-009				METHOD OF REDUCING ELECTRICAL DISCONTINUITIES USING PRECISE EMBEDDED RESISTANCE MATERIAL	M. Rowlands et al							
1-07-010	**2-07-015**	US		METHOD OF MAKING CIRCUITIZED ASSEMBLY INCLUDING A PLURALITY OF CIRCUITIZED SUBSTRATES	J. Lauffer	1/15/2008	12/007,704	2009-0178273				Pending
1-07-011				TEMPORARY MASK FOR INTERNAL FEATURES/HOLES DURING PCB	J. Konrad et al							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				COMPOSITE LAMINATION								
1-07-012				METHOD FOR FABRICATION OF A THICK ASSEMBLED BOARD FROM TWO BOARDS	B. Chan et al							Publicly Disclosed
1-07-013	**2-08-011**	US		METHOD TO JOIN TWO PARALLEL BOARDS WITH AN LGA CONNECTOR	B. Chan et al							
1-07-014	**ABANDONED**			DOUBLE SIDED MULTI-CHIP MODULE CONSTRUCTION	B. Chan et al							Publicly Disclosed
1-07-015	**ABANDONED**			METHOD TO OPTIMIZE THE PARTITION OF ALL-TO-ALL INTERCONNECTED MULTIPROCESSOR COMPUTING SYSTEM	H. Lin et al							Publicly Disclosed
1-07-016				METHOD TO TEST LARGE MULTIPROCESSOR MULTICLUSTER COMPUTER SYSTEM WITH FULL COVERAGE	H. Lin et al							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-07-017	**ABANDONED**			OPTIMIZED DESIGN FOR HIGH SPEED ELECTRONIC INTERCONNECTIONS	H. Lin et al							Publicly Disclosed
1-07-018	**2-08-001**	US		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	J. Lauffer R. Magnuson V. Markovich J. Paoletti K. Papathomas R. Rai	3/28/2008	12/078,206	2009-0241332				Pending
1-07-019	**ABANDONED**			USING EMBEDDED PRINTED RESISTORS TO IMPROVE ELECTRICAL PERFORMANCE IN A PRINTED CIRCUIT BOARD	M. Rowlands et al							Publicly Disclosed
1-07-020	**ABANDONED**			INTERNAL AIR CAVITIES FOR LOWEST LOSS TRANSMISSION LINE STRUCTURE"	M. Rowlands et al							Publicly Disclosed
1-07-021	**2-08-004**	US		BOWTIE LGA CONNECTOR	B. Chan et al							
1-07-022	**2-08-010**	US		METHOD OF FORMING MULTILAYER CAPACITORS IN A PRINTED CIRCUIT SUBSTRATE	R. Das F. Egitto H. Lin J. Lauffer V. Markovich	10/22/2010	12/909,983					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-07-023	**2-07-023**	US		METHOD FOR IMPREGNATING ORGANIC FIBER PAPERS, INCLUDING P-ARAMID PAPERS	R. Japp W. Fotorny K. Papathomas M. Poliks V. Markovich	7/7/2010	12/831,411					Pending
1-07-024	**ON HOLD**			LAMINATE DRILL BACKER	R. Japp et al							On Hold
1-07-025	**2-07-017**	US		CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	R. Japp V. Markovich K. Papathomas M. Poliks	4/10/2008	12/081,051	2008-0191354	12/27/2011	8,084,863	5/30/2025	Issued (CIP of EI-2-04-007)
	2-07-017D	US		METHOD OF MAKING A CIRCUITIZED SUBSTRATE WITH CONTINUOUS THERMOPLASTIC SUPPORT FILM DIELECTRIC LAYERS	R. Japp V. Markovich K. Papathomas M. Poliks	3/2/2009	12/380,637	2009-0258161				Pending
1-07-026	**2-08-002**	US		MULTILAYERED CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	R. Japp V. Markovich K. Papathomas M. Poliks	4/10/2008	12/081,042	2008-0191353	1/12/2010	7,646,098		Issued

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-08-002D	US		MULTILAYERED CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	R. Japp V. Markovich K. Papathomas M. Poliks	3/2/2009	12/380,617	2009-0173426				Pending
1-07-027	**2-07-027**	US		HALOGEN-FREE DIELECTRIC COMPOSITION FOR USE AS DIELECTRIC LAYER IN CIRCUITIZED SUBSTRATES	R. Japp K. Papathomas	2/25/2010	12/712,238	2011-0207866				Abandoned
1-07-028	**2-07-028**	US		CONDUCTIVE METAL NUB FOR ENHANCED ELECTRICAL INTERCONNECTION, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	L. Matienzo N. Card D. VanHart J. Konrad F. Egitto R. Das	1/20/2011	13/009,922					Pending
1-07-029				A METHOD FOR MANUFACTURING ESD PROTECTION CIRCUITRY	R. Das et al							
1-07-030	**ABANDONED**			HANDLING AND ASSEMBLY OF SMALL ORGANIC PACKAGES	T. Antesberger et al							Abandoned

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-07-031	**ABANDONED**			FLOW BALANCING THROUGH MULTIPLE COLD PLATES	J. Lauffer et al							Abandoned
1-07-032				THICK COPPER PCB PROCESS/BUILD	M. Wozniak et al							Trade Secret
1-07-033				MIXED PASTE METALLURGIES FOR	J. Konrad et al							Trade Secret
1-07-034				LAMINATION PROCESS TO REDUCE DISHING IN HIGH FILL DEMAND PCBS	K.Papathomas et al							Trade Secret
1-07-035				PROCESS TO PREPARE AND USE DOUBLED UP HOLE FILLING SHEETS IN THICK PRINTED CIRCUIT BOARDS	R. Japp et al							Trade Secret
1-07-036				METHOD AND STRUCTURE FOR A RIGID FLEX CIRCUIT BOARD HAVING MULTIPLE SURFACE FINISHES AND A WIRE BONDABLE FLEXIBLE LAYER	T. Miller et al							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-07-037				METHOD AND STRUCTURE FOR A RIGID FLEX CIRCUIT BOARD WITH EXTERNAL FLEX CONNECTION AND A CAVITY	T. Miller et al							Trade Secret
1-07-038				CU FILLED PTH	R. Keesler et al							Trade Secret
1-07-039	**2-08-007**	US		SPRING ACTUATED CLAMPING MECHANISM	B. Chan M. Lauffer	6/25/2008	12/215,079	2009-0320280	10/4/2011	8,028,390	**12/16/2029**	Issued
	2-08-007D	US		SPRING ACTUATED CLAMPING MECHANISM	B. Chan M. Lauffer	4/20/2011	13/090,676					Pending
1-08-001				METHOD OF MAKING BOARDS AND LAMINATE CHIP CARRIERS (LCC) FOR HIGH SPEED, AND RF (RADIO FREQUENCY) APPLICATIONS	R. Das et al							Trade Secret
1-08-002				SELF-ALIGNED, PLATED INTERPOSER	F. Egitto et al							
1-08-003	**2-08-005**	US		CIRCULAR CONNECTED SYSTEM	H. Lin et al							Trade Secret
1-08-004				HIGH CAPACITANCE RESIN COATED COPPER CAPACITIVE (RC3)	R. Das et al							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				MATERIAL FOR MULTILAYERED EMBEDDED CAPACITORS								
1-08-005	**2-08-023**	US		CONDUCTIVE PASTE FOR DEVICE LEVEL INTERCONNECTS	R. Das R. Magnuson M. Poliks V. Markovich	9/17/2010	12/884,657					Pending
1-08-006	**2-08-006**	US		HIGH DENSITY DECAL AND METHOD FOR ATTACHING SAME	V. Markovich R. Smith H. Lin F. Egitto R. Das W. Wilson R. Rai	7/16/2010	12/837,640					Pending
1-08-007				LMT/NO LEAD INTERCONNECT PASTE	R. Das et a							Trade Secret
1-08-008				MIXED METALLURGY PASTE FOR Z-INTERCONNECT	R. Das et al							Trade Secret
1-08-009	**2-08-008**	US		MULTI-LAYER EMBEDDED CAPACITANCE AND RESISTANCE SUBSTRATE CORE	R. Das J. Lauffer I. Memis S. Rosser	9/9/2008	12/283,146	2010-0060381	9/7/2010	7,791,897		Issued
	2-08-008D	US		MULTI-LAYER EMBEDDED CAPACITANCE AND RESISTANCE SUBSTRATE	R. Das J. Lauffer I. Memis S. Rosser	3/10/2010	12/720,849	2010-0167210				Allowed

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				CORE								
1-08-010	**2-08-024**	US		METHOD FOR VIA PLATING IN ELECTRONIC PACKAGES CONTAINING FLUOROPOLYMER DIELECTRIC LAYERS	R. Edwards F. Egitto L. Matienzo S. Pitely D. VanHart	4/22/2010	12/765,110	2011-0260299				Pending
1-08-011				PROCESS OF LCP BASED SUBSTRATE	R. Das et al							Trade Secret
1-08-012	**2-08-012**	US		LIQUID CRYSTAL POLYMER LAYER FOR ENCAPSULATION AND IMPROVED HERMITICITY OF CIRCUITIZED SUBSTRATES	R. Das M. Rowlands	9/17/2010	12/884,392					Allowed
1-08-013	**2-08-013**	US		CORELESS LCC/SIP/CARDS STRUCTURES AND MFG METHODS	V. Markovich et al							
1-08-014	**On Hold**			TRIANGULAR BLOCKS ON THE LEADING EDGE POSTS OF THE TPP LOADER	T. Kozakowski							On Hold
1-08-016	**2-08-016**	US		INTEGRATED 3D	V. Markovich							

SCHEDULE - 1

Disc. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				SEMICONDUCTOR PACKAGING								
1-08-017				MELTING AND RE-MELTING CONDUCTIVE PASTE FOR INTERCONNECTS	R. Das							Trade Secret
1-08-018				IMPROVED PROCESS FOR HEAVY COPPER DRILLING	M. Wozniak et al							Trade Secret
1-08-019	2-08-017	US		CONSTRUCTION OF HIGH SPEED AND HIGH DENSITY COMPUTING SYSTEM WITH MODULAR 3-D DETACHABLE COMPUTE MODULES	F. Egitto et al							
1-08-021	2-08-025	US		NEW HIGH DENSITY PACKAGING-COMPUTING SYSTEM	V. Markovich et al	4/8/2011	13/082,599					Pending
1-08-022	2-08-020	US		MODULAR 3-D DETACHABLE HIGH SPEED AND HIGH DENSITY PACKAGING STRUCTURE	H. Lin et al							
1-08-023	2-08-018	US		INTERCONNECT STRUCTURE THAT LIMITS STRESS WITHIN A SEMI-INSULATING X-	E. Johnson et al		See -1, -2, -3					

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.s	Publication No.	Issued	Patent No.	Patent Expires	Status
				RAY DETECTOR CRYSTAL								
	2-08-018-1	US			E. Johnson et al							
	2-08-018-2	US			E. Johnson et al							
	2-08-018-3	US			E. Johnson et al							
1-08-024	2-08-021	US		HIGH DENSITY SEMICONDUCTOR PACKAGING SOLUTIONS	V. Markovich et al.		See -1, -2, -3					See -1, -2, -3
	2-08-021-1	US		CORELESS LAYER BUILDUP STRUCTURE	T. Antesberger R. Das F. Egitto V. Markovich W. Wilson	4/22/2010	12/764,993					Pending
	2-08-021-2	US		CORELESS LAYER BUILDUP STRUCTURE WITH LGA	T. Antesberger R. Das F. Egitto V. Markovich W. Wilson	4/22/2010	12/764,994					Pending
	2-08-021-3	US		CORELESS LAYER BUILDUP STRUCTURE WITH LGA AND JOINING LAYER	T. Antesberger R. Das F. Egitto V. Markovich W. Wilson	4/22/2010	12/764,997					Pending
1-09-001	2-09-001	US		CHEMICAL MODIFICATION OF CHROMATE CONVERSION COATED	L. Matienzo D. Sissenstein	12/16/2009	12/653,680	2011-0139364				Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				ALUMINUM WORK PIECES								
1-09-002	2-09-002	US		CONDUCTIVE PASTE COMPOSITION AND METHOD OF MAKING CIRCUITIZED SUBSTRATE	R. Das et al.	4/8/2011	13/082,502					Pending
1-09-003	2-09-003	US		SEMI-CONDUCTOR CHIP WITH COMPRESSIBLE CONTACT STRUCTURE AND ELECTRONIC PACKAGE UTILIZING SAME	H. Lin F. Egitto V. Markovich	7/15/2010	12/836,612					Pending
1-09-004				METHOD FOR CREATING PRESS FIT CONNECTORS	T. Dornbos et al.							
1-09-005	2-09-005	US		ELECTRONIC PACKAGE INCLUDING HIGH DENSITY INTERPOSER AND CIRCUITIZED SUBSTRATE ASSEMBLY UTILIZING SAME	T. Antesberger F. Egitto V. Markovich W. Wilson	11/30/2009	12/592,682	2011-0127664	6/2/2011			Pending

SCHEDULE - 1

074658.01352/22095298v.5

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
	2-090-005A	US		METHOD OF MAKING HIGH DENSITY INTERPOSER AND ELECTRONIC PACKAGE UTILIZING SAME	T. Antesberger F. Egitto V. Markovich W. Wilson	12/1/2009	12/592,734	2011-0126408				Pending
1-09-006	**2-09-006**	US		HIGH PERFORMANCE UNSUPPORTED MATERIAL FOR ELECTRONIC PACKAGING	K. Papathomas et al.							Trade Secret
1-09-007	**ON HOLD**			A SOLDER AND ELECTRICAL CONDUCTIVE ADHESIVE CONNECTION	D. Sissenstein							On Hold
1-09-008	**2-09-008**	US		HIGH DENSITY CONNECTOR FOR INTERCONNECTING FINE PITCH CIRCUIT PACKAGING STRUCTURES	B. Chan D. Alcoe	5/28/2010	12/789,642	2010-0323558	7/5/2011	7,972,178		Issued
1-09-009	**2-09-009**	US		ELECTRONIC PACKAGE AND METHOD OF MAKING SAME	R. Das F. Egitto V. Markovich	10/22/2010	12/910,020					Pending
1-09-010	**Trade Secret**			PROCESS OF KEEPING THE METERING ROLLERS OF A TREATER TOWER WET DURING THE PROCESSING OF MEGTRON6	D. Fiske et al.							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				PREPREG								
1-09-011	Trade Secret			NANO-MICRO FILLED CONDUCTING ADHESIVE CONTAINING EPOXY, FLUX AND LMP TOGETHER	R. Das et al.							Trade Secret
1-09-012	2-09-012	US		OXYGEN-PLASMA SURFACE MODIFICATION FO LIQUID CRYSTALLINE POLYMER FILM FOR INCREASED ADHESION TO COPPER AND SELF	M. Schadt et al	8/4/2011	13/197,804					Pending
1-09-013				PATTERNING OF POLYMERS TO CREATE SELECTED AREAS OF DIFFERENT SURFACE ENERGIES	F. Egitto et al							
1-09-014	ON HOLD			ARGON PLASMA ETCHING OF ASICS OR HIGH LEAD SOLDER BALL COMPONENTS TO REMOVE	D. Sissenstein et al							On Hold

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				OXIDATION								
1-09-015	**2-09-015**	US		METHOD OF SMALL CAVITY FORMATION ON BURIED RESISTOR LAYER USING FUSION BONDING	A. Bhatt et al							
1-09-016	**Trade Secret**				A. Bhatt et al							Trade Secret
1-09-017	**Trade Secret**				R. Das et al							Trade Secret
1-10-001	**2-10-001**	US		CIRCUITIZED SUBSTRATE WITH DIELECTRIC INTERPOSER ASSEMBLY AND METHOD	R. Das J. Lauffer V. Markovich J. McNamara	12/20/2010	12/972,700					Pending
1-10-002	**2-10-002**	US		ANTI-TAMPER MICROCHIP PACKAGE BASED ON THERMAL NANOFLUIDS OR FLUIDS	R. Das V. Markovich J. McNamara M. Poliks	9/17/2010	12/884,421					Pending
1-10-003	**2-10-003**	US		LAND GRID ARRAY (LGA) CONTACT CONNECTOR MODIFICATION	F. Marconi B. Bonitz W. Wilson	10/14/2010	12/904,305					Pending
1-10-004	**2-10-004**	US		CIRCUITIZED SUBSTRATE WITH LOW LOSS CAPACITIVE MATERIAL	R. Das et al.	10/10/2011	13/269,770					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No	Issued	Patent No.	Patent Expires	Status
				AND METHOD OF MAKING SAME								
1-10-005	**2-10-005**	US		SOLDER-ECA (ELECTRICALLY CONDUCTIVE ADHESIVE) BASED INTERCONNECTS FOR CZT CRYSTAL ATTACH	V. Markovich et al.	1/26/2012	13/358,716					Pending
1-10-006	**2-10-006**	US		CERAMIC THIN FILM BASED EMBEDDED CAPACITORS FOR ORGANIC PACKAGING	R. Das et al.							
1-10-007	**EI-2-10-007**	US		BIO-COMPATIBLE, STRETCHABLE SUBSTRATES (BIOFLEX) FOR ELECTRONIC TEXTILES AND MEDICAL APPLICATIONS	R. Das et al.							
1-10-008	**2-10-008**	US		METAL BUMP CONTACT FOR FLEXIBLE SUBSTRATES, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	W. Wilson et al.	7/19/2011	13/184,882					Pending

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-10-009	**2-10-009**	US		ELECTRONIC PACKAGE WITH THERMAL INTERPOSER AND METHOD OF MAKING SAME	V. Markovich R. Das F. Egitto J. McNamara	2/8/2011	13/022,654					Pending
1-10-010	**2-10-010**	US		3D-PACKAGE INTERPOSER PACKAGE (PIP)	R. Das et al.							
1-10-011	**2-10-011**	US		INTEGRATED CIRCUIT DIE COVERPLATE FOR ANTI-TAMPER PACKAGING	M. Vincent et al.							
1-10-012	**2-10-012**	US		THERMAL SUBSTRATE	F. Egitto et al.	7/25/2011	13/189,980					Pending
1-10-013	**2-10-013**	US		PROCESS TO PURIFY WASTEWATER GENERATED IN THE PROCESS OF HYDRO FRACTURING OF NON-CONVENTIONAL GEOLOGIC FORMATIONS	P. Speranza et al.	9/21/2011	13/238,392					Pending
1-10-014	**2-10-014**	US		MINIATURIZED ELECTRONICS AS SPYING DEVICE	R. Das et al.							
1-10-015	**EI-2-10-015**	US		RIGID-FLEX CONSTRUCTION	F. Egitto et al.							

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-10-016	**EI-2-10-016**	US		PROCEDURE TO RUN FOLLOW ON PROCESSES FOR PRODUCT THAT WAS RUN ON THE OPTICAL REGISTRATION SYSTEM AT LAYUP/LAMINATIONS	R. Yale et al.							Publicly Disclosed
1-10-017	**EI-2-10-017**	US		PINNING METHOD FOR THE LAMINATIONS PROCESS	R. Yale et al.							
1-10-018	**2-10-018**	US		BUMPED CONNECTION FOR FLEX SUBSTRATES	W. Wilson et al.	9/22/2011	13/239,544					Pending
1-10-019	**See 2-10-023**			PACKAGING USING LIQUID IMMERSION COOLING OF ELECTRONIC ASSEMBLIES	B. Chan et al.							Combined with 2-10-023
1-10-020	**EI-2-10-020**	US		CIRCUITIZED SUBSTRATE WITH EMBEDDED RFID FOR TRACKING DEVICES	R. Das et al.							
1-10-021	**EI-2-10-021**	US		CIRCUITIZED SUBSTRATE WITH EMBEDDED CAPACITORS FOR ANTI TAMPERING	R. Das et al.							

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
1-10-022	**EI-2-10-022**	US		SELF DESTRUCTIVE INTEGRATED CIRCUIT DIE FOR ANTI-TAMPER PACKAGING	M. Vincent et al.							
1-10-023	**2-10-023**	US		SYSTEM ARCHITECTURE WITH STACKING SUBASSEMBLIES WITHOUT ROUTING HIGHSPEED SIGNALS THROUGH BACKPLANES	B. Chan et al.							
1-10-024	**EI-2-10-024**	US		NOVEL SPRING CONNECTION FOR CZT CRYSTAL ASSEMBLY	B. Chan et al.							
1-10-025	**Trade Secret**			CIRCUITIZED SUBSTRATE WITH RECHARGEABLE EMBEDDED BATTERY	R. Das et al.							Trade Secret (Combined with EI-1-11-004)
1-11-001	**EI-2-11-001**			CIRCUITIZED SUBSTRATE WITH LOCALIZED BENDING	R. Das et al.							Trade Secret
1-11-002	**Trade Secret**				R. Das et al.							Trade Secret
1-11-003	**Trade Secret**			DOUBLE SIDE CIRCUITIZATION FOR MULTILAYER	R. Das et al.							Trade Secret

SCHEDULE - 1

Discl. No.	Docket No.	Country	PR	Title	Inventor(s)	Filing Date	Appl. No.	Publication No.	Issued	Patent No.	Patent Expires	Status
				FLEX								
1-11-004	See EI-2-11-001			DESIGN ENHANCEMENTS FOR IMPROVING REGISTRATION AND ELECTRICAL YIELD FOR MULTILAYER FLEXIBLE SUBSTRATE	R. Das et al.							Trade Secret (Combined with EI-1-11-001)
1-11-005	Trade Secret			BLISTER ELIMINATION PROCESS	C. Palomaki et al.							Trade Secret
1-11-006	EI-2-11-006	US		CIRCUITIZED SUBSTRATE WITH EMBEDDED CAPACITORS, EMBEDDED RESISTORS AND EMBEDDED RFID	R. Das, et al.							
1-11-007	EI-2-11-007	US		CORE EZ WITH LCP CORE	M. Schadt							We in the process of building customer prototypes

SCHEDULE - 1

POWER OF ATTORNEY

ENDICOTT INTERCONNECT TECHNOLOGIES, INC., a New York corporation ("Endicott"), EI TRANSPORTATION COMPANY LLC, a Delaware limited liability company ("EI Transport"), ENDICOTT MEDTECH, INC., a New York corporation ("Medtech," together with Endicott and EI Transport, collectively, the "Grantor"), hereby authorizes PNC BANK, NATIONAL ASSOCIATION, its successors and assigns, and any officer or agent thereof (collectively, "Agent"), as agent for the Lenders under that certain Revolving Credit and Security Agreement among Agent, the financial institutions which are now or which hereafter become a party thereto as lenders (the "Lenders"), and Grantor, dated as of February 10, 2012 (as it may hereafter be amended, modified, restated or replaced from time to time, the "Loan Agreement"), during the continuance of an Event of Default (as defined in the Loan Agreement) as the true and lawful attorney-in-fact of Grantor, with the power to endorse the name of Grantor on all applications, assignments, documents, papers and instruments necessary for Agent to enforce and effectuate its rights under that certain Trademark and Patent Security Agreement between Grantor and Agent dated as of February 10, 2012 (as it may hereafter be supplemented, restated, superseded, amended or replaced, the "Trademark and Patent Security Agreement"), including, without limitation, the power to record its interest in any Trademarks and Patents (as defined in the Trademark and Patent Security Agreement) or additional trademarks and patents of Grantor in the United States Patent and Trademark Office or other appropriate governmental office including, without limitation, the power to execute on behalf of Grantor, a supplement to the Trademark and Patent Security Agreement, to use the Trademarks and Patents or to grant or issue any exclusive or non-exclusive license under the Trademarks or Patents to anyone else, or to assign, pledge, convey or otherwise transfer title in or dispose of the Trademarks or Patents to anyone else including, without limitation, the power to execute on behalf of Grantor, a Trademark or Patent, in each case subject to the terms of the Trademark and Patent Security Agreement. Nothing herein contained shall obligate Agent to use or exercise any rights granted herein.

This Power of Attorney is given and any action taken pursuant hereto is intended to be so given or taken pursuant to and subject to the provisions of the Loan Agreement.

Grantor hereby unconditionally ratifies all that such attorney shall lawfully do or cause to be done following the occurrence and during the continuance of an Event of Default by virtue hereof and in accordance with the terms of the Trademark and Patent Security Agreement, the Loan Agreement and the Other Documents.

This Power of Attorney shall be irrevocable for the life of the Trademark and Patent Security Agreement.

IN WITNESS WHEREOF, Grantor has executed this Power of Attorney as of the date stated above.

ENDICOTT INTERCONNECT TECHNOLOGIES, INC.

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

ENDICOTT MEDTECH, INC.

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

EI TRANSPORTATION COMPANY, LLC

By: Endicott Interconnect Technologies, Inc., its sole member

By: William Lynn
Name: William Lynn
Title: Chief Financial Officer

COMPANY ACKNOWLEDGMENT

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6 day of February, 2012, by William Lynn as CFO of Endicott Interconnect Technologies, Inc.

[Seal] ANN B. CIANFLONE
Notary Public, State of New York
No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/____

Notary Public, State of New York
My commission expires on 2/13/2013

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6 day of February, 2012, by William Lynn as CFO of EI Transportation Company, LLC.

[Seal] ANN B. CIANFLONE
Notary Public, State of New York
No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/____

Notary Public, State of New York
My commission expires on 2/13/2013

State of New York)
: SS
County of Broome)

This instrument was acknowledged before me on the 6 day of February, 2012, by William Lynn as CFO of Endicott Medtech, Inc.

[Seal] ANN B. CIANFLONE
Notary Public, State of New York
No. 02CI6141144
Residing in Broome County
My Commission Expires 2/13/____

Notary Public, State of New York
My commission expires on 2/13/2013

[ACKNOLWEDGEMENT TO POWER OF ATTORNEY TO TRADEMARK AND PATENT SECURITY AGREEMENT]